

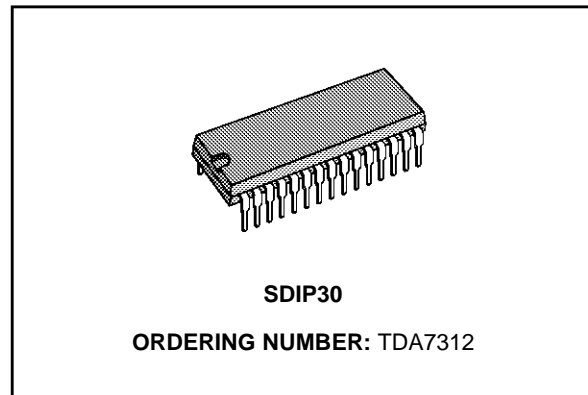
## DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

ADVANCE DATA

- INPUT MULTIPLEXER:
  - 4 STEREO INPUTS
- FOUR SELECTABLE ADDRESSES
- TWO DIGITAL CONTROL OUTPUTS
- INPUT AND OUTPUT FOR EXTERNAL EQUALIZER OR NOISE REDUCTION SYSTEM
- VOLUME CONTROL IN 1.25dB STEPS
- TREBLE AND BASS CONTROL
- TWO SPEAKER ATTENUATORS:
  - INDEPENDENT SPEAKERS CONTROL IN 1.25dB STEPS
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I<sup>2</sup>C BUS

### DESCRIPTION

The TDA7312 is a volume, tone (bass and treble) balance (Left/Right) processor for quality audio applications.

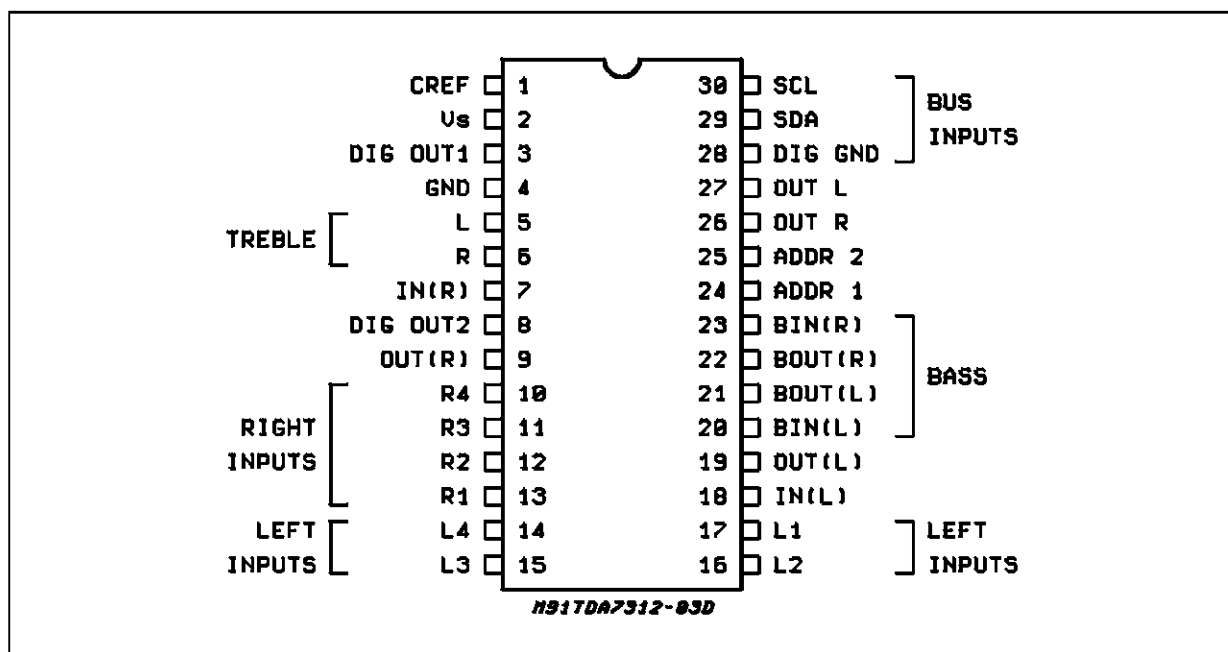


Control is accomplished by serial I<sup>2</sup>C bus microprocessor interface.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

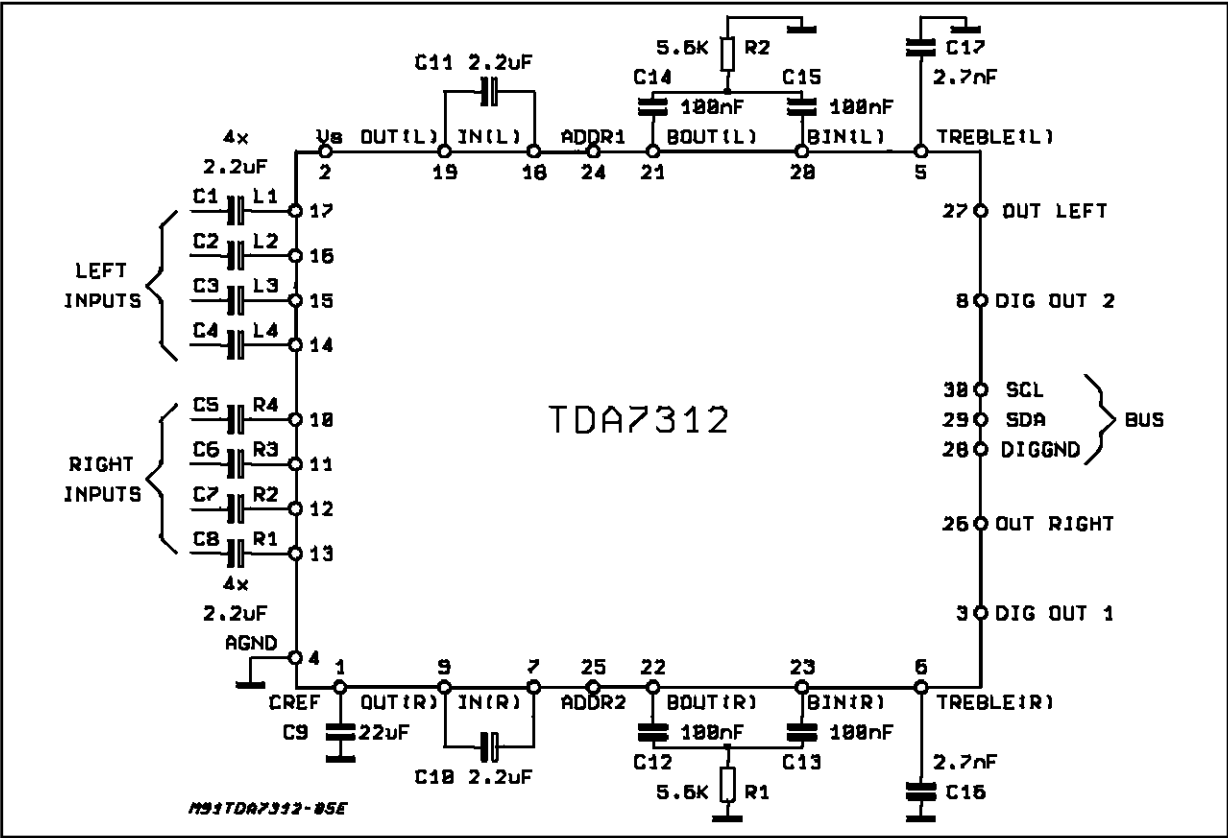
Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and Low DC stepping are obtained.

### PIN CONNECTION (Top view)



TDA7312

TEST CIRCUIT



THERMAL DATA

Symbol	Description	SDIP30	Unit
R <sub>th j-pins</sub>	Thermal Resistance Junction-pins	max	85

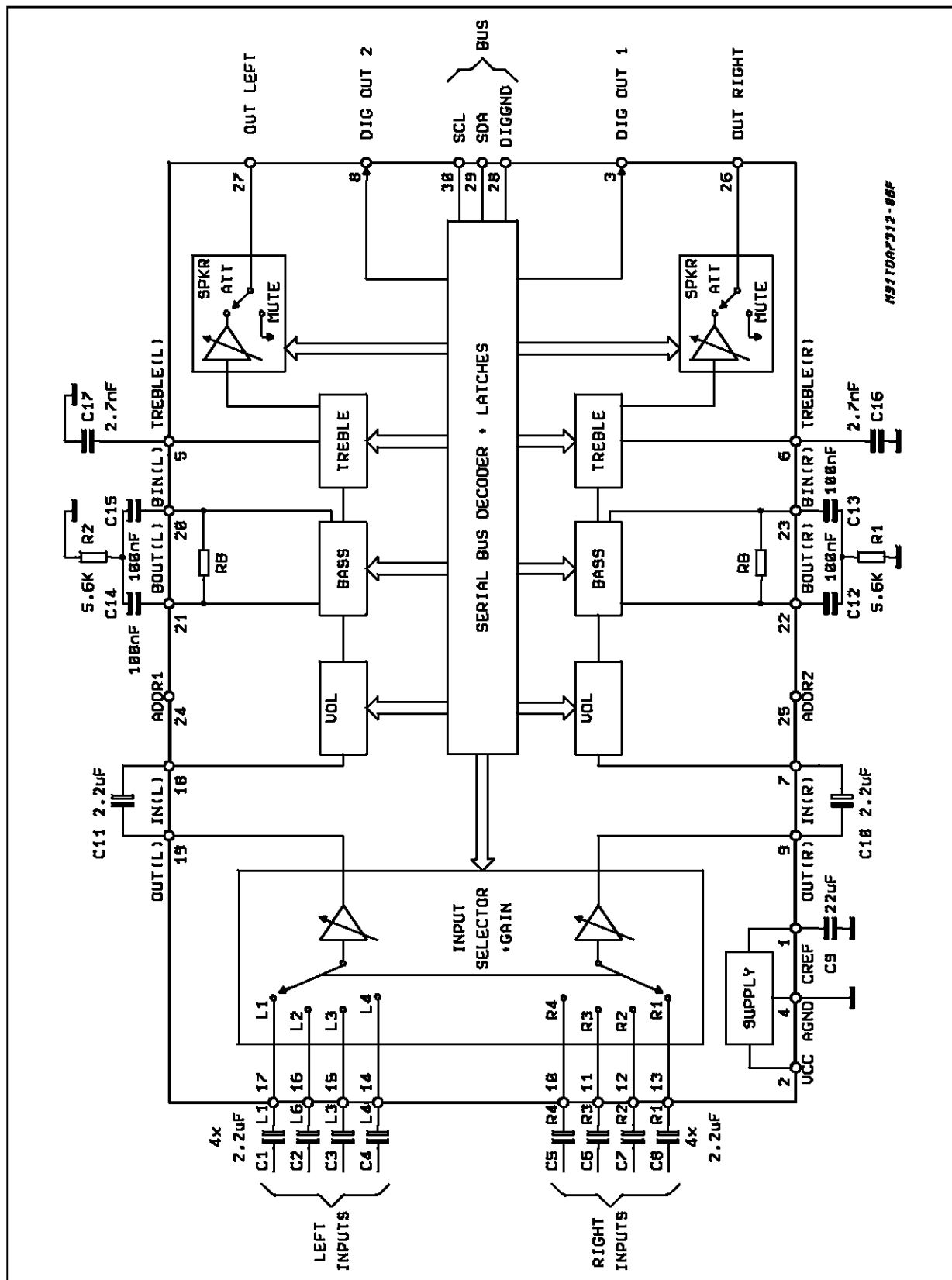
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>S</sub>	Operating Supply Voltage	10.2	V
T <sub>amb</sub>	Operating Ambient Temperature	0 to 70	°C
T <sub>stg</sub>	Storage Temperature Range	-40 to 150	°C

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>S</sub>	Supply Voltage	6	9	10	V
V <sub>CL</sub>	Max. input signal handling	2			V <sub>rms</sub>
THD	Total Harmonic Distortion V = 1V <sub>rms</sub> f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio		106		dB
Sc	Channel Separation f = 1KHz		103		dB
	Volume Control 1.25dB step	-78.75		0	dB
	Bass and Treble Control 2db step	-14		+14	dB
	Fader and Balance Control 1.25dB step	-38.75		0	dB
	Mute Attenuation		100		dB

## BLOCK DIAGRAM



## TDA7312

**ELECTRICAL CHARACTERISTICS** (refer to the test circuit  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_S = 9\text{V}$ ,  $R_L = 10\text{K}\Omega$ ,  $R_G = 600\Omega$ , all controls flat ( $G = 0$ ),  $f = 1\text{KHz}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

### SUPPLY

$V_S$	Supply Voltage		6	9	10	V
$I_S$	Supply Current			8	11	mA
SVR	Ripple Rejection		60	80		dB

### INPUT SELECTORS

$R_{II}$	Input Resistance	Input 1, 2, 3	35	50	70	$\text{K}\Omega$
$V_{CL}$	Clipping Level		2	2.5		Vrms
$S_{IN}$	Input Separation (2)		80	100		dB
$R_L$	Output Load resistance		2			$\text{K}\Omega$
$e_{IN}$	Input Noise			2		$\mu\text{V}$

### VOLUME CONTROL

$R_{IV}$	Input Resistance		20	33	50	$\text{k}\Omega$
$C_{RANGE}$	Control Range		70	75	80	dB
$A_{VMIN}$	Min. Attenuation		-1	0	1	dB
$A_{VMAX}$	Max. Attenuation		70	75	80	dB
$A_{STEP}$	Step Resolution		0.5	1.25	1.75	dB
$E_A$	Attenuation Set Error	$A_v = 0$ to $-20\text{dB}$ $A_v = -20$ to $-60\text{dB}$	-1.25 -3	0	1.25 2	dB dB
$E_T$	Tracking Error				2	dB
$V_{DC}$	DC Steps	adjacent attenuation steps From $0\text{dB}$ to $A_v$ max		0 0.5	3 7.5	mV mV

### SPEAKER ATTENUATORS

$C_{range}$	Control Range		35	37.5	40	dB
$S_{STEP}$	Step Resolution		0.5	1.25	1.75	dB
$E_A$	Attenuation set error				1.5	dB
$A_{MUTE}$	Output Mute Attenuation		80	100		dB
$V_{DC}$	DC Steps	adjacent att. steps from 0 to mute		0 1	3 10	mV mV

### BASS CONTROL (1)

$G_b$	Control Range	Max. Boost/cut	$\pm 12$	$\pm 14$	$\pm 16$	dB
$B_{STEP}$	Step Resolution		1	2	3	dB
$R_B$	Internal Feedback Resistance		34	44	58	$\text{K}\Omega$

### TREBLE CONTROL (1)

$G_t$	Control Range	Max. Boost/cut	$\pm 13$	$\pm 14$	$\pm 15$	dB
$T_{STEP}$	Step Resolution		1	2	3	dB

### DIGITAL OUTPUTS

$V_{CESAT}$		$V_{OUT} = \text{Low } I_C = 1\text{mA}$		0.2	0.3	V
$I_{leak}$	I leakage	$V_{OUT} = V_S$			10	$\mu\text{A}$

**ELECTRICAL CHARACTERISTICS** (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

**AUDIO OUTPUTS**

$V_{OCL}$	Clipping Level	$d = 0.3\%$	2	2.5		Vrms
$R_L$	Output Load Resistance		2			K $\Omega$
$C_L$	Output Load Capacitance				10	nF
$R_{OUT}$	Output resistance		30	75	120	$\Omega$
$V_{OUT}$	DC Voltage Level		4.2	4.5	4.8	V

**GENERAL**

$e_{NO}$	Output Noise	BW = 20-20KHz, flat output muted all gains = 0dB		2.5 5	15	$\mu V$ $\mu V$
		A curve all gains = 0dB		3		$\mu V$
S/N	Signal to Noise Ratio	all gains = 0dB; $V_O = 1V_{rms}$		106		dB
d	Distortion	$A_V = 0$ , $V_{IN} = 1V_{rms}$ $A_V = -20dB$ , $V_{IN} = 1V_{rms}$ $V_{IN} = 0.3V_{rms}$		0.01 0.09 0.04	0.1 0.3	% % %
Sc	Channel Separation left/right		80	103		dB
	Total Tracking error	$A_V = 0$ to -20dB -20 to -60 dB		0 0	1 2	dB dB

**BUS INPUTS**

$V_{IL}$	Input Low Voltage				1	V
$V_{IH}$	Input High Voltage		3			V
$I_{IN}$	Input Current		-5		+5	$\mu A$
$V_O$	Output Voltage SDA Acknowledge	$I_O = 1.6mA$			0.4	V

ADDRESS PIN (Internal 50K $\Omega$  pull down resistor).**Notes:**SDA, SCL, DIG OUT 1, DIG OUT 2 Pins are high impedance when  $V_S = 0$ 

(1) Bass and Treble response see attached diagram (fig.16). The center frequency and quality of the resonance behaviour can be chosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network

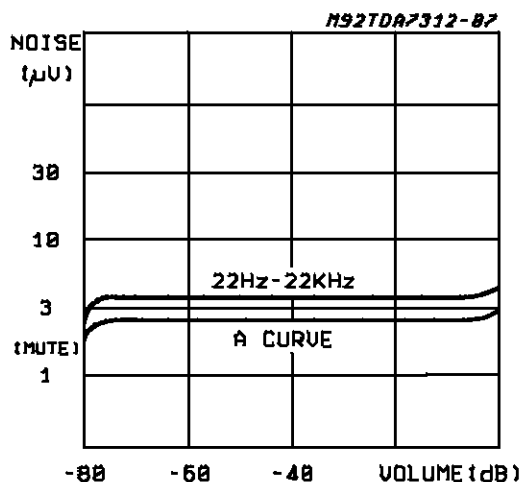
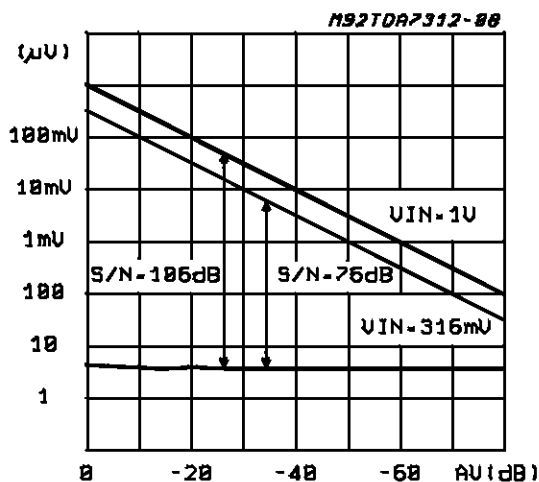
(2) The selected input is grounded thru the 2.2 $\mu F$  capacitor.**Figure 1:** Noise vs. Volume/Gain Settings**Figure 2:** Signal to Noise Ratio vs. Volume Setting

Figure 3: Distortion & Noise vs. Frequency

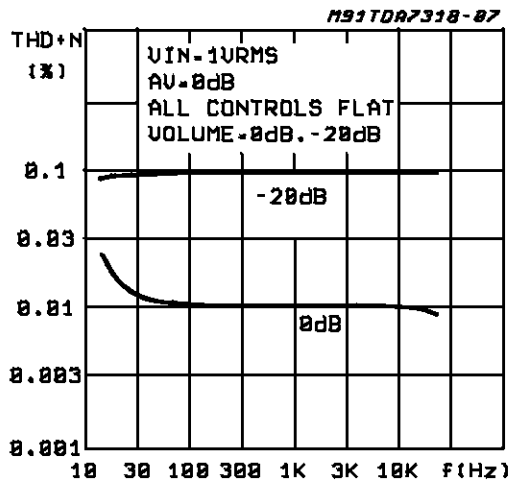


Figure 5: Distortion vs. Load Resistance

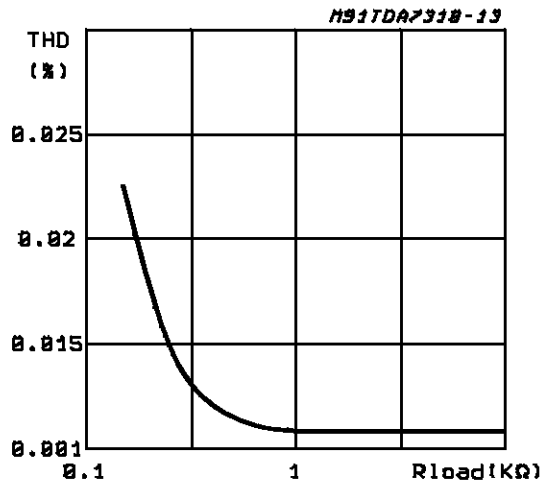


Figure 7: Input Separation (L1 → L2, L3, L4) vs. Frequency

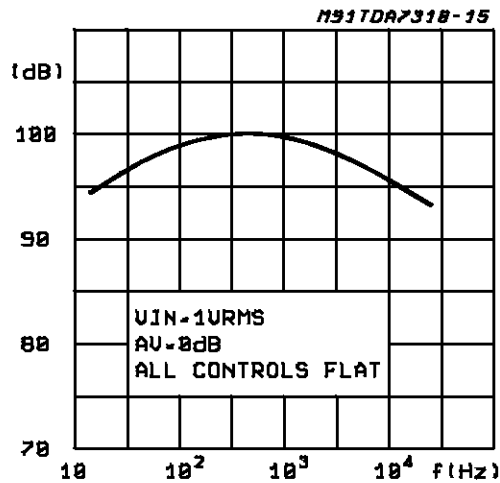


Figure 4: Distortion & Noise vs. Frequency

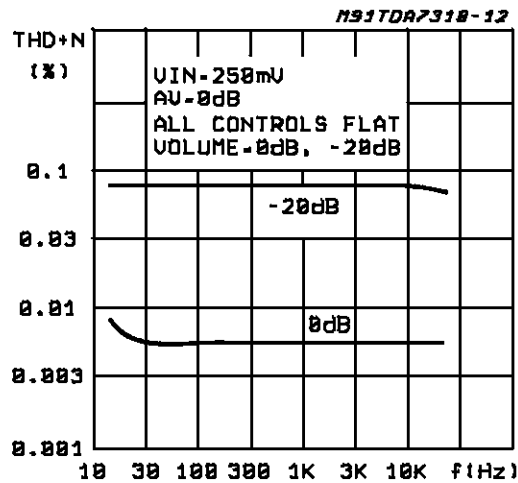


Figure 6: Channel Separation (L → R) vs. Frequency

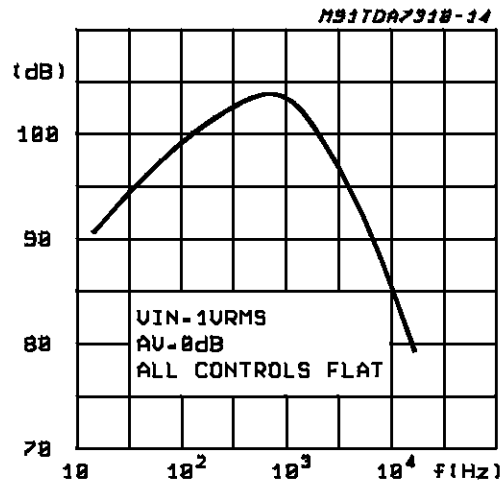
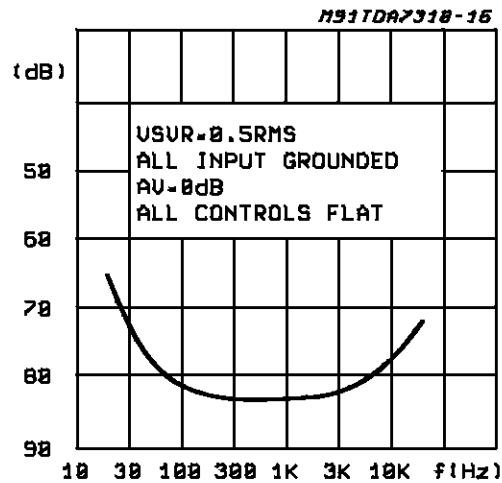
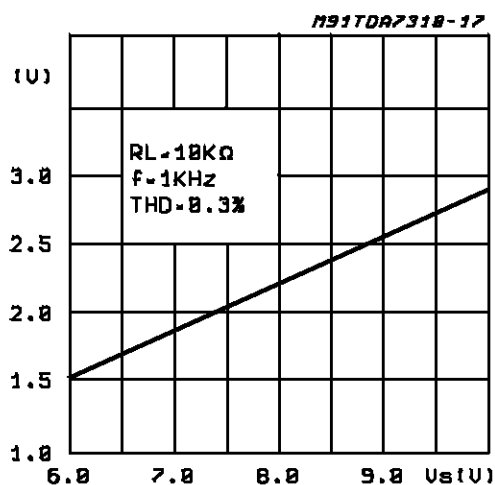
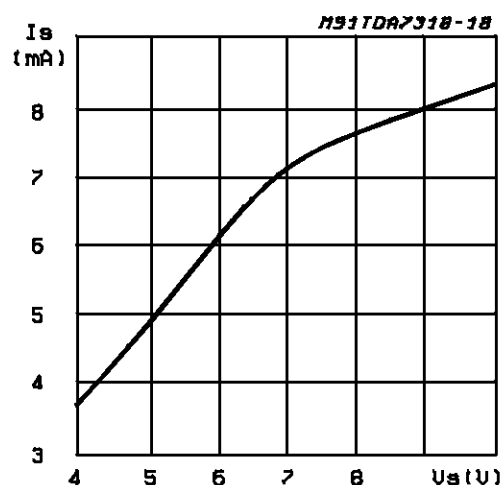
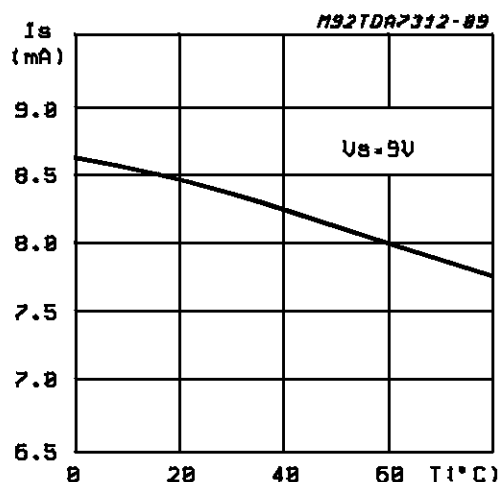
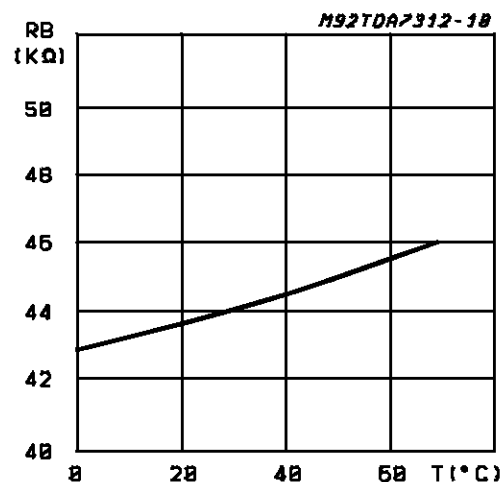
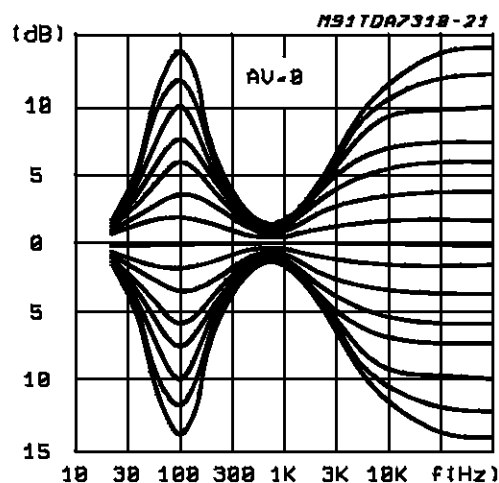


Figure 8: Supply Voltage Rejection vs. Frequency



**Figure 9:** Output Clipping Level vs. Supply Voltage**Figure 10:** Quiescent Current vs. Supply Voltage**Figure 11:** Supply Current vs. Temperature**Figure 12:** Bass Resistance vs. Temperature**Figure 13:** Typical Tone Response (with the ext. components indicated in the test circuit)

## I<sup>2</sup>C BUS INTERFACE

Data transmission from microprocessor to the TDA7312 and viceversa takes place thru the 2 wires I<sup>2</sup>C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

### Data Validity

As shown in fig. 14, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

### Start and Stop Conditions

As shown in fig.15 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

### Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an ac-

knowledge bit. The MSB is transferred first.

### Acknowledge

The master ( $\mu$ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 16). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

### Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the  $\mu$ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Figure 14: Data Validity on the I<sup>2</sup>C BUS

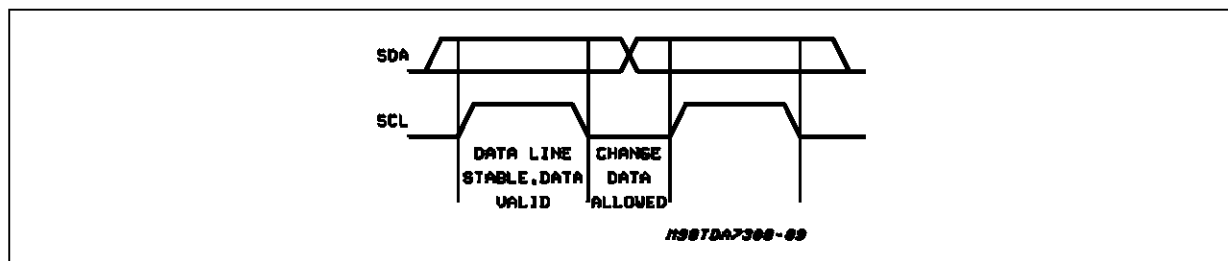


Figure 15: Timing Diagram of I<sup>2</sup>C BUS

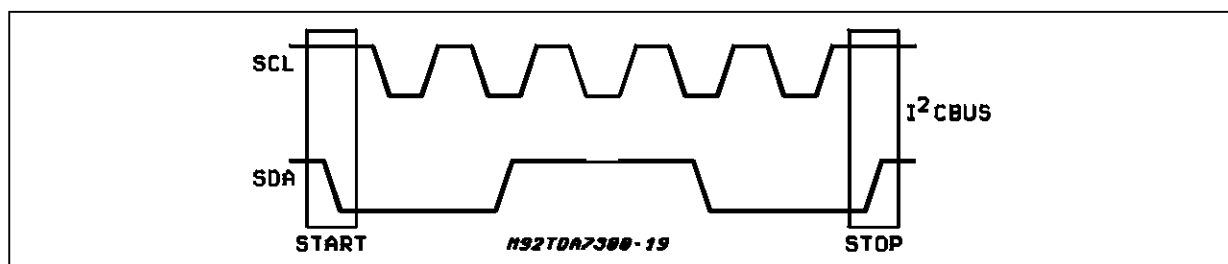
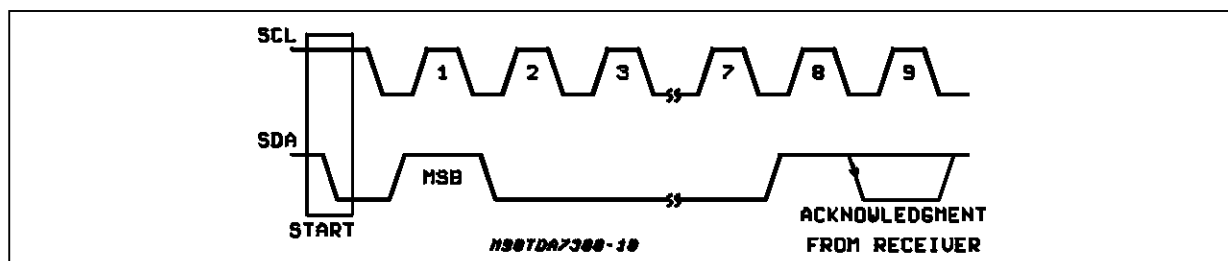


Figure 16: Acknowledge on the I<sup>2</sup>C BUS

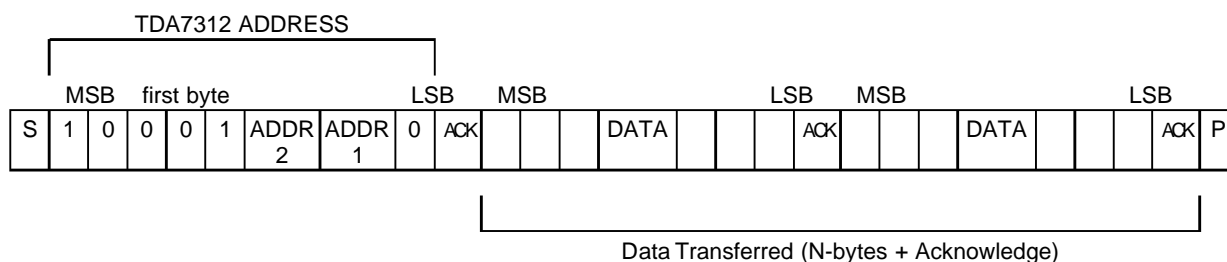




**SOFTWARE SPECIFICATION****Interface Protocol**

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7312 address (the 8th bit of the byte must be 0). The TDA7312 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge

S = Start

P = Stop

**SOFTWARE SPECIFICATION**

Chip address

1	0	0	0	1	ADDR 2	ADDR 1	0
MSB							LSB

ADDR2	ADDR1	CHIP ADDRESS
0	0	88 HEX
0	1	8A HEX
1	0	8C HEX
1	1	8E HEX

DATA BYTES

MSB								LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume control	
1	0	0	B1	B0	A2	A1	A0	Speaker ATT L	
1	0	1	B1	B0	A2	A1	A0	Speaker ATT R	
0	1	0	D2	D1	S2	S1	S0	Audio switch	
0	1	1	0	C3	C2	C1	C0	Bass control	
0	1	1	1	C3	C2	C1	C0	Treble control	

Ax = 1.25dB steps; Bx = 10dB steps; Cx = 2dB steps; Sx = Input Selector; Dx = Dig Out Pins

**SOFTWARE SPECIFICATION** (continued)

## DATA BYTES (detailed description)

**Volume**

MSB				LSB			FUNCTION	
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

For example a volume of -45dB is given by:

0 0 1 0 0 1 0 0

**Speaker Attenuators**

MSB						LSB			FUNCTION	
1	0	0	B1	B0	A2	A1	A0	Speaker L		
1	0	1	B1	B0	A2	A1	A0	Speaker R		
					0	0	0	0		
					0	0	1	-1.25		
					0	1	0	-2.5		
					0	1	1	-3.75		
					1	0	0	-5		
					1	0	1	-6.25		
					1	1	0	-7.5		
					1	1	1	-8.75		
			0011					0		
								-10		
								-20		
								-30		
			11		1	1	1	Mute		

For example attenuation of 25dB on speaker R is given by:

1 0 1 1 0 1 0 0

**Audio Switch**

MSB							LSB		FUNCTION
010			D2	D1	S2	S1	S0	Audio Switch	
			100					Stereo 1	
			101					Stereo 2	
			110					Stereo 3	
			111					Stereo 4	
			01					DIG. OUT 1 = 0	
			01					DIG. OUT 1 = 1	
			00					DIG. OUT 2 = 0	
			00					DIG. OUT 2 = 1	

**Bass and Treble**

0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

C3 = Sign

For example Bass at -10dB is obtained by the following 8 bit string:

0 1 1 0 0 0 1 0

**Status at Power on Reset**

Volume = 78.75dB

Treble = Bass = +2dB

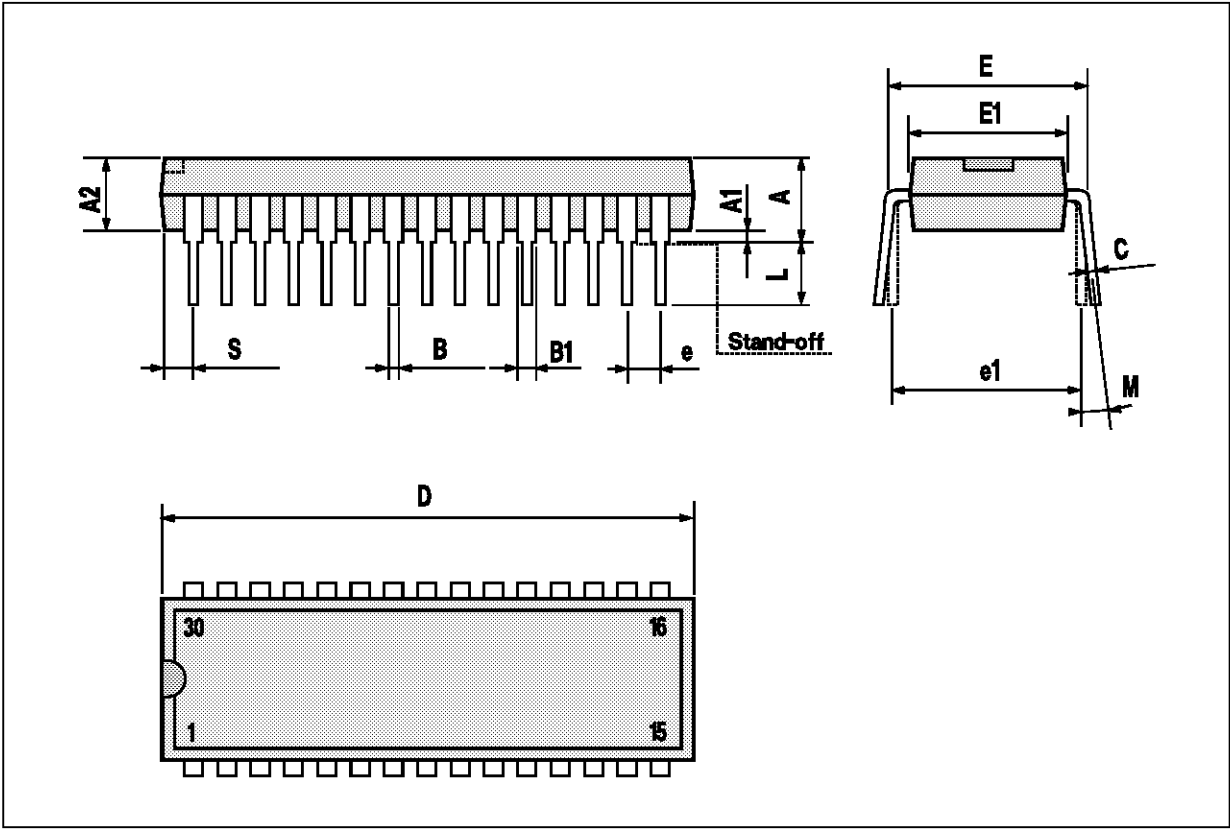
Spkrs Attenuators = Mute

Input = Stereo 1

Dig. OUT 1 = Dig. OUT 2 = 1

SDIP30 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.12	0.15	0.18
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	0.76	0.99	1.40	0.030	0.039	0.055
C	0.20	0.25	0.36	0.008	0.01	0.014
D	27.43	27.94	28.45	1.08	1.10	1.12
E	10.16	10.41	11.05	0.400	0.410	0.435
E1	8.38	8.64	9.40	0.330	0.340	0.370
e		1.78			0.070	
e1		10.16			0.400	
L	2.54	3.30	3.81	0.10	0.13	0.15
M	0°(min.), 15°(max.)					
S	0.31			0.012		



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