Advanced
Micro
Devices

Am85C30
Enhanced Serial Communication Controller

Application/Errata Note

Am85C30
Enhanced Serial Communication Controller (ESCC)

Application Note

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This application note is intended to clarify ESCC operation in relation to the "Valid Access Recovery Time parameter (#49)".

PROBLEM

The Am85C30 (ESCC) device may have invalid data written into its registers/FIFO if parameter #49 (Trc; Valid Access Recovery Time) is violated. This means that if the system (CPU) does another write operation, to ESCC or any other device, during the 3 to 3.5 PCLK time period required by the ESCC to complete its internal WRITE, the ESCC may write incorrect data to its internal registers/FIFO.

ESCC OPERATION

The ESCC WRITE timing with internal state machine WRITE is shown in Figure 1.

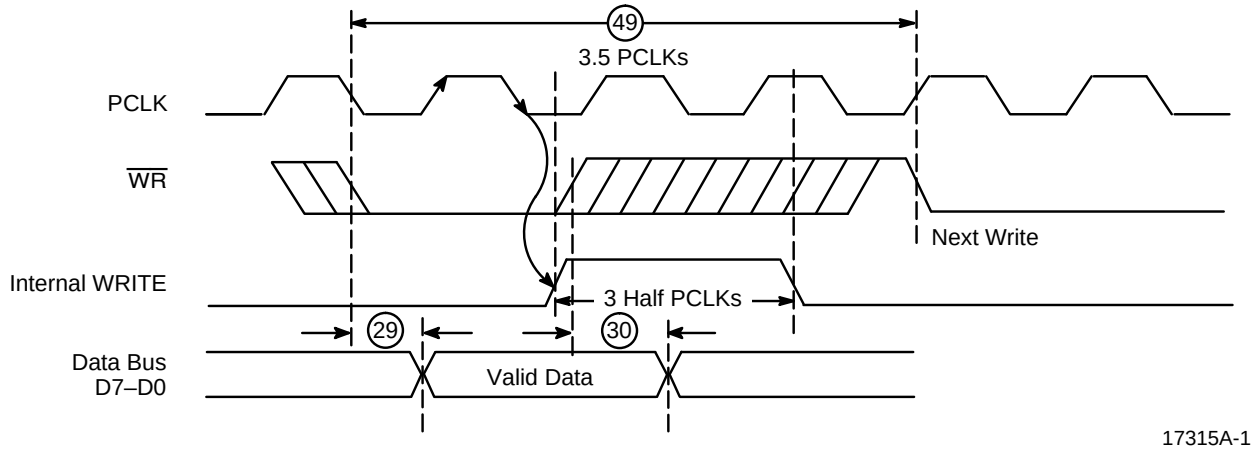

Figure 1

The ESCC does data writes to its FIFO or registers using an internal WRITE signal synchronized with PCLK. This write signal is generated from a state machine that starts the internal write operation only after the external write ($\overline{WR}$) signal goes active and the ESCC synchronizes this high to low transition of $\overline{WR}$ pulse with PCLK (using the next rising edge of PCLK followed by a falling edge). This synchronization can delay the internal write signal by 1/2 to 1 1/2 clocks depending on the external $\overline{WR}$ signal relationship to PCLK. The ESCC needs 3-Half (1 1/2) cycles of PCLK to complete the internal write operation. Data is latched internally on the rising edge of the $\overline{WR}$ signal. The data needs to be valid (setup time; parameter 29-TdWRf[DW]) before the rising edge of the $\overline{WR}$ and stay valid for the hold time (parameter 30-ThDW[WR]) to this edge for the data to be correctly written to the appropriate register or FIFO. Now if another $\overline{WR}$ is attempted (to ESCC or to some other device on the same bus) before the internal WRITE is gone inactive (i.e., in violation of parameter #49), this new undesired data could be latched by the $\overline{WR}$ pulse into the ESCC and subsequently written to its FIFO or registers.

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Am85C30 Errata and Workaround

Errata 1. Valid Access Recovery Time (Parameter #49) Violation

Problem:

ESCC may have invalid data written into its registers/ FIFO if another WRITE (to ESCC or some other device with the common WR strobe) is attempted during the valid access recovery time (i.e., parameter #49). The ESCC does not qualify the write strobe ($\overline{WR}$) with chip enable ($\overline{CE}$). In most applications PCLK is same or faster than CPU clock and the CPU cannot do another read or write access in the recovery time required by the ESCC, thus the above will not be a problem.

Workaround:

If PCLK is slower than CPU clock, then any extra non-ESCC WRITEs during the valid access recovery time can be stopped by gating the external $\overline{WR}$ with $\overline{CE}$ of the ESCC (see Figure 2 below).

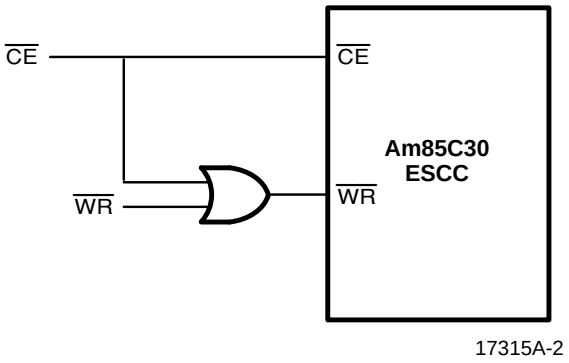

Figure 2

As far as extra ESCC WRITEs during the same valid access recovery time, there cannot be a workaround as this is a violation of parameter #49.

Errata 2. Read Back of Bit 4/ Write Register 5

Problem:

Read back of Bit 4 (Send Break)/Write Register 5 does not work, ESCC always returns '1' on read back.

Workaround:

None.