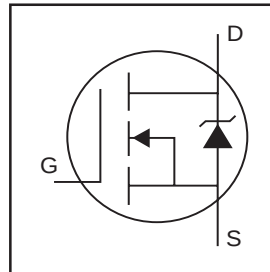


- Surface Mount (IRFR2407)
- Straight Lead (IRFU2407)
- Advanced Process Technology
- Dynamic dv/dt Rating
- Fast Switching
- Fully Avalanche Rated

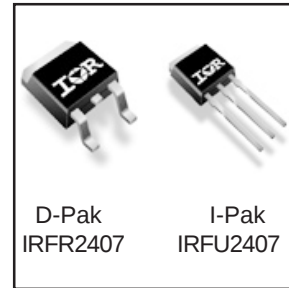
Description

Seventh Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



$V_{DS} = 75V$
$R_{DS(on)} = 0.026\Omega$
$I_D = 42A^{\circ}$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	42 [Ⓓ]	A
$I_D @ T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	29 [Ⓓ]	
I_{DM}	Pulsed Drain Current ^①	170	
$P_D @ T_C = 25^{\circ}C$	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ^②	130	mJ
I_{AR}	Avalanche Current ^①	25	A
E_{AR}	Repetitive Avalanche Energy ^①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ^③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

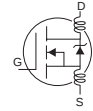
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

* When mounted on 1" square PCB (FR-4 or G-10 Material) .

For recommended footprint and soldering techniques refer to application note #AN-994

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.078	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0218	0.026	Ω	$V_{GS} = 10V, I_D = 25A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
g_{fs}	Forward Transconductance	27	—	—	S	$V_{DS} = 25V, I_D = 25A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 60V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	74	110	nC	$I_D = 25A$
Q_{gs}	Gate-to-Source Charge	—	13	19		$V_{DS} = 60V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	22	34		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 38V$
t_r	Rise Time	—	90	—		$I_D = 25A$
$t_{d(off)}$	Turn-Off Delay Time	—	65	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	66	—		$V_{GS} = 10V$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2400	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	340	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	77	—		$f = 1.0MHz$, See Fig. 5
C_{oss}	Output Capacitance	—	15700	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	220	—		$V_{GS} = 0V, V_{DS} = 60V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	220	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	42	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	170		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 25A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	100	150	ns	$T_J = 25^\circ\text{C}, I_F = 25A$
Q_{rr}	Reverse Recovery Charge	—	400	600	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.42mH$
 $R_G = 25\Omega, I_{AS} = 25A$.
- ③ $I_{SD} \leq 25A, di/dt \leq 290A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$

- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A

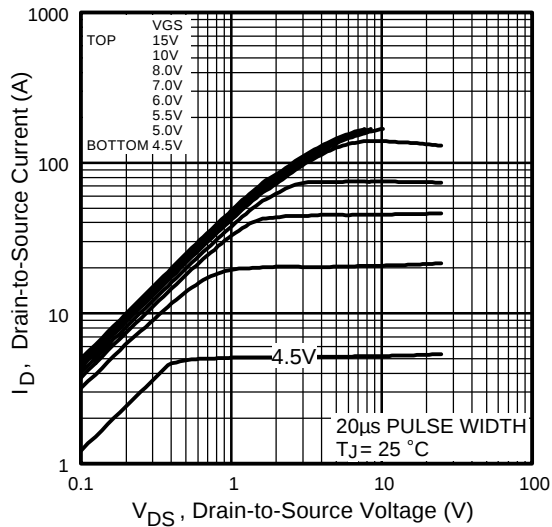


Fig 1. Typical Output Characteristics

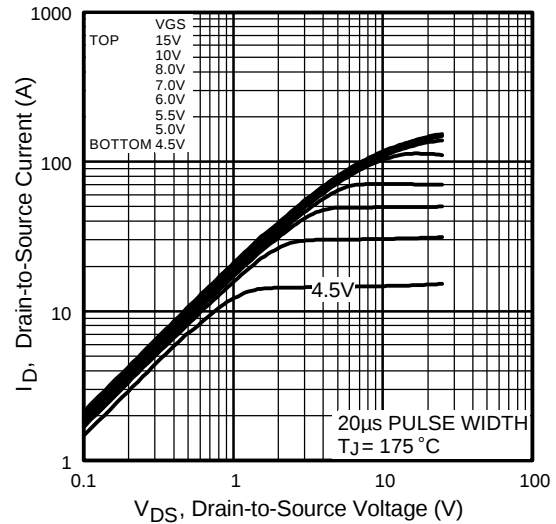


Fig 2. Typical Output Characteristics

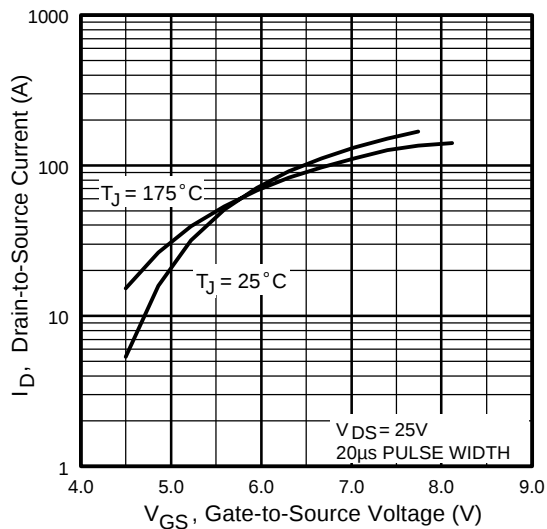


Fig 3. Typical Transfer Characteristics

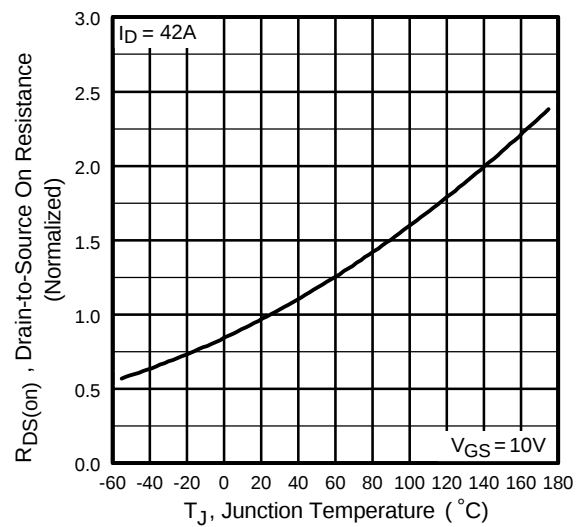


Fig 4. Normalized On-Resistance Vs. Temperature

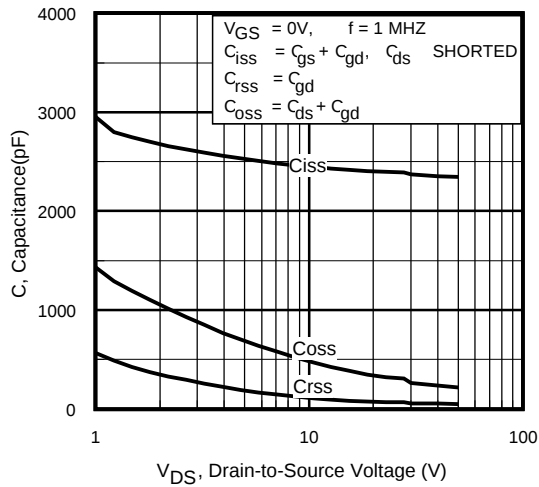


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

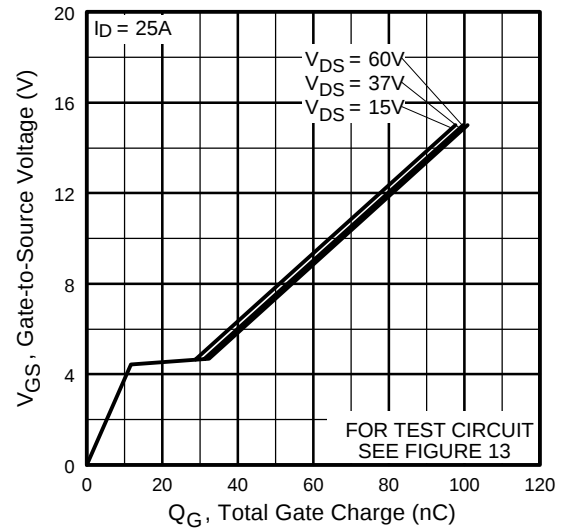


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

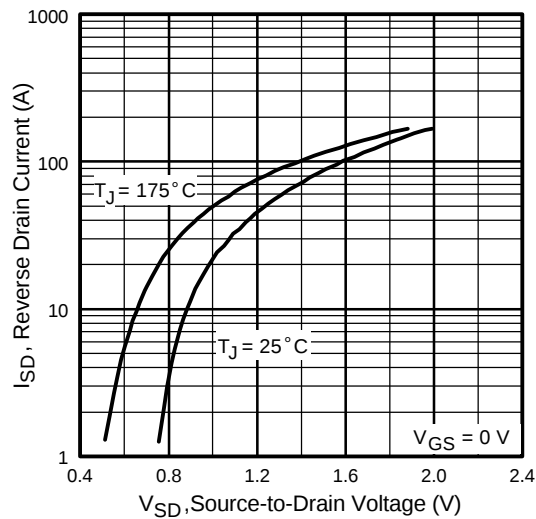


Fig 7. Typical Source-Drain Diode Forward Voltage

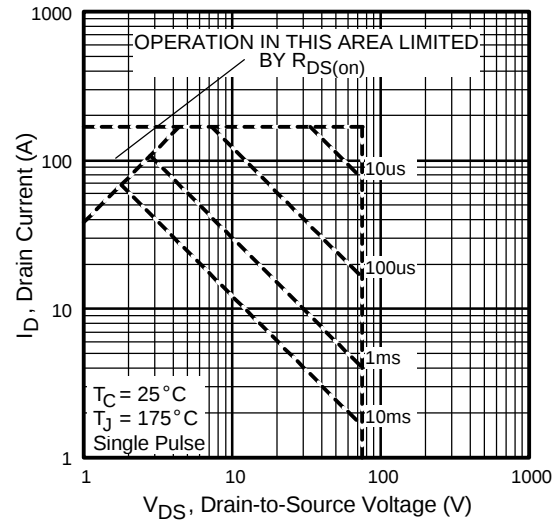


Fig 8. Maximum Safe Operating Area

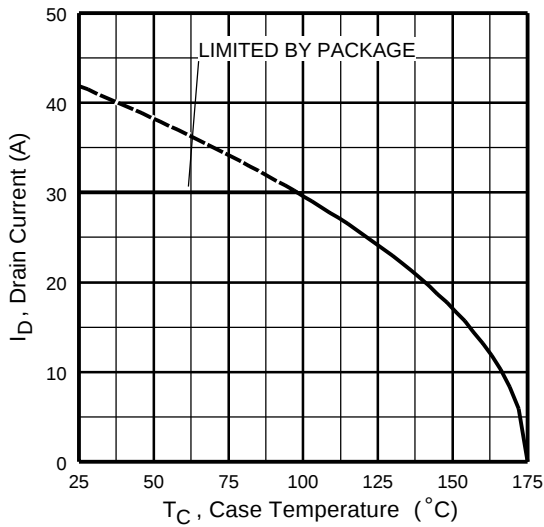


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

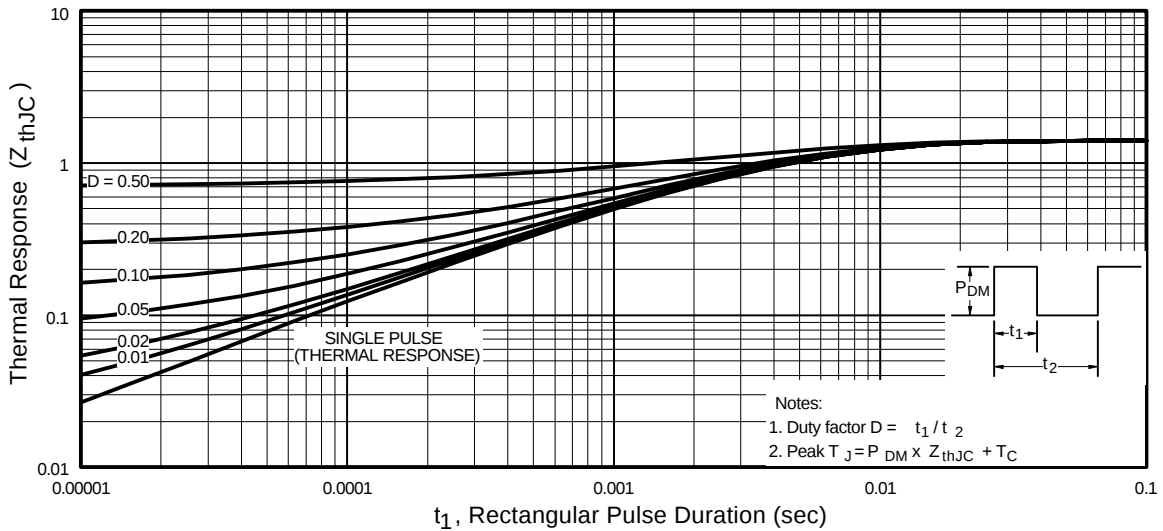


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

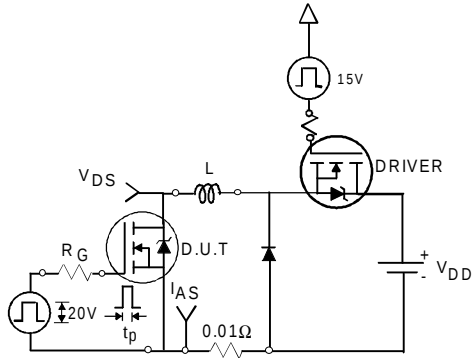


Fig 12a. Unclamped Inductive Test Circuit

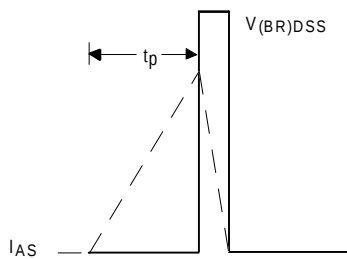


Fig 12b. Unclamped Inductive Waveforms

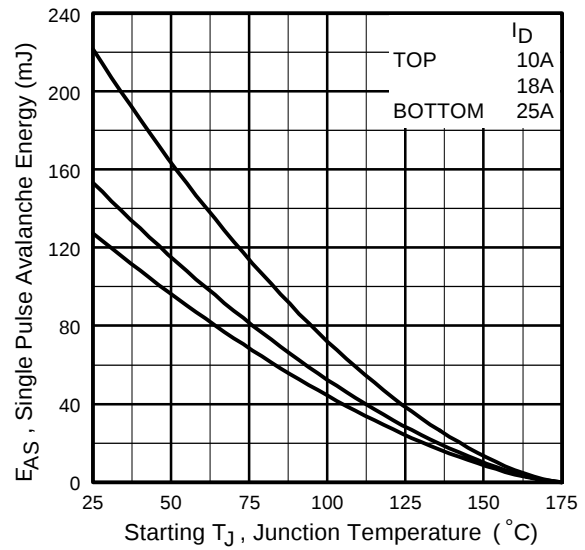


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

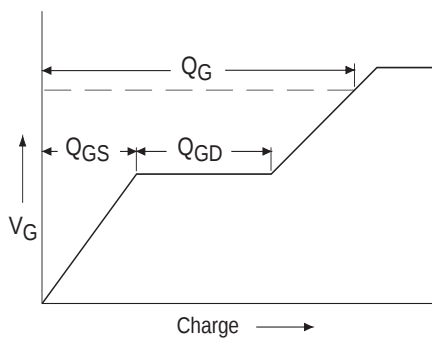


Fig 13a. Basic Gate Charge Waveform

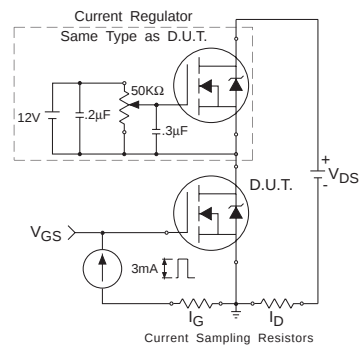
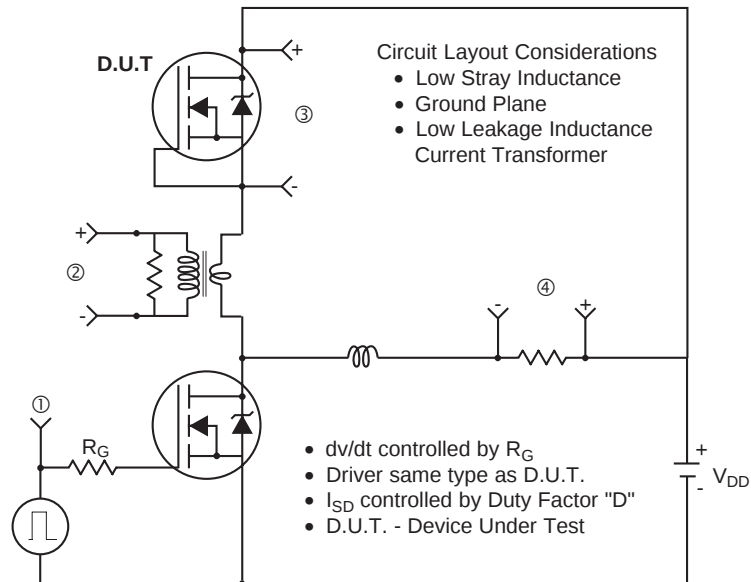


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

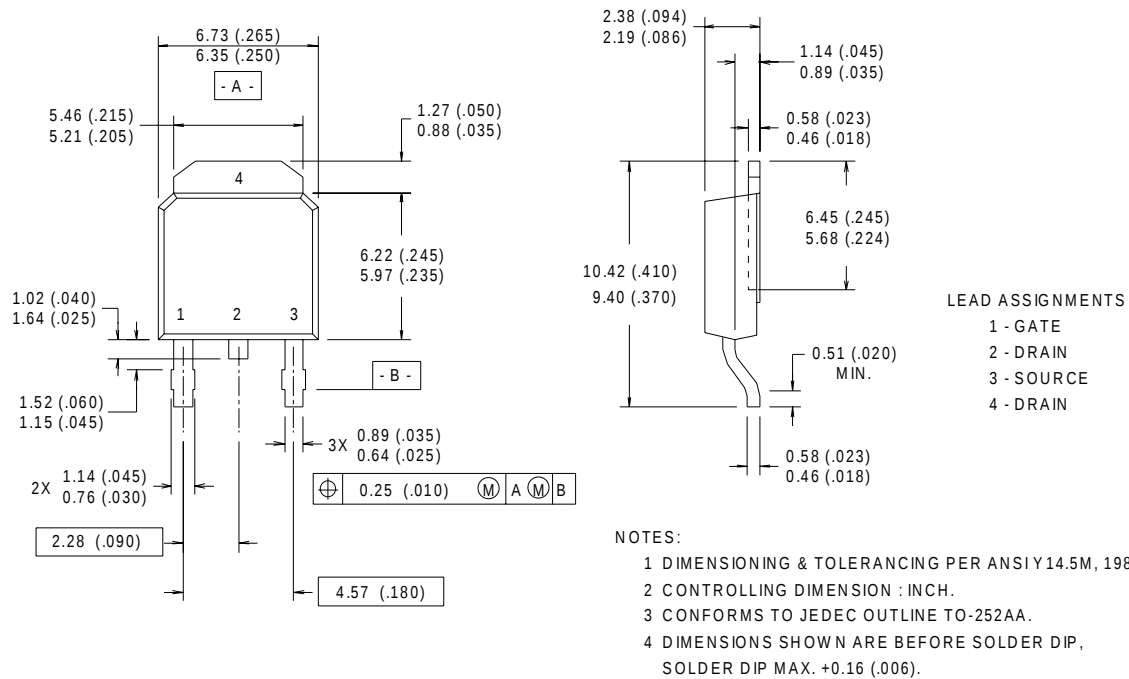
Fig 14. For N-Channel HEXFET® Power MOSFETs

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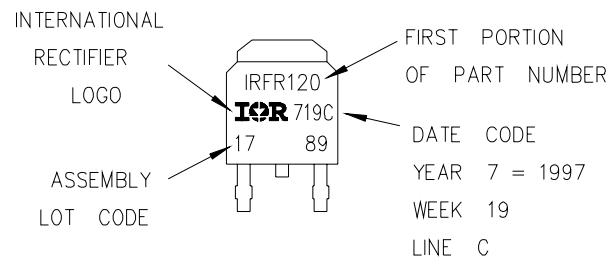
D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



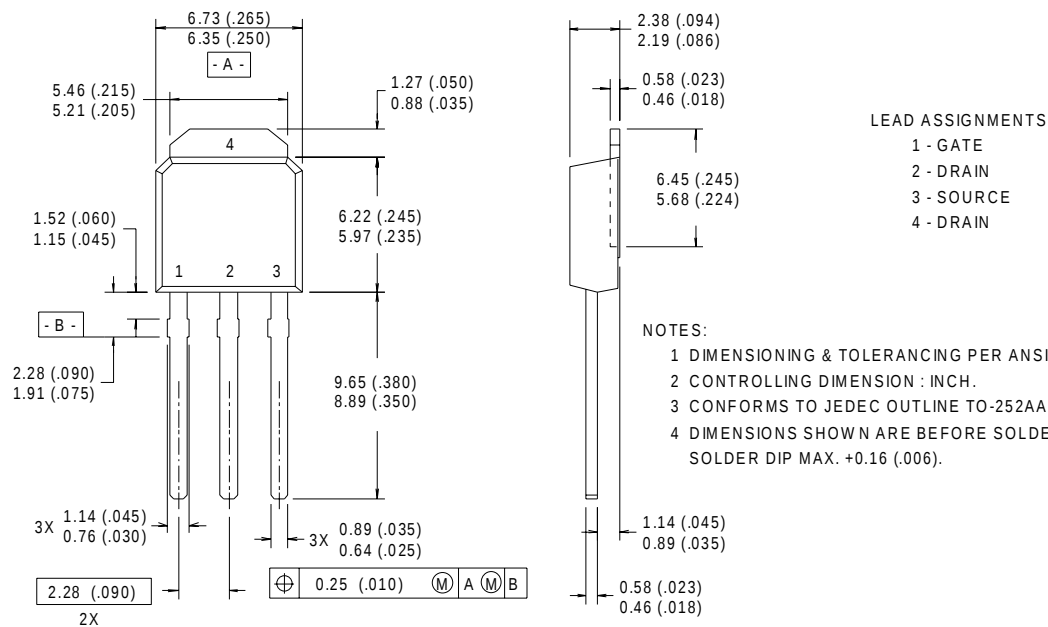
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



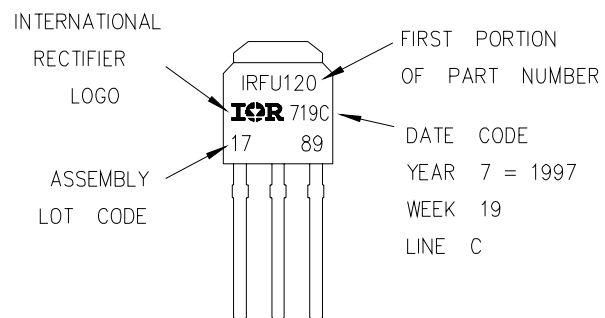
I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

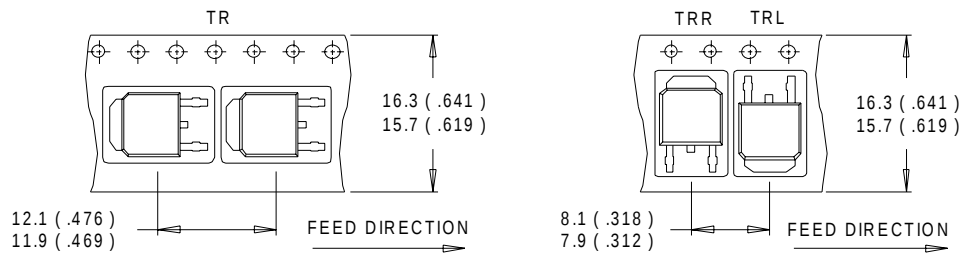


IRFR/U2407

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IR Rectifier

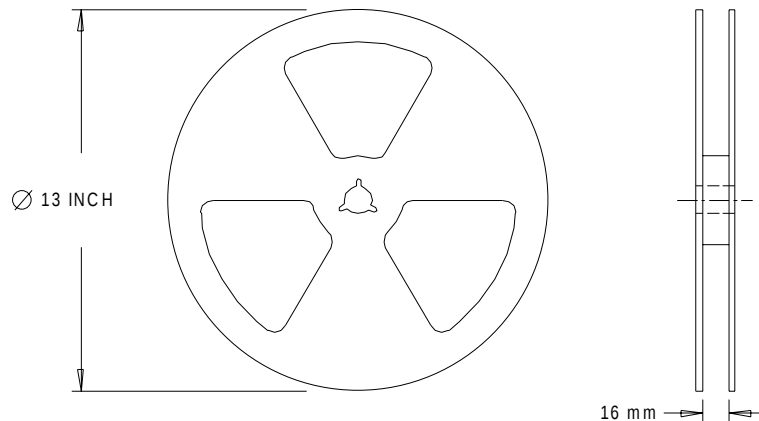
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

International
IR Rectifier

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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 3/00

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>