

## GENERAL DESCRIPTION

The SP510E is a highly integrated physical layer solution that is configurable to support multiple serial standards. It incorporates eight drivers and eight receivers (8TX/8RX), configurable for either differential (V.11 or V.35) or single ended (V.28 and V.10) signaling.

SP510E enables a Serial Communications Controller to implement a variety of serial port types including V.24, V.25, V.36, EIA-530, EIA-530-A, X.21, RS-232. The device architecture is designed to support the data and clock signals used in HDLC or SDLC serial ports as either DTE or DCE.

Operating configuration is programmable in system using the mode-select pins. The V.11 and V.35 modes include internal bus termination that may be switched in or out using the TERM\_OFF pin.

The SP510E is ideal for space constrained applications. It requires only a single 5V supply for full operation. The  $V_L$  pin determines the receiver output voltage ( $V_{OH}$ , down to 1.65V), for interfacing with lower voltage CPUs and FPGAs. For single supply operation at 5V the  $V_L$  pin will be connected to  $V_{CC}$ .

Fully compliant V.28 and V.10 driver output voltages are generated using the onboard charge pump. Special power sequencing is not required during system startup. Charge pump outputs are internally regulated to minimize power consumption. The SP510E requires only four 1 $\mu$ F capacitors for complete functionality. The device may be put into a low power shutdown mode when not in active use.

All receivers have fail-safe protection to put outputs into an output-high state when inputs are open, shorted, or terminated but idle.

## FEATURES

- Up to 52Mbps Differential Transmission Rates
- $\pm 15$ kV HBM ESD Tolerance for Analog I/O Pins
- Integrated Termination Resistors for V.11/V.35
- Eight Drivers and Eight Receivers (8TX/8RX)
- Adjustable Logic Level Pin  $V_L$  (Down to 1.65V)
- Software Selectable Protocols with 3-Bit Word:
  - RS-232 (V.28)
  - EIA-530 (V.10 & V.11)
  - EIA-530A (V.10 & V.11)
  - X.21 (V.11)
  - RS-449/V.36
- Internal Line or Digital Loopback Testing
- Adheres to NET1/NET2 and TBR2 Requirements
- Easy Flow-Through Pinout
- Single +5V Supply Voltage
- Individual Driver/Receiver Enable/Disable Controls
- Operates in DTE or DCE Mode
- Pin Compatible Upgrade for SP509, SP508

## TYPICAL APPLICATIONS

- Data Communication Networks
- Telecommunication Equipment
- Secured Data Communication
- CSU and DSU
- Data Routers
- Network Switches
- WAN Access Equipment
- VoIP-PBX Gateways

## ORDERING INFORMATION

| PART NUMBER | PACKAGE      | OPERATING TEMPERATURE RANGE | DEVICE STATUS |
|-------------|--------------|-----------------------------|---------------|
| SP510EEF-L  | 100-pin LQFP | -40°C to +85°C              | Active        |
| SP510ECF-L  | 100-pin LQFP | 0°C to +70°C                | Active        |

**ABSOLUTE MAXIMUM RATINGS**

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

|                                                                                                                                                                           |                              |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| Supply Voltage $V_{CC}$                                                                                                                                                   | +7.0V                        |
| Logic-Interface Voltage ( $V_L$ )                                                                                                                                         | $V_L \leq V_{CC}$            |
| Receiver DC Input Voltage                                                                                                                                                 | $\pm 15.5V$                  |
| Input Voltage at TTL Input Pins                                                                                                                                           | -0.3V to ( $V_{CC} + 0.5V$ ) |
| Driver Output Voltage (from Ground)                                                                                                                                       | -7.5V to +12.5V              |
| Short Circuit Duration, TxOUT to GND                                                                                                                                      | Continuous                   |
| Storage Temperature Range                                                                                                                                                 | -65°C to +150°C              |
| Lead Temperature (soldering, 10s)                                                                                                                                         | +300°C                       |
| Continuous Power Dissipation at $T_{AMB} = +70^\circ C$<br>100-Pin LQFP<br>(derate 19mW/°C above +70°C)<br>$\theta_{JA} = 52.7^\circ C/W$ , $\theta_{JC} = 6.5^\circ C/W$ | 1520mW                       |

**ESD PROTECTION**

|                           |          |    |                  |
|---------------------------|----------|----|------------------|
| TX Output & RX Input Pins | $\pm 15$ | kV | Human Body Model |
| All Other Pins            | $\pm 2$  | kV | Human Body Model |

**TABLE 1: DC ELECTRICAL CHARACTERISTICS**

| <b>DC ELECTRICAL CHARACTERISTICS</b>                                                                                                                                              |                   |                                                     |                     |       |                     |      |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----------------------------------------------------|---------------------|-------|---------------------|------|
| V <sub>CC</sub> = +4.75V to +5.25V, C1-C4 = 1μF. T <sub>AMB</sub> = T <sub>MIN</sub> to T <sub>MAX</sub> , unless otherwise noted. Typical values are at T <sub>AMB</sub> = +25°C |                   |                                                     |                     |       |                     |      |
| PARAMETERS                                                                                                                                                                        | SYMBOL            | TEST CONDITIONS                                     | MIN                 | TYP   | MAX                 | UNIT |
| V <sub>CC</sub> Supply Voltage                                                                                                                                                    | V <sub>CC</sub>   |                                                     | 4.75                |       | 5.25                | V    |
| Logic Interface Voltage                                                                                                                                                           | V <sub>L</sub>    | V <sub>L</sub> ≤ V <sub>CC</sub>                    | 1.65                |       | 5.25                | V    |
| I <sub>CC</sub> Supply Current                                                                                                                                                    | I <sub>CC</sub>   |                                                     |                     |       | 300                 | mA   |
| I <sub>CC</sub> Shutdown                                                                                                                                                          | I <sub>CCSD</sub> |                                                     |                     | 200   |                     | μA   |
| <b>DRIVER INPUT AND LOGIC INPUT PINS</b>                                                                                                                                          |                   |                                                     |                     |       |                     |      |
| Logic Input High                                                                                                                                                                  | V <sub>IH</sub>   |                                                     | 1.6                 |       |                     | V    |
| Logic Input Low                                                                                                                                                                   | V <sub>IL</sub>   |                                                     |                     |       | 0.4                 | V    |
| <b>RECEIVER OUTPUTS</b>                                                                                                                                                           |                   |                                                     |                     |       |                     |      |
| Receiver Logic Output Low                                                                                                                                                         | V <sub>OL</sub>   | I <sub>OUT</sub> = -3.2 mA                          |                     |       | 0.4                 | V    |
| Receiver Logic Output High                                                                                                                                                        | V <sub>OH</sub>   | I <sub>OUT</sub> = 1 mA                             | V <sub>L</sub> -0.3 |       | V <sub>L</sub> +0.3 | V    |
| Receiver Output Short-Circuit Current                                                                                                                                             | I <sub>OSS</sub>  | 0V < V <sub>O</sub> < V <sub>CC</sub>               |                     | ±20   | ±60                 | mA   |
| Receiver Output Leakage Current                                                                                                                                                   | I <sub>OZ</sub>   | Receivers disabled<br>0.4V < V <sub>O</sub> < 5.25V |                     | ±0.05 | ±1                  | μA   |
| <b>V.28 / RS-232 DRIVERS</b>                                                                                                                                                      |                   |                                                     |                     |       |                     |      |
| Output Voltage Swing                                                                                                                                                              | V <sub>T</sub>    | Output load = 3kΩ to GND<br>Figure 3                | ±5                  | ±6    | ±15                 | V    |
|                                                                                                                                                                                   | V <sub>OC</sub>   | Open Circuit Output<br>Figure 2                     |                     |       | ±15                 | V    |
| Short Circuit Current                                                                                                                                                             | I <sub>SC</sub>   | V <sub>OUT</sub> = 0V, Figure 5                     |                     |       | ±100                | mA   |
| Power-Off Impedance                                                                                                                                                               |                   | Figure 6                                            | 300                 | 10M   |                     | Ω    |
| <b>V.28 / RS-232 RECEIVERS</b>                                                                                                                                                    |                   |                                                     |                     |       |                     |      |
| Input Voltage Range                                                                                                                                                               |                   |                                                     | -15                 |       | 15                  | V    |
| Input Threshold Low                                                                                                                                                               |                   |                                                     | 0.8                 | 1.2   |                     | V    |
| Input Threshold High                                                                                                                                                              |                   |                                                     |                     | 1.7   | 3                   | V    |
| Input Hysteresis                                                                                                                                                                  |                   |                                                     |                     | 500   |                     | mV   |
| Input Resistance                                                                                                                                                                  |                   | Figure 8                                            | 3                   | 5     | 7                   | kΩ   |
| Open Circuit Bias                                                                                                                                                                 | V <sub>OC</sub>   | Figure 9                                            |                     |       | ±2                  | V    |

**DC ELECTRICAL CHARACTERISTICS**

$V_{CC} = +4.75V$  to  $+5.25V$ ,  $C1-C4 = 1\mu F$ ,  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_{AMB} = +25^{\circ}C$

| PARAMETERS                     | SYMBOL             | TEST CONDITIONS              | MIN         | TYP | MAX         | UNIT      |
|--------------------------------|--------------------|------------------------------|-------------|-----|-------------|-----------|
| <b>V.10 / RS-423 DRIVERS</b>   |                    |                              |             |     |             |           |
| Open Circuit Voltage           | $V_{OC}$           | Figure 10                    | $\pm 4$     |     | $\pm 6$     | V         |
| Test Terminated Voltage        | $V_T$              | Figure 11                    | $0.9V_{OC}$ |     |             | V         |
| Short Circuit Current          | $I_{SC}$           | Figure 12                    |             |     | $\pm 150$   | mA        |
| Power-Off Current              |                    | Figure 13                    |             |     | $\pm 100$   | $\mu A$   |
| <b>V.10 / RS-423 RECEIVERS</b> |                    |                              |             |     |             |           |
| Input Current                  | $I_{IA}$           | Figure 15 and Figure 16      | -3.25       |     | +3.25       | mA        |
| Input Impedance                |                    |                              | 4           | 15  |             | $k\Omega$ |
| Sensitivity                    |                    |                              |             |     | $\pm 0.2$   | V         |
| <b>V.11 / RS-422 DRIVERS</b>   |                    |                              |             |     |             |           |
| Open Circuit Voltage           | $V_{OCA}, V_{OCB}$ | Figure 17                    |             |     | $\pm 6$     | V         |
| Test Terminated Voltage        | $V_T$              | Figure 18                    | $\pm 2$     |     |             | V         |
| Balance                        | $\Delta V_T$       | Figure 18                    |             |     | $\pm 0.4$   | V         |
| Driver DC Offset               | $V_{OS}$           | Figure 18                    |             |     | 3           | V         |
| Offset Balance                 | $\Delta V_{OS}$    | Figure 18                    |             |     | $\pm 0.4$   | V         |
| Short Circuit Output Current   | $I_{SA}, I_{SB}$   | Figure 19                    |             |     | $\pm 150$   | mA        |
| Power-Off Current              |                    | Figure 20                    |             |     | $\pm 100$   | $\mu A$   |
| <b>V.11 / RS-422 RECEIVERS</b> |                    |                              |             |     |             |           |
| Receiver Input Range           | $V_{CM}$           |                              | -7          |     | +7          | V         |
| Input Current                  | $I_{IA}, I_{IB}$   | Figure 21 and Figure 23      |             |     | $\pm 3.25$  | mV        |
| Input Current with Termination | $I_{IA}, I_{IB}$   | Figure 24 and Figure 25      |             |     | $\pm 60.75$ | mA        |
| Receiver Input Impedance       | $R_{IN}$           | $-10V \leq V_{CM} \leq +10V$ | 4           | 15  |             | $k\Omega$ |
| Receiver Sensitivity           | $V_{TH}$           |                              |             |     | $\pm 0.2$   | V         |
| Receiver Input Hysteresis      | $\Delta V_{TH}$    | $V_{CM} = 0 V$               |             | 15  |             | mV        |

**DC ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub> = +4.75V to +5.25V, C1-C4 = 1μF. T<sub>AMB</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>AMB</sub> = +25°C

| PARAMETERS                                                      | SYMBOL          | TEST CONDITIONS                                                     | MIN                 | TYP  | MAX                 | UNIT |
|-----------------------------------------------------------------|-----------------|---------------------------------------------------------------------|---------------------|------|---------------------|------|
| <b>V.35 DRIVERS (ALL VALUES MEASURED WITH TERM_OFF = '0')</b>   |                 |                                                                     |                     |      |                     |      |
| Test Terminated Voltage                                         | V <sub>T</sub>  | Figure 26                                                           | ±0.44               |      | ±0.66               | V    |
| Offset                                                          | V <sub>OS</sub> | Figure 26                                                           |                     |      | ±0.6                | V    |
| Output Overshoot                                                |                 | Figure 26,<br>V <sub>ST</sub> = Steady State Voltage                | -0.2V <sub>ST</sub> |      | +0.2V <sub>ST</sub> | V    |
| Source Impedance                                                |                 | Figure 29<br>Z <sub>S</sub> = V <sub>2</sub> / V <sub>1</sub> x 50Ω | 50                  |      | 150                 | Ω    |
| Short Circuit Impedance                                         |                 | Figure 28                                                           | 135                 |      | 165                 | Ω    |
| <b>V.35 RECEIVERS (ALL VALUES MEASURED WITH TERM_OFF = '0')</b> |                 |                                                                     |                     |      |                     |      |
| Sensitivity                                                     |                 |                                                                     |                     | ±100 | ±200                | mV   |
| Source Impedance                                                |                 | Figure 30<br>Z <sub>S</sub> = V <sub>2</sub> / V <sub>1</sub> x 50Ω | 90                  |      | 110                 | Ω    |
| Short-Circuit Impedance                                         |                 | Figure 31                                                           | 135                 |      | 165                 | Ω    |
| <b>TRANSCEIVER LEAKAGE CURRENT</b>                              |                 |                                                                     |                     |      |                     |      |
| Driver Output Tri-state Current                                 |                 | Drivers disabled, Figure 32                                         |                     | 500  |                     | μA   |
| Receiver Output Tri-state Current                               |                 | Tx and Rx Disabled,<br>0.4V ≤ V <sub>O</sub> ≤ 2.4V                 |                     | 1    | 10                  | μA   |

TABLE 2: AC TIMING CHARACTERISTICS

| TIMING CHARACTERISTICS                                                                                                                             |                      |                                                      |     |     |     |            |
|----------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------------------------------------|-----|-----|-----|------------|
| $V_{CC} = +4.75$ to $5.25V$ , $C1-C4 = 1\mu F$ ; $T_{AMB} = T_{MIN}$ to $T_{MAX}$ , unless noted. Typical values are at $T_{AMB} = +25^{\circ}C$ . |                      |                                                      |     |     |     |            |
| PARAMETERS                                                                                                                                         | SYMBOL               | TEST CONDITIONS                                      | MIN | TYP | MAX | UNIT       |
| <b>V.28 / RS-232 DRIVER</b>                                                                                                                        |                      |                                                      |     |     |     |            |
| Maximum Transmission Rate                                                                                                                          |                      | Figure 7                                             | 250 |     |     | kbps       |
| Driver Propagation Delay                                                                                                                           | $t_{DPLH}, t_{DPLH}$ |                                                      | 0.5 | 1   | 5   | $\mu s$    |
| Driver Transition Time                                                                                                                             |                      | +3V to -3V, Figure 7                                 | 0.2 |     | 1.5 | $\mu s$    |
| Instantaneous Slew Rate                                                                                                                            |                      | +3V to -3V, Figure 4                                 | 4   |     | 30  | V/ $\mu s$ |
| Driver Skew                                                                                                                                        |                      | $ t_{DPLH} - t_{DPLH} $<br>at zero crossing          |     | 100 | 800 | ns         |
| Driver Channel to Channel Skew                                                                                                                     |                      |                                                      |     | 20  |     | ns         |
| Driver Output Enable Time<br>Tri-state to Output Low                                                                                               | $t_{DZL}$            | $C_L = 100$ pF, S1 closed<br>Figure 34 and Figure 40 |     |     | 2   | $\mu s$    |
| Driver Output Enable Time<br>Tri-state to Output High                                                                                              | $t_{DZH}$            | $C_L = 100$ pF, S2 closed<br>Figure 34 and Figure 40 |     |     | 2   | $\mu s$    |
| Driver Output Disable Time<br>Output Low to Tri-state                                                                                              | $t_{DLZ}$            | $C_L = 15$ pF, S1 closed<br>Figure 34 and Figure 40  |     |     | 2   | $\mu s$    |
| Driver Output Disable Time<br>Output High to Tri-state                                                                                             | $t_{DHZ}$            | $C_L = 15$ pF, S2 closed<br>Figure 34 and Figure 40  |     |     | 2   | $\mu s$    |
| <b>V.28 / RS-232 RECEIVER</b>                                                                                                                      |                      |                                                      |     |     |     |            |
| Receiver Propagation Delay                                                                                                                         | $t_{PHL}, t_{PLH}$   | $R_{IN}$ to $R_{OUT}$ , $C_L = 15$ pF                | 50  | 100 | 500 | ns         |
| Receiver Skew                                                                                                                                      |                      | $ t_{PHL} - t_{PLH} $ at 1.5V                        |     | 50  |     | ns         |
| Receiver Channel to Channel Skew                                                                                                                   |                      |                                                      |     | 20  |     | ns         |
| Receiver Output Rise / Fall Time                                                                                                                   | $t_R, t_F$           | $C_L = 15$ pF                                        |     | 15  |     | ns         |
| Receiver Output Enable Time<br>Tri-state to Output Low                                                                                             | $t_{ZL}$             | $C_L = 100$ pF, S1 closed<br>Figure 35 and Figure 40 |     |     | 2   | $\mu s$    |
| Receiver Output Enable Time<br>Tri-state to Output High                                                                                            | $t_{ZH}$             | $C_L = 100$ pF, S2 closed<br>Figure 35 and Figure 40 |     |     | 2   | $\mu s$    |
| Receiver Output Disable Time<br>Output Low to Tri-state                                                                                            | $t_{LZ}$             | $C_L = 15$ pF, S1 closed<br>Figure 35 and Figure 40  |     |     | 2   | $\mu s$    |
| Receiver Output Disable Time<br>Output High to Tri-state                                                                                           | $t_{HZ}$             | $C_L = 15$ pF, S2 closed<br>Figure 35 and Figure 40  |     |     | 2   | $\mu s$    |
| Charge Pump Rise Time                                                                                                                              |                      | Shutdown to operational                              |     |     | 2   | ms         |

**TIMING CHARACTERISTICS**

$V_{CC} = +4.75$  to  $5.25V$ ,  $C1-C4 = 1\mu F$ ;  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ , unless noted. Typical values are at  $T_{AMB} = +25^{\circ}C$ .

| PARAMETERS                                               | SYMBOL               | TEST CONDITIONS                                                                      | MIN | TYP | MAX | UNIT    |
|----------------------------------------------------------|----------------------|--------------------------------------------------------------------------------------|-----|-----|-----|---------|
| <b>V.10 / RS-423 DRIVER</b>                              |                      |                                                                                      |     |     |     |         |
| Maximum Transmission Rate                                |                      |                                                                                      | 250 |     |     | kbps    |
| Driver Propagation Delay                                 | $t_{DPLH}, t_{DPLH}$ |                                                                                      | 30  | 150 | 500 | ns      |
| Driver Rise / Fall Time                                  | $t_{DR}, t_{DF}$     | 10% to 90%, <a href="#">Figure 14</a>                                                |     |     | 500 | ns      |
| Driver Skew                                              |                      | $ t_{DPLH} - t_{DPLH} $<br>at zero crossing                                          |     |     | 100 | ns      |
| Driver Channel to Channel Skew                           |                      |                                                                                      |     | 5   |     | ns      |
| Driver Output Enable Time<br>Tri-state to Output Low     | $t_{DZL}$            | $C_L = 100$ pF, S1 closed<br><a href="#">Figure 34</a> and <a href="#">Figure 40</a> |     |     | 2   | $\mu s$ |
| Driver Output Enable Time<br>Tri-state to Output High    | $t_{DZH}$            | $C_L = 100$ pF, S2 closed<br><a href="#">Figure 34</a> and <a href="#">Figure 40</a> |     |     | 2   | $\mu s$ |
| Driver Output Disable Time<br>Output Low to Tri-state    | $t_{DLZ}$            | $C_L = 15$ pF, S1 closed<br><a href="#">Figure 34</a> and <a href="#">Figure 40</a>  |     |     | 2   | $\mu s$ |
| Driver Output Disable Time<br>Output High to Tri-state   | $t_{DHZ}$            | $C_L = 15$ pF, S2 closed<br><a href="#">Figure 34</a> and <a href="#">Figure 40</a>  |     |     | 2   | $\mu s$ |
| <b>V.10 / RS-423 RECEIVER</b>                            |                      |                                                                                      |     |     |     |         |
| Receiver Propagation Delay                               | $t_{PHL}, t_{PLH}$   |                                                                                      |     | 100 | 500 | ns      |
| Receiver Output Rise / Fall Time                         | $t_R, t_F$           | $C_L = 15$ pF                                                                        |     | 15  |     | ns      |
| Receiver Skew                                            |                      | $ t_{PHL} - t_{PLH} $ at 1.5V                                                        |     | 5   |     | ns      |
| Receiver Channel to Channel Skew                         |                      |                                                                                      |     | 5   |     | ns      |
| Receiver Output Enable Time<br>Tri-state to Output Low   | $t_{ZL}$             | $C_L = 100$ pF, S1 closed<br><a href="#">Figure 35</a> and <a href="#">Figure 40</a> |     |     | 2   | $\mu s$ |
| Receiver Output Enable Time<br>Tri-state to Output High  | $t_{ZH}$             | $C_L = 100$ pF, S2 closed<br><a href="#">Figure 35</a> and <a href="#">Figure 40</a> |     |     | 2   | $\mu s$ |
| Receiver Output Disable Time<br>Output Low to Tri-state  | $t_{LZ}$             | $C_L = 15$ pF, S1 closed<br><a href="#">Figure 35</a> and <a href="#">Figure 40</a>  |     |     | 2   | $\mu s$ |
| Receiver Output Disable Time<br>Output High to Tri-state | $t_{HZ}$             | $C_L = 15$ pF, S2 closed<br><a href="#">Figure 35</a> and <a href="#">Figure 40</a>  |     |     | 2   | $\mu s$ |

**TIMING CHARACTERISTICS**

$V_{CC} = +4.75$  to  $5.25V$ ,  $C_1$ - $C_4 = 1\mu F$ ;  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ , unless noted. Typical values are at  $T_{AMB} = +25^{\circ}C$ .

| PARAMETERS                                               | SYMBOL               | TEST CONDITIONS                                                  | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------|----------------------|------------------------------------------------------------------|-----|-----|-----|------|
| <b>HIGH SPEED V.11 / RS-422 (DRIVERS 1, 2 &amp; 3)</b>   |                      |                                                                  |     |     |     |      |
| Maximum Bit Rate                                         |                      |                                                                  | 52  |     |     | Mbps |
| Driver Rise and Fall Time                                | $t_{DR}, t_{DF}$     | 10-90%<br>Figure 22 and Figure 36                                |     |     | 6   | ns   |
| Driver Propagation Delay Time                            | $t_{DPLH}, t_{DPLH}$ | $C_L = 50$ pF<br>Figure 33 and Figure 36                         |     | 20  | 50  | ns   |
| Driver Skew                                              |                      | $ t_{DPLH} - t_{DPLH} $ $C_L = 50$ pF<br>Figure 33 and Figure 36 |     |     | 3.8 | ns   |
| Driver Channel to Channel Skew                           |                      |                                                                  |     | 2   |     | ns   |
| Driver Output Enable Time<br>Tri-state to Output Low     | $t_{DZL}$            | $C_L = 100$ pF, S1 closed<br>Figure 34 and Figure 37             |     |     | 100 | ns   |
| Driver Output Enable Time<br>Tri-state to Output High    | $t_{DZH}$            | $C_L = 100$ pF, S2 closed<br>Figure 34 and Figure 37             |     |     | 100 | ns   |
| Driver Output Disable Time<br>Output Low to Tri-state    | $t_{DLZ}$            | $C_L = 15$ pF, S1 closed<br>Figure 34 and Figure 37              |     |     | 100 | ns   |
| Driver Output Disable Time<br>Output High to Tri-state   | $t_{DHZ}$            | $C_L = 15$ pF, S2 closed<br>Figure 34 and Figure 37              |     |     | 100 | ns   |
| <b>HIGH SPEED V.11 / RS-422 (RECEIVERS 1, 2 &amp; 3)</b> |                      |                                                                  |     |     |     |      |
| Receiver Output Rise / Fall Time                         | $t_R, t_F$           | $C_L = 50$ pF                                                    |     |     | 6   | ns   |
| Receiver Propagation Delay                               | $t_{PHL}, t_{PLH}$   | $C_L = 50$ pF<br>Figure 33 and Figure 38                         |     | 20  | 50  | ns   |
| Receiver Skew                                            |                      | $ t_{PHL} - t_{PLH} $ $C_L = 50$ pF<br>Figure 33 and Figure 38   |     |     | 3.8 | ns   |
| Receiver Channel to Channel Skew                         |                      |                                                                  |     | 2   |     | ns   |
| Receiver Output Enable Time<br>Tri-state to Output Low   | $t_{ZL}$             | $C_L = 100$ pF, S1 closed<br>Figure 35 and Figure 39             |     |     | 100 | ns   |
| Receiver Output Enable Time<br>Tri-state to Output High  | $t_{ZH}$             | $C_L = 100$ pF, S2 closed<br>Figure 35 and Figure 39             |     |     | 100 | ns   |
| Receiver Output Disable Time<br>Output Low to Tri-state  | $t_{LZ}$             | $C_L = 15$ pF, S1 closed<br>Figure 35 and Figure 39              |     |     | 100 | ns   |
| Receiver Output Disable Time<br>Output High to Tri-state | $t_{HZ}$             | $C_L = 15$ pF, S2 closed<br>Figure 35 and Figure 39              |     |     | 100 | ns   |

**TIMING CHARACTERISTICS**

$V_{CC} = +4.75$  to  $5.25V$ ,  $C1-C4 = 1\mu F$ ;  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ , unless noted. Typical values are at  $T_{AMB} = +25^{\circ}C$ .

| PARAMETERS                                                      | SYMBOL               | TEST CONDITIONS                                                    | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------------|----------------------|--------------------------------------------------------------------|-----|-----|-----|------|
| <b>V.11 / RS-422 HANDSHAKE SIGNALS (DRIVERS 4, 5 &amp; 6)</b>   |                      |                                                                    |     |     |     |      |
| Maximum Bit Rate                                                |                      | Figure 33                                                          | 10  |     |     | Mbps |
| Driver Rise and Fall Time                                       | $t_{DR}, t_{DF}$     | Figure 22 and Figure 36                                            |     | 2   | 10  | ns   |
| Driver Propagation Delay Time                                   | $t_{DPLH}, t_{DPLH}$ | $C_L = 50$ pF<br>Figure 33 and Figure 36                           |     | 20  | 50  | ns   |
| Driver Skew                                                     |                      | $ t_{DPLH} - t_{DPLH} $ , $C_L = 50$ pF<br>Figure 33 and Figure 36 |     |     | 10  | ns   |
| Driver Channel to Channel Skew                                  |                      |                                                                    |     | 2   |     | ns   |
| Driver Output Enable Time<br>Tri-state to Output Low            | $t_{DZL}$            | $C_L = 100$ pF, S1 closed<br>Figure 34 and Figure 37               |     |     | 100 | ns   |
| Driver Output Enable Time<br>Tri-state to Output High           | $t_{DZH}$            | $C_L = 100$ pF, S2 closed<br>Figure 34 and Figure 37               |     |     | 100 | ns   |
| Driver Output Disable Time<br>Output Low to Tri-state           | $t_{DLZ}$            | $C_L = 15$ pF, S1 closed<br>Figure 34 and Figure 37                |     |     | 100 | ns   |
| Driver Output Disable Time<br>Output High to Tri-state          | $t_{DHZ}$            | $C_L = 15$ pF, S2 closed<br>Figure 34 and Figure 37                |     |     | 100 | ns   |
| <b>V.11 / RS-422 HANDSHAKE SIGNALS (RECEIVERS 4, 5 &amp; 6)</b> |                      |                                                                    |     |     |     |      |
| Receiver Output Rise / Fall Time                                | $t_R, t_F$           | $C_L = 50$ pF                                                      |     |     | 20  | ns   |
| Receiver Propagation Delay                                      | $t_{PHL}, t_{PLH}$   | $C_L = 50$ pF<br>Figure 33 and Figure 38                           |     | 20  | 50  | ns   |
| Receiver Skew                                                   |                      | $ t_{PHL} - t_{PLH} $ $C_L = 50$ pF<br>Figure 33 and Figure 38     |     |     | 10  | ns   |
| Receiver Channel to Channel Skew                                |                      |                                                                    |     | 2   |     | ns   |
| Receiver Output Enable Time<br>Tri-state to Output Low          | $t_{ZL}$             | $C_L = 100$ pF, S1 closed<br>Figure 35 and Figure 39               |     |     | 100 | ns   |
| Receiver Output Enable Time<br>Tri-state to Output High         | $t_{ZH}$             | $C_L = 100$ pF, S2 closed<br>Figure 35 and Figure 39               |     |     | 100 | ns   |
| Receiver Output Disable Time<br>Output Low to Tri-state         | $t_{LZ}$             | $C_L = 15$ pF, S1 closed<br>Figure 35 and Figure 39                |     |     | 100 | ns   |
| Receiver Output Disable Time<br>Output High to Tri-state        | $t_{HZ}$             | $C_L = 15$ pF, S2 closed<br>Figure 35 and Figure 39                |     |     | 100 | ns   |

**TIMING CHARACTERISTICS**

$V_{CC} = +4.75$  to  $5.25V$ ,  $C1-C4 = 1\mu F$ ;  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ , unless noted. Typical values are at  $T_{AMB} = +25^{\circ}C$ .

| PARAMETERS                                               | SYMBOL               | TEST CONDITIONS                                                  | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------|----------------------|------------------------------------------------------------------|-----|-----|-----|------|
| <b>V.35 (DRIVERS 1, 2 &amp; 3)</b>                       |                      |                                                                  |     |     |     |      |
| Maximum Bit Rate                                         |                      | $f_{MAX} = 20$ MHz, Figure 33                                    | 40  |     |     | Mbps |
| Driver Rise and Fall Time                                | $t_{DR}, t_{DF}$     | Figure 29                                                        |     |     | 10  | ns   |
| Driver Propagation Delay Time                            | $t_{DPLH}, t_{DPLH}$ | $C_L = 50$ pF<br>Figure 33 and Figure 36                         |     | 25  | 50  | ns   |
| Driver Skew                                              |                      | $ t_{DPLH} - t_{DPLH} $ $C_L = 50$ pF<br>Figure 33 and Figure 36 |     | 2   | 5   | ns   |
| Driver Channel to Channel Skew                           |                      |                                                                  |     | 2   |     | ns   |
| Driver Output Enable Time<br>Tri-state to Output Low     | $t_{DZL}$            | $C_L = 100$ pF, S1 closed<br>Figure 34 and Figure 37             |     |     | 200 | ns   |
| Driver Output Enable Time<br>Tri-state to Output High    | $t_{DZH}$            | $C_L = 100$ pF, S2 closed<br>Figure 34 and Figure 37             |     |     | 200 | ns   |
| Driver Output Disable Time<br>Output Low to Tri-state    | $t_{DLZ}$            | $C_L = 15$ pF, S1 closed<br>Figure 34 and Figure 37              |     |     | 200 | ns   |
| Driver Output Disable Time<br>Output High to Tri-state   | $t_{DHZ}$            | $C_L = 15$ pF, S2 closed<br>Figure 34 and Figure 37              |     |     | 200 | ns   |
| <b>V.35 (RECEIVERS 1, 2 &amp; 3)</b>                     |                      |                                                                  |     |     |     |      |
| Receiver Propagation Delay                               | $t_{PHL}, t_{PLH}$   | $C_L = 50$ pF<br>Figure 33 and Figure 38                         |     | 30  | 50  | ns   |
| Receiver Skew                                            |                      | $ t_{PHL} - t_{PLH} $ $C_L = 50$ pF<br>Figure 33 and Figure 38   |     |     | 5   | ns   |
| Receiver Channel to Channel Skew                         |                      |                                                                  |     | 2   |     | ns   |
| Receiver Output Enable Time<br>Tri-state to Output Low   | $t_{ZL}$             | $C_L = 100$ pF, S1 closed<br>Figure 35 and Figure 39             |     |     | 200 | ns   |
| Receiver Output Enable Time<br>Tri-state to Output High  | $t_{ZH}$             | $C_L = 100$ pF, S2 closed<br>Figure 35 and Figure 39             |     |     | 200 | ns   |
| Receiver Output Disable Time<br>Output Low to Tri-state  | $t_{LZ}$             | $C_L = 15$ pF, S1 closed<br>Figure 35 and Figure 39              |     |     | 200 | ns   |
| Receiver Output Disable Time<br>Output High to Tri-state | $t_{HZ}$             | $C_L = 15$ pF, S2 closed<br>Figure 35 and Figure 39              |     |     | 200 | ns   |

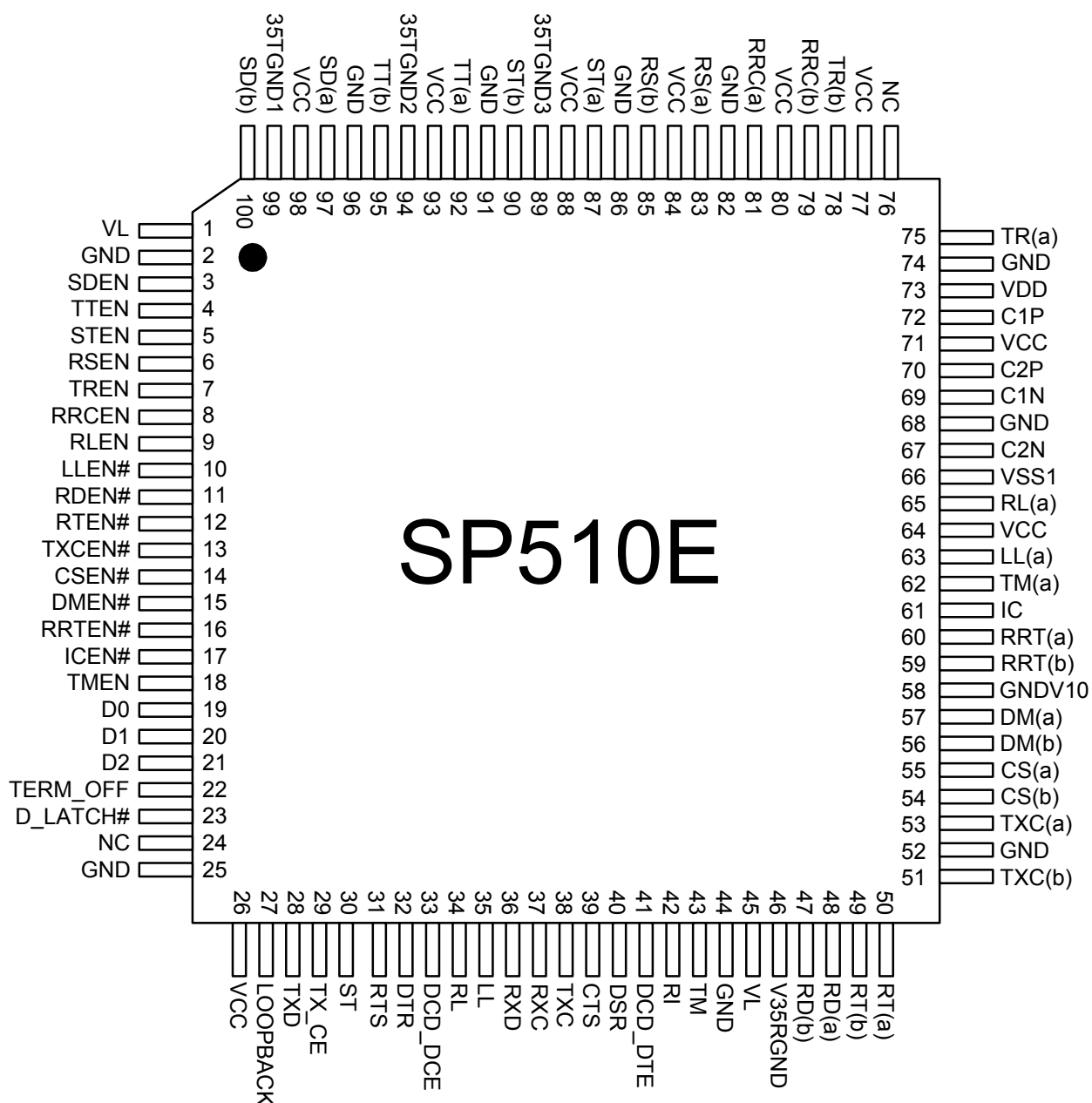
**FIGURE 1. PIN OUT DIAGRAM**


TABLE 3: PIN DESCRIPTIONS BY FUNCTION

| PIN NAME                    | PIN NUMBER | I/O |     | DESCRIPTION                                                            |
|-----------------------------|------------|-----|-----|------------------------------------------------------------------------|
| <b>DIFFERENTIAL DRIVERS</b> |            |     |     |                                                                        |
| TxD                         | 28         | I   | TTL | TxD Driver Input                                                       |
| SD(b) / SD(a)               | 100, 97    | O   | TTL | Differential Transmit data non-inverting (b) and inverting (a) outputs |
| V35TGND1                    | 99         | I   |     | SD Termination Reference                                               |
| SDEN                        | 3          | I   | TTL | TxD Driver Enable                                                      |
| TxCE                        | 29         | I   | TTL | TxCE Driver Input                                                      |
| TT(b) / TT(a)               | 95, 92     | O   | TTL | Differential TxCE non-inverting (b) and inverting (a) outputs          |
| V35TGND2                    | 94         | I   |     | TT Termination Reference                                               |
| TTEN                        | 4          | I   | TTL | TxCE Driver Enable                                                     |
| ST                          | 30         | I   | TTL | ST Driver Input                                                        |
| ST(b) / ST(a)               | 90, 87     | O   | TTL | Differential ST non-inverting (b) and inverting (a) outputs            |
| V35TGND3                    | 89         | I   |     | ST Termination Reference                                               |
| STEN                        | 5          | I   | TTL | ST Driver Enable                                                       |
| RTS                         | 31         | I   | TTL | RTS Driver Input                                                       |
| RS(b) / RS(a)               | 85, 83     | O   | TTL | Differential RTS non-inverting (b) and inverting (a) outputs           |
| RSEN                        | 6          | I   | TTL | RTS Driver Enable                                                      |
| DTR                         | 32         | I   | TTL | DTR Driver Input                                                       |
| TR(b) / TR(a)               | 78, 75     | O   | TTL | Differential DTR non-inverting (b) and inverting (a) outputs           |
| TREN                        | 7          | I   | TTL | DTR Driver Enable                                                      |
| DCD_DCE                     | 33         | I   | TTL | DCD_DCE Driver Input                                                   |
| RRC(b) / RRC(a)             | 79, 81     | O   | TTL | Differential DCD non-inverting (b) and inverting (a) outputs           |
| RRCEN                       | 8          | I   | TTL | DCD Driver Enable                                                      |
| <b>SINGLE ENDED DRIVERS</b> |            |     |     |                                                                        |
| RL                          | 34         | I   | TTL | RL Driver Input                                                        |
| RL(a)                       | 65         | O   | TTL | RL Driver Output                                                       |
| RLEN                        | 9          | I   | TTL | RL Driver Enable                                                       |
| LL                          | 35         | I   | TTL | LL Driver Input                                                        |
| LL(a)                       | 63         | O   | TTL | LL Driver Output                                                       |
| LLEN#                       | 10         | I   | TTL | LL Driver Enable, active low                                           |

| PIN NAME                      | PIN NUMBER | I/O |     | DESCRIPTION                                                     |
|-------------------------------|------------|-----|-----|-----------------------------------------------------------------|
| <b>DIFFERENTIAL RECEIVERS</b> |            |     |     |                                                                 |
| RxD                           | 36         | O   | TTL | RxD Receiver Output                                             |
| RD(b) / RD(a)                 | 47, 48     | I   | TTL | Differential RXD non-inverting (b) and inverting (a) inputs     |
| RDEN#                         | 11         | I   | TTL | RxD Receiver Enable, active low                                 |
| RxC                           | 37         | O   | TTL | RxC Receiver Output                                             |
| RT(b) / RT(a)                 | 49, 50     | I   | TTL | Differential RXC non-inverting (b) and inverting (a) inputs     |
| RTEN#                         | 12         | I   | TTL | RxC Receiver Enable, active low                                 |
| TxC                           | 38         | O   | TTL | TxC Receiver Output                                             |
| TxC(b) / TxC(a)               | 51, 53     | I   | TTL | Differential TxC non-inverting (b) and inverting (a) inputs     |
| TxCEN#                        | 13         | I   | TTL | TxC Receiver Enable, active low                                 |
| CTS                           | 39         | O   | TTL | CTS Receiver Output                                             |
| CS(b) / CS(a)                 | 54, 55     | I   | TTL | Differential CTS non-inverting (b) and inverting (a) inputs     |
| CSEN#                         | 14         | I   | TTL | CTS Receiver Enable, active low                                 |
| DSR                           | 40         | O   | TTL | DSR Receiver Output                                             |
| DM(b) / DM(a)                 | 56, 57     | I   | TTL | Differential DSR non-inverting (b) and inverting (a) inputs     |
| DMEN#                         | 15         | I   | TTL | DSR Receiver Enable, active low                                 |
| DCD_DTE                       | 41         | O   | TTL | DCD_DTE Receiver Output                                         |
| RRT(b) / RRT(a)               | 59, 60     | I   | TTL | Differential DCD_DTE non-inverting (b) and inverting (a) inputs |
| RRTEN#                        | 16         | I   | TTL | DCD_DTE Receiver Enable, active low                             |
| <b>SINGLE ENDED RECEIVERS</b> |            |     |     |                                                                 |
| IC                            | 61         | I   | TTL | RI Receiver Input                                               |
| RI                            | 42         | O   | TTL | RI Receiver Output                                              |
| ICEN#                         | 17         | I   | TTL | RI Receiver Enable, active low                                  |
| TM(a)                         | 62         | I   | TTL | TM Receiver Input                                               |
| TM                            | 43         | O   | TTL | TM Receiver Output                                              |
| TMEN                          | 18         | I   | TTL | TM Receiver Enable                                              |

| PIN NAME                       | PIN NUMBER                            | I/O |     | DESCRIPTION                                                                            |
|--------------------------------|---------------------------------------|-----|-----|----------------------------------------------------------------------------------------|
| PROTOCOL & MODE SELECTION PINS |                                       |     |     |                                                                                        |
| D2, D1, D0                     | 21, 20, 19                            | I   | TTL | Mode Select - Refer to <a href="#">Table 5</a> and <a href="#">Table 6</a>             |
| CHARGE PUMP PINS               |                                       |     |     |                                                                                        |
| C1P, C1N                       | 72, 69                                | I   |     | Charge Pump Capacitor 1 +/- inputs. Connect a 1 μF capacitor between C1P and C1N pins. |
| C2P, C2N                       | 70, 67                                | I   |     | Charge Pump Capacitor 2 +/- inputs. Connect a 1 μF capacitor between C2P and C2N pins. |
| VSS1                           | 66                                    | I   |     | -2xV <sub>CC</sub> Charge Pump                                                         |
| VDD                            | 73                                    | I   |     | 2xV <sub>CC</sub> Charge Pump                                                          |
| GENERAL CONTROL PINS           |                                       |     |     |                                                                                        |
| LOOPBACK#                      | 27                                    | I   | TTL | Loopback mode enable, active low                                                       |
| D_LATCH#                       | 23                                    | I   |     | Decoder Latch, active low                                                              |
| TERM_OFF                       | 22                                    | I   |     | Termination disable                                                                    |
| RESERVED PINS                  |                                       |     |     |                                                                                        |
| NC                             | 24, 76                                |     |     | No Connect                                                                             |
| POWER AND GROUND PINS          |                                       |     |     |                                                                                        |
| VCC                            | 26, 64, 71, 77, 80, 84, 88, 98        | I   |     | 5V supply                                                                              |
| VL                             | 1, 45                                 | I   |     | Logic I/O Power Supply Input                                                           |
| GND                            | 2, 25, 44, 52, 68, 74, 82, 86, 91, 96 | I   |     | Ground                                                                                 |
| GNDV10                         | 58                                    | I   |     | V.10 Receiver Ground Reference                                                         |
| V35RGND                        | 46                                    | O   |     | Receiver Termination Reference                                                         |

**NOTE:** Pin type: I = Input, O = Output, I/O = Input/output.

**TABLE 4: PIN DESCRIPTIONS BY PIN NUMBER**

| <b>PIN DESCRIPTIONS BY PIN NUMBER</b> |            |                               |    |         |                                |
|---------------------------------------|------------|-------------------------------|----|---------|--------------------------------|
| 1                                     | VL         | Logic I/O Power Supply Input  | 32 | DTR     | DTR Driver TTL Input           |
| 2                                     | GND        | Ground                        | 33 | DCD_DCE | DCD_DCE Driver TTL Input       |
| 3                                     | SDEN       | TxD Driver Enable Input       | 34 | RL      | RL Driver TTL Input            |
| 4                                     | TTEN       | TxCE Driver Enable Input      | 35 | LL      | LL Driver TTL Input            |
| 5                                     | STEN       | ST Driver Enable Input        | 36 | RxD     | RxD Receiver TTL Output        |
| 6                                     | RSEN       | RTS Driver Enable Input       | 37 | RxC     | RxC Receiver TTL Output        |
| 7                                     | TREN       | DTR Driver Enable Input       | 38 | TxC     | TxC Receiver TTL Output        |
| 8                                     | RRCEN      | DCD Driver Enable Input       | 39 | CTS     | CTS Receiver TTL Output        |
| 9                                     | RLEN       | RL Driver Enable Input        | 40 | DSR     | DSR Receiver TTL Output        |
| 10                                    | LLEN#      | LL Driver Enable Input        | 41 | DCD_DTE | DCD_DTE Receiver TTL Output    |
| 11                                    | RDEN#      | RxD Receiver Enable Input     | 42 | RI      | RI Receiver TTL Output         |
| 12                                    | RTEN#      | RxC Receiver Enable Input     | 43 | TM      | TM Receiver TTL Output         |
| 13                                    | TxCEN#     | TxC Receiver Enable Input     | 44 | GND     | Ground                         |
| 14                                    | CSEN#      | CTS Receiver Enable Input     | 45 | VL      | Logic I/O Power Supply Input   |
| 15                                    | DMEN#      | DSR Receiver Enable Input     | 46 | V35RGND | Receiver Termination Reference |
| 16                                    | RRTEN#     | DCD_DTE Receiver Enable Input | 47 | RD(b)   | RXD Non-Inverting Input        |
| 17                                    | ICEN#      | RI Receiver Enable Input      | 48 | RD(a)   | RXD Inverting Input            |
| 18                                    | TMEN       | TM Receiver Enable Input      | 49 | RT(b)   | RxC Non-Inverting Input        |
| 19                                    | D0         | Mode Select Input - Bit 0     | 50 | RT(a)   | RxC Inverting Input            |
| 20                                    | D1         | Mode Select Input - Bit 1     | 51 | TxC(b)  | TxC Non-Inverting Input        |
| 21                                    | D2         | Mode Select Input - Bit 2     | 52 | GND     | Ground                         |
| 22                                    | TERM_OFF   | Termination Disable Input     | 53 | TxC(a)  | TxC Inverting Input            |
| 23                                    | D_LATCH#   | Decoder Latch Input           | 54 | CS(b)   | CTS Non-Inverting Input        |
| 24                                    | N/C        | No Connect                    | 55 | CS(a)   | CTS Inverting Input            |
| 25                                    | GND        | Ground                        | 56 | DM(b)   | DSR Non-Inverting Input        |
| 26                                    | VCC        | 5V Power Supply Input         | 57 | DM(a)   | DSR Inverting Input            |
| 27                                    | LOOP-BACK# | Loopback Mode Enable Input    | 58 | GNDV10  | V.10 Rx Ground Reference       |
| 28                                    | TxD        | TxD Driver TTL Input          | 59 | RRT(b)  | DCD_DTE Non-Inverting Input    |
| 29                                    | TxCE       | TxCE Driver TTL Input         | 60 | RRT(a)  | DCD_DTE Inverting Input        |
| 30                                    | ST         | ST Driver TTL Input           | 61 | IC      | RI Receiver Input              |
| 31                                    | RTS        | RTS Driver TTL Input          | 62 | TM(a)   | TM Receiver Input              |

| PIN DESCRIPTIONS BY PIN NUMBER |        |                                  |     |          |                           |
|--------------------------------|--------|----------------------------------|-----|----------|---------------------------|
| 63                             | LL(a)  | LL Driver Output                 | 82  | GND      | Ground                    |
| 64                             | VCC    | 5V Power Supply Input            | 83  | RS(a)    | RTS Inverting Output      |
| 65                             | RL(a)  | RL Driver Output                 | 84  | VCC      | 5V Power Supply Input     |
| 66                             | VSS1   | -2 x V <sub>CC</sub> Charge Pump | 85  | RS(b)    | RTS Non-Inverting Output  |
| 67                             | C2N    | Charge Pump Capacitor            | 86  | GND      | Ground                    |
| 68                             | GND    | Ground                           | 87  | ST(a)    | ST Inverting Output       |
| 69                             | C1N    | Charge Pump Capacitor            | 88  | VCC      | 5V Power Supply Input     |
| 70                             | C2P    | Charge Pump Capacitor            | 89  | V35TGND3 | ST Termination Reference  |
| 71                             | VCC    | 5V Power Supply Input            | 90  | ST(b)    | ST Non-Inverting Output   |
| 72                             | C1P    | Charge Pump Capacitor            | 91  | GND      | Ground                    |
| 73                             | VDD    | 2 x V <sub>CC</sub> Charge Pump  | 92  | TT(a)    | TxCE Inverting Output     |
| 74                             | GND    | Ground                           | 93  | VCC      | 5V Power Supply Input     |
| 75                             | TR(a)  | DTR Inverting Output             | 94  | V35TGND2 | TT Termination Reference  |
| 76                             | NC     | No Connect                       | 95  | TT(b)    | TxCE Non-Inverting Output |
| 77                             | VCC    | 5V Power Supply Input            | 96  | GND      | Ground                    |
| 78                             | TR(b)  | DTR Non-Inverting Output         | 97  | SD(a)    | TxD Inverting Output      |
| 79                             | RRC(b) | DCD Non-Inverting Output         | 98  | VCC      | 5V Power Supply Input     |
| 80                             | VCC    | 5V Power Supply Input            | 99  | V35TGND1 | SD Termination Reference  |
| 81                             | RRC(a) | DCD Inverting Output             | 100 | SD(b)    | TxD Non-Inverting Output  |

TABLE 5: DRIVER MODE SELECTION

| DRIVER OUTPUT PIN     | V.35<br>MODE | EIA-530<br>MODE | RS-232<br>MODE<br>(V.28) | EIA-530A<br>MODE | RS-449<br>MODE<br>(V.36) | X.21<br>MODE<br>(V.11) | SHUT-<br>DOWN | SUGGESTED<br>SIGNAL |
|-----------------------|--------------|-----------------|--------------------------|------------------|--------------------------|------------------------|---------------|---------------------|
| MODE (D2, D1, D0)     | 001          | 010             | 011                      | 100              | 101                      | 110                    | 111           |                     |
| T <sub>1</sub> OUT(a) | V.35         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | TxD(a)              |
| T <sub>1</sub> OUT(b) | V.35         | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | TxD(b)              |
| T <sub>2</sub> OUT(a) | V.35         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | TxCE(a)             |
| T <sub>2</sub> OUT(b) | V.35         | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | TxCE(b)             |
| T <sub>3</sub> OUT(a) | V.35         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | TxC_DCE(a)          |
| T <sub>3</sub> OUT(b) | V.35         | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | TxC_DCE(b)          |
| T <sub>4</sub> OUT(a) | V.28         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | RTS(a)              |
| T <sub>4</sub> OUT(b) | High-Z       | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | RTS(b)              |
| T <sub>5</sub> OUT(a) | V.28         | V.11            | V.28                     | V.10             | V.11                     | V.11                   | High-Z        | DTR(a)              |
| T <sub>5</sub> OUT(b) | High-Z       | V.11            | High-Z                   | High-Z           | V.11                     | V.11                   | High-Z        | DTR(b)              |
| T <sub>6</sub> OUT(a) | V.28         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | DCD_DCE(a)          |
| T <sub>6</sub> OUT(b) | High-Z       | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | DCD_DCE(b)          |
| T <sub>7</sub> OUT(a) | V.28         | V.10            | V.28                     | V.10             | V.10                     | High-Z                 | High-Z        | RL                  |
| T <sub>8</sub> OUT(a) | V.28         | V.10            | V.28                     | V.10             | V.10                     | High-Z                 | High-Z        | LL                  |

TABLE 6: RECEIVER MODE SELECTION

| RECEIVER INPUT PIN   | V.35<br>MODE | EIA-530<br>MODE | RS-232<br>MODE<br>(V.28) | EIA-530A<br>MODE | RS-449<br>MODE<br>(V.36) | X.21<br>MODE<br>(V.11) | SHUT-<br>DOWN | SUGGESTED<br>SIGNAL |
|----------------------|--------------|-----------------|--------------------------|------------------|--------------------------|------------------------|---------------|---------------------|
| MODE (D2, D1, D0)    | 001          | 010             | 011                      | 100              | 101                      | 110                    | 111           |                     |
| R <sub>1</sub> IN(a) | V.35         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | RxD(a)              |
| R <sub>1</sub> IN(b) | V.35         | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | RxD(b)              |
| R <sub>2</sub> IN(a) | V.35         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | RxCE(a)             |
| R <sub>2</sub> IN(b) | V.35         | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | RxCE(b)             |
| R <sub>3</sub> IN(a) | V.35         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | TxC_DTE(a)          |
| R <sub>3</sub> IN(b) | V.35         | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | TxC_DTE(b)          |
| R <sub>4</sub> IN(a) | V.28         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | CTS(a)              |
| R <sub>4</sub> IN(b) | High-Z       | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | CTS(b)              |
| R <sub>5</sub> IN(a) | V.28         | V.11            | V.28                     | V.10             | V.11                     | V.11                   | High-Z        | DSR(a)              |
| R <sub>5</sub> IN(b) | High-Z       | V.11            | High-Z                   | High-Z           | V.11                     | V.11                   | High-Z        | DSR(b)              |
| R <sub>6</sub> IN(a) | V.28         | V.11            | V.28                     | V.11             | V.11                     | V.11                   | High-Z        | DCD_DTE(a)          |
| R <sub>6</sub> IN(b) | High-Z       | V.11            | High-Z                   | V.11             | V.11                     | V.11                   | High-Z        | DCD_DTE(b)          |
| R <sub>7</sub> IN(a) | V.28         | V.10            | V.28                     | V.10             | V.10                     | High-Z                 | High-Z        | RI                  |
| R <sub>8</sub> IN(a) | V.28         | V.10            | V.28                     | V.10             | V.10                     | High-Z                 | High-Z        | TM                  |

**TABLE 7: V.11 & V.35 DRIVERS**

| INPUTS |       | OUTPUTS |       |
|--------|-------|---------|-------|
| Tx_EN# | Tx_IN | Tx(A)   | Tx(B) |
| 1      | 1     | 0       | 1     |
| 1      | 0     | 1       | 0     |

**TABLE 8: V.28 DRIVERS**

| INPUTS |       | OUTPUTS |                 |
|--------|-------|---------|-----------------|
| Tx_EN# | Tx_IN | Tx(A)   | Tx(B)           |
| 1      | 1     | < -5V   | > 30 k $\Omega$ |
| 1      | 0     | > +5V   | > 30 k $\Omega$ |

**TABLE 9: V.10 DRIVERS**

| INPUTS |       | OUTPUTS |                 |
|--------|-------|---------|-----------------|
| Tx_EN# | Tx_IN | Tx(A)   | Tx(B)           |
| 1      | 1     | < -4V   | > 30 k $\Omega$ |
| 1      | 0     | > +4V   | > 30 k $\Omega$ |

**TABLE 10: V.11 & V.35 RECEIVERS**

| INPUTS         | OUTPUTS |
|----------------|---------|
| Rx(A) - Rx(B)  | RO      |
| $\geq 200$ mV  | 1       |
| $\leq -200$ mV | 0       |
| Open / shorted | 1       |

**TABLE 11: V.28 RECEIVERS**

| INPUTS        | OUTPUTS |
|---------------|---------|
| Rx(A) - Rx(B) | RO      |
| $\geq +3$ V   | 0       |
| $\leq -3$ V   | 1       |
| Open / ground | 1       |

**TABLE 12: V.10 RECEIVERS**

| INPUTS        | OUTPUTS |
|---------------|---------|
| Rx(A) - Rx(B) | RO      |
| $\geq +0.3$ V | 0       |
| $\leq -0.3$ V | 1       |
| Open / ground | 1       |

FIGURE 2. V.28 DRIVER OUTPUT OPEN CIRCUIT VOLTAGE

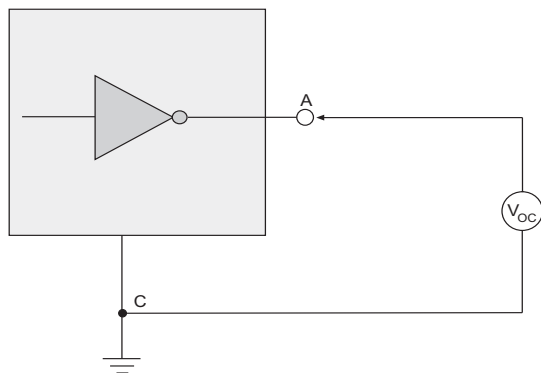


FIGURE 3. V.28 DRIVER OUTPUT LOADED VOLTAGE

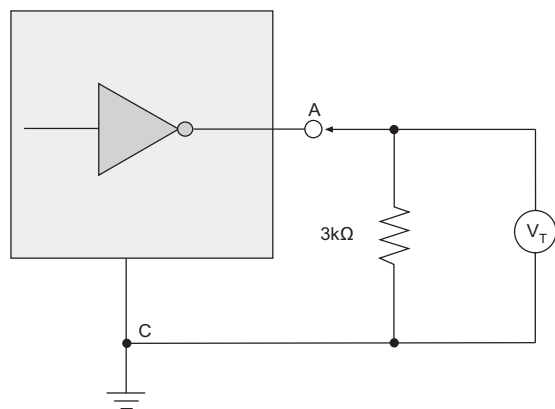


FIGURE 4. V.28 DRIVER OUTPUT SLEW RATE

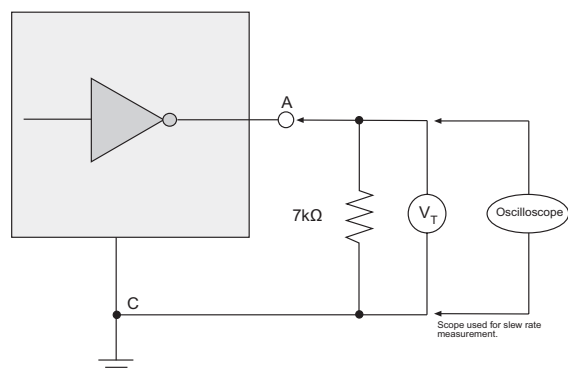


FIGURE 5. V.28 DRIVER OUTPUT SHORT CIRCUIT CURRENT

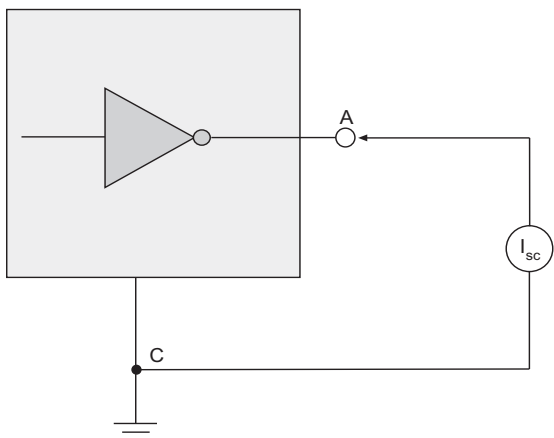


FIGURE 6. V.28 DRIVER OUTPUT POWER-OFF IMPEDANCE

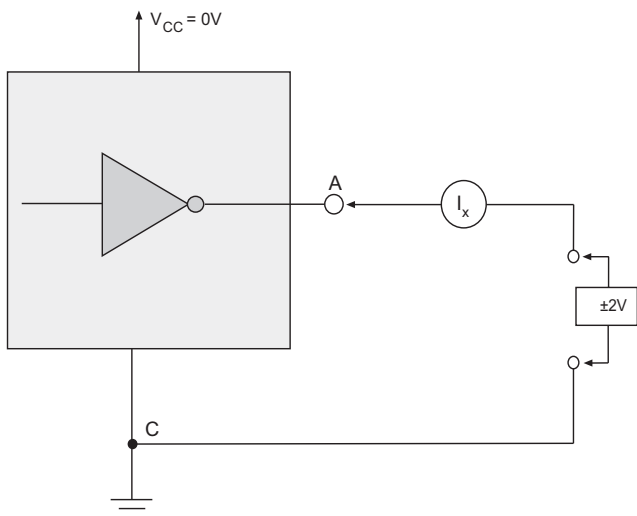


FIGURE 7. V.28 DRIVER OUTPUT RISE/FALL TIME

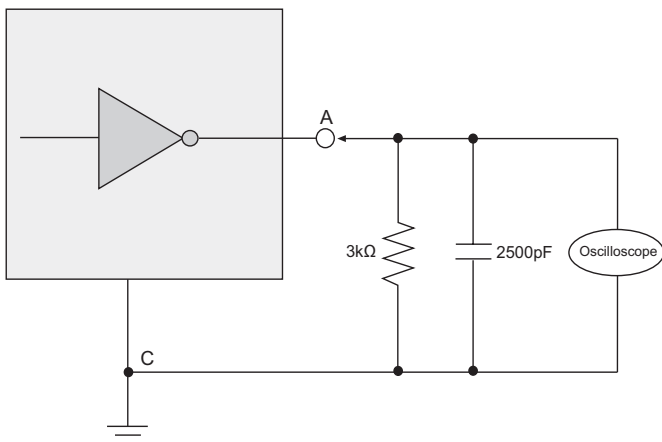


FIGURE 8. V.28 RECEIVER INPUT IMPEDANCE

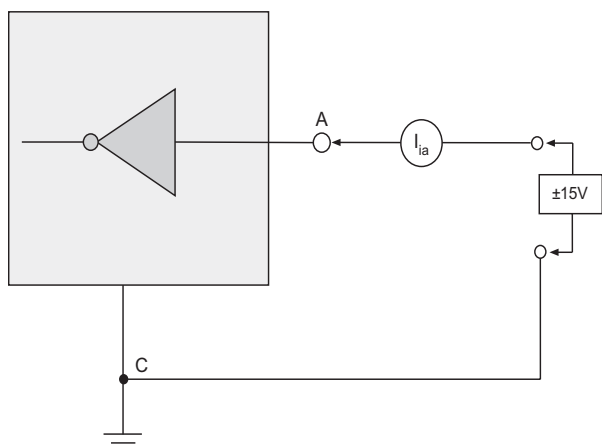


FIGURE 9. V.28 RECEIVER INPUT OPEN-CIRCUIT BIAS

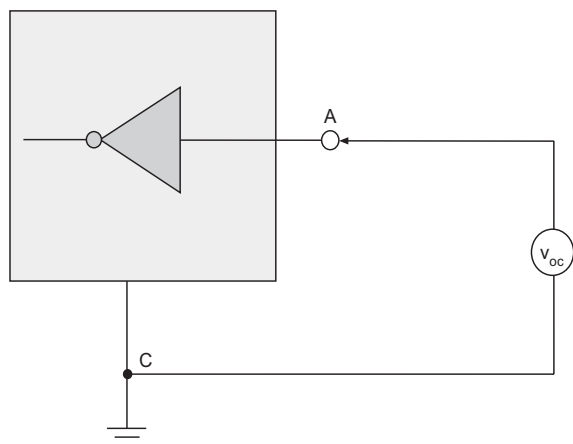


FIGURE 10. V.10 DRIVER OUTPUT OPEN-CIRCUIT VOLTAGE

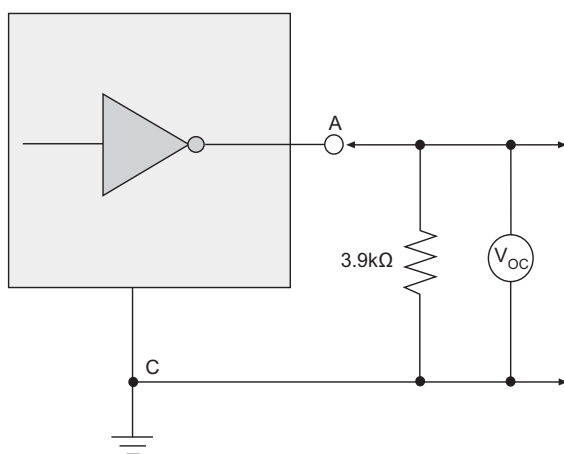


FIGURE 11. V.10 DRIVER OUTPUT TEST TERMINATED VOLTAGE

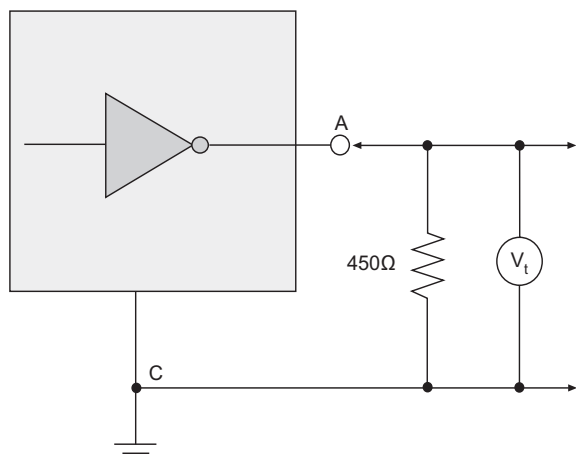


FIGURE 12. V.10 DRIVER OUTPUT SHORT-CIRCUIT CURRENT

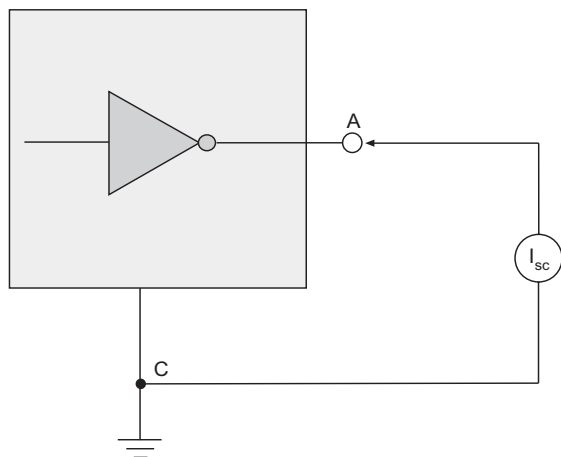


FIGURE 13. V.10 DRIVER OUTPUT POWER-OFF IMPEDANCE

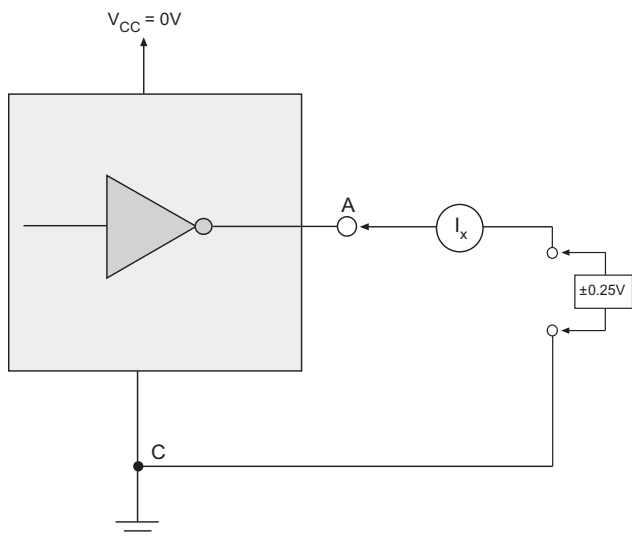


FIGURE 14. V.10 DRIVER OUTPUT TRANSITION TIME

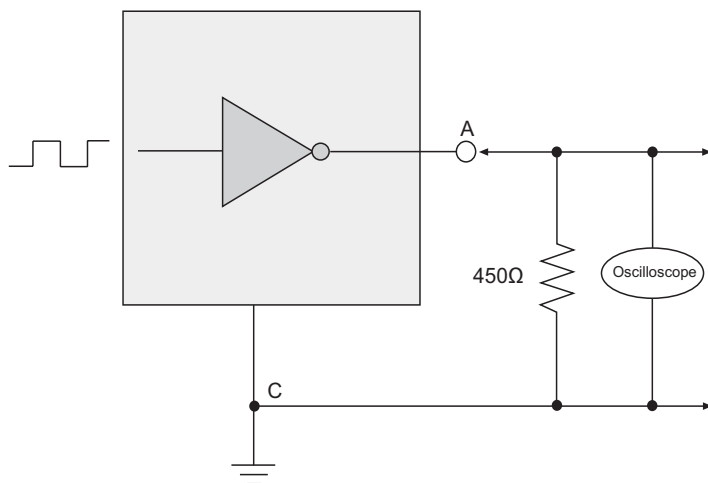


FIGURE 15. V.10 RECEIVER INPUT CURRENT

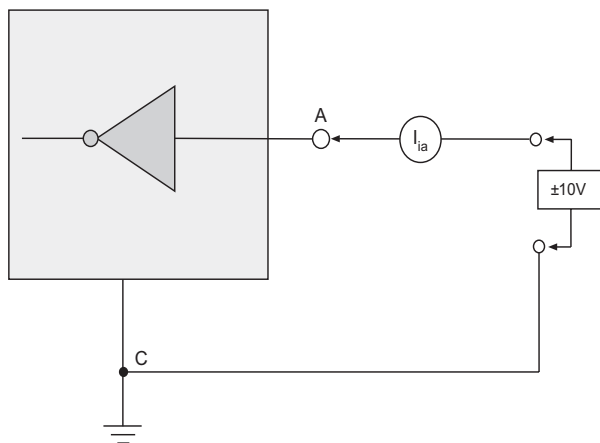


FIGURE 16. V.10 RECEIVER INPUT IV GRAPH

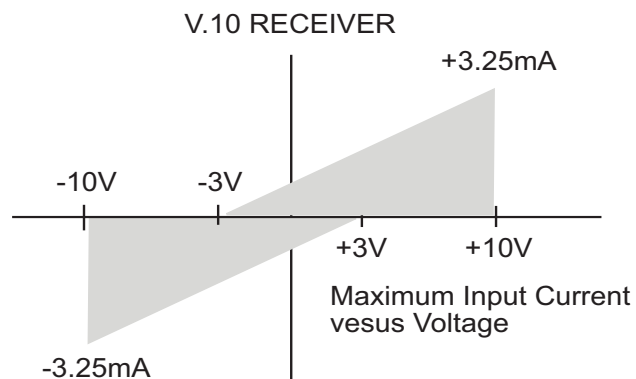


FIGURE 17. V.11 DRIVER OUTPUT TEST TERMINATED VOLTGE

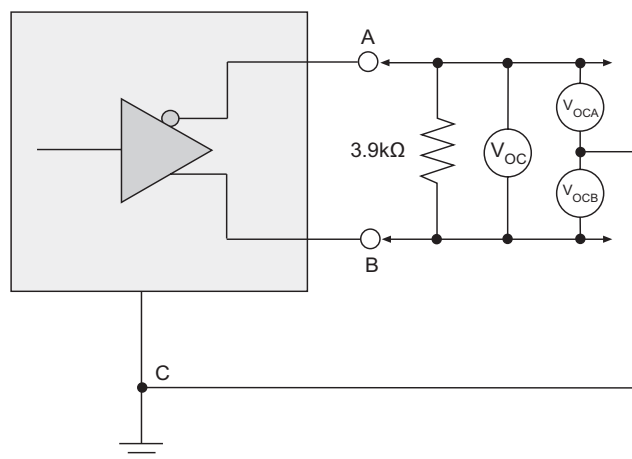


FIGURE 18. V.11 DRIVER OUTPUT TEST TERMINATED VOLTAGE

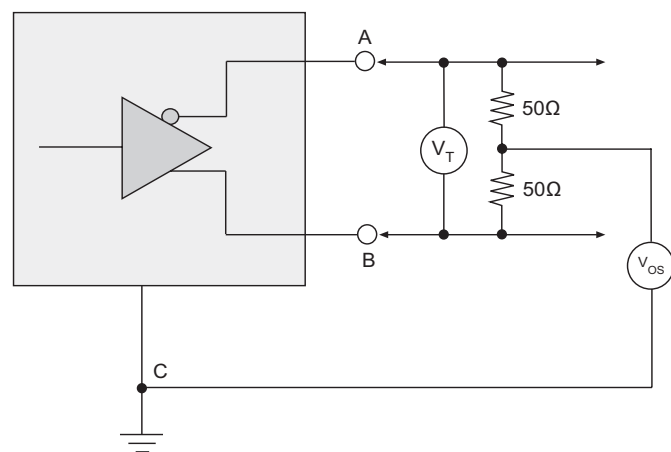


FIGURE 19. V.11 DRIVER OUTPUT SHORT-CIRCUIT CURRENT

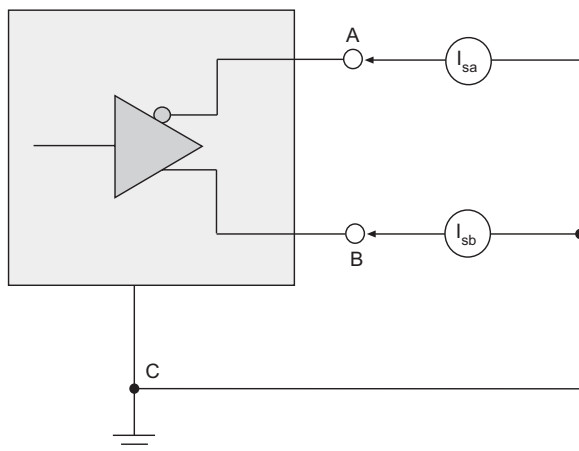


FIGURE 20. V.11 DRIVER OUTPUT POWER-OFF CURRENT

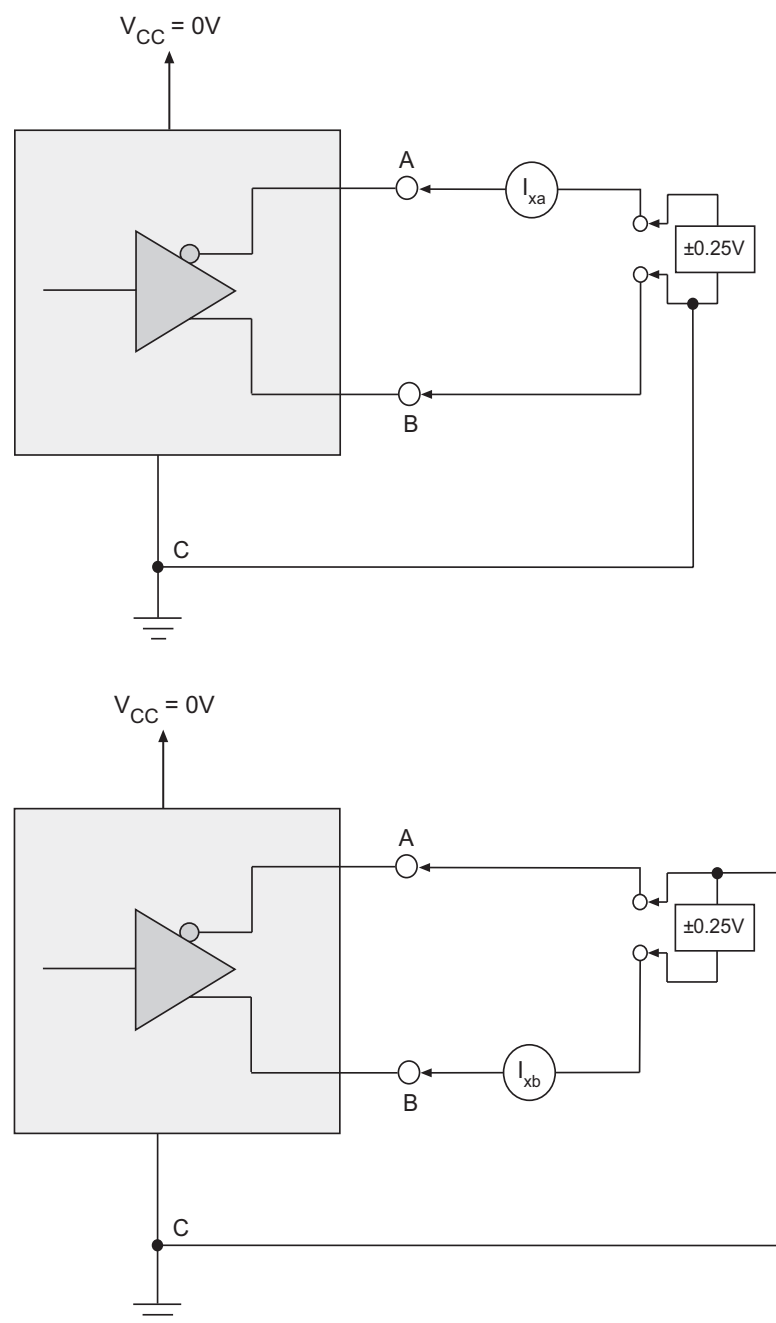


FIGURE 21. V.11 RECEIVER INPUT CURRENT

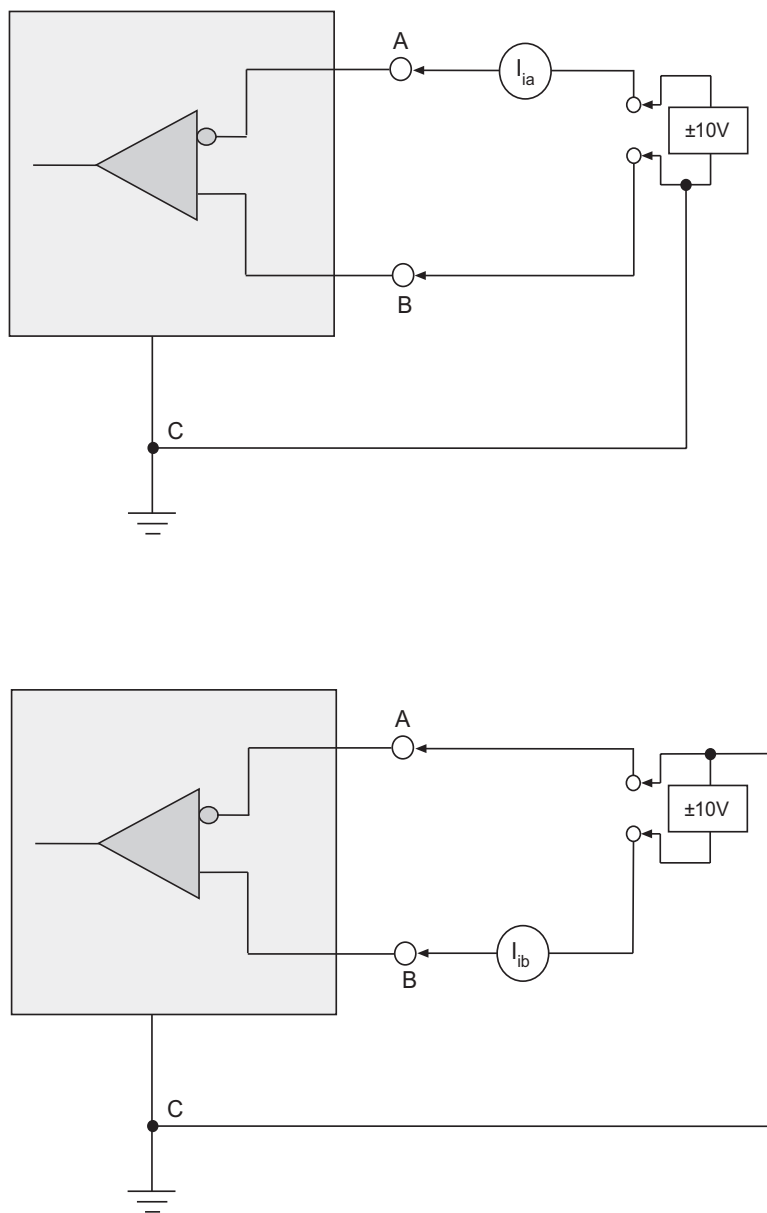


FIGURE 22. V.11 DRIVER OUTPUT RISE/FALL TIME

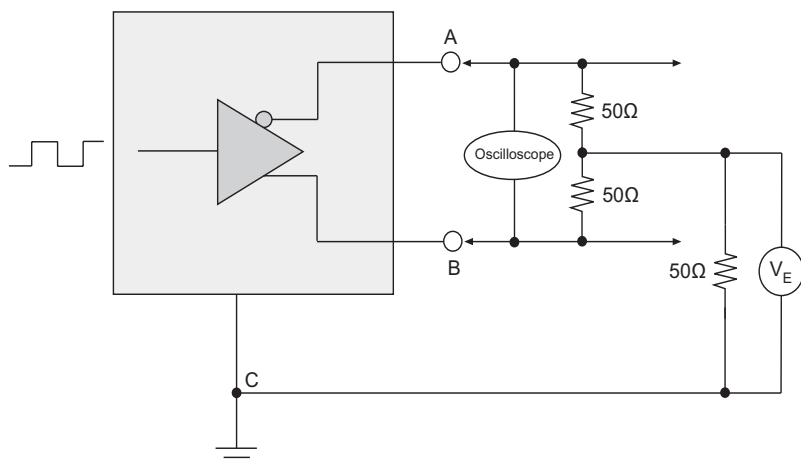
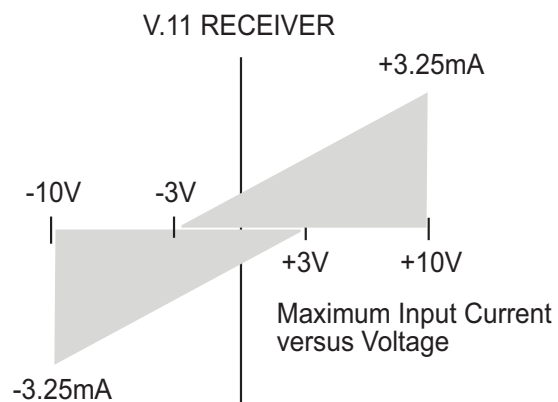


FIGURE 23. V.11 RECEIVER INPUT IV GRAPH



**FIGURE 24. V.11 RECEIVER INPUT CURRENT WITH TERMINATION**

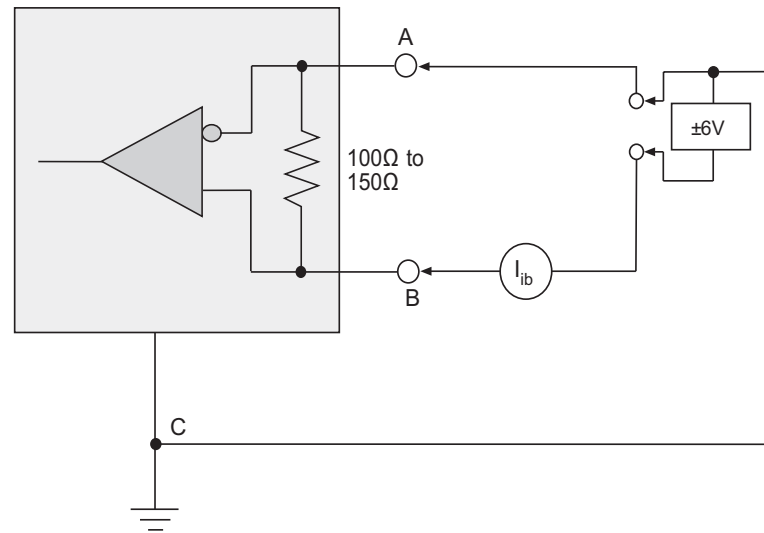
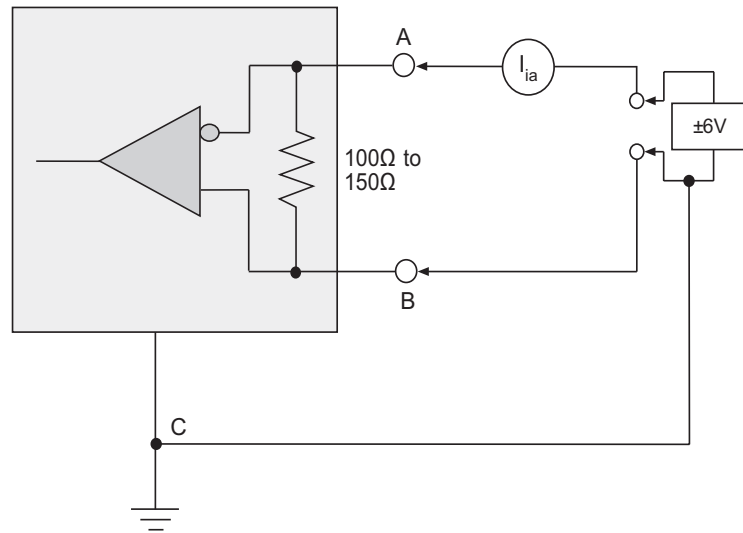


FIGURE 25. V.11 RECEIVER INPUT IV GRAPH WITH TERMINATION

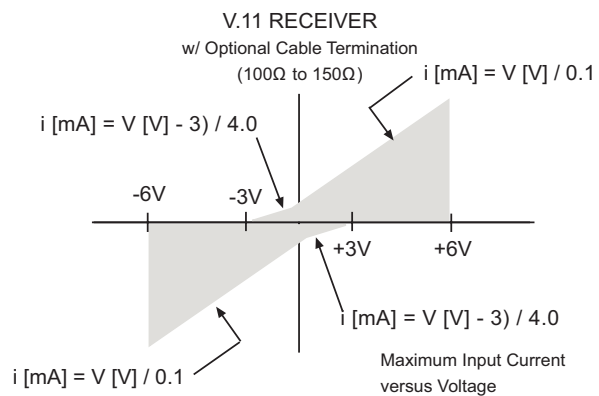


FIGURE 26. V.35 DRIVER OUTPUT TEST TERMINATED VOLTAGE

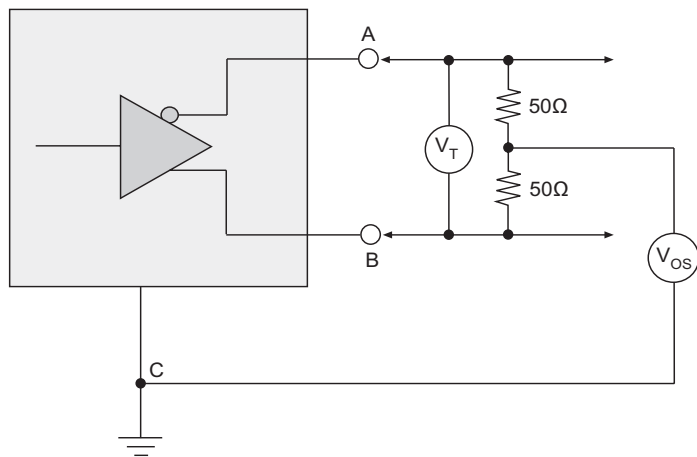


FIGURE 27. V.35 DRIVER OUTPUT SOURCE IMPEDANCE

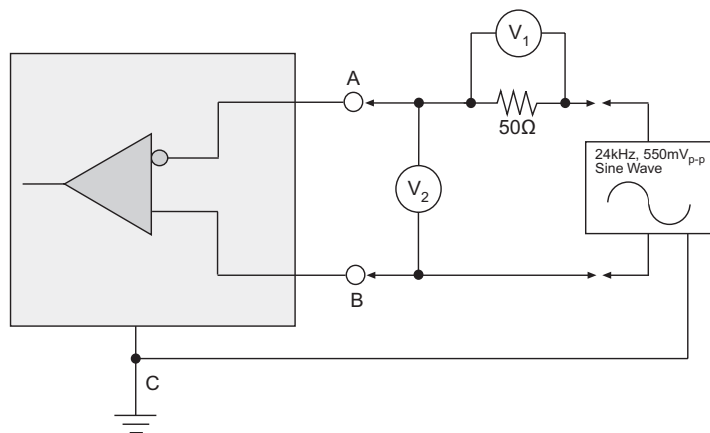


FIGURE 28. V.35 DRIVER OUTPUT SHORT-CIRCUIT IMPEDANCE

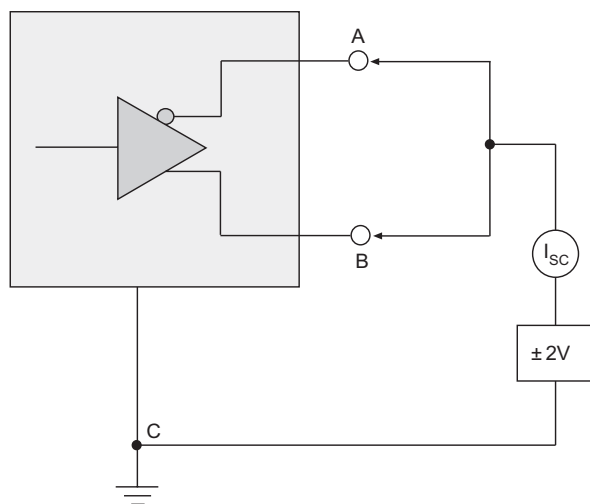


FIGURE 29. V.35 DRIVER OUTPUT RISE/FALL TIME

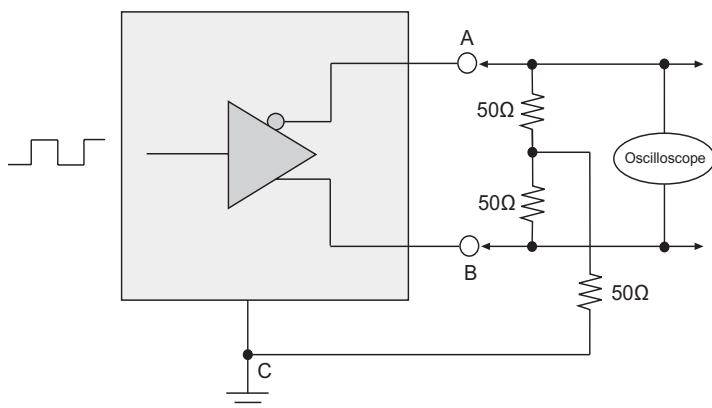


FIGURE 30. V.35 RECEIVER INPUT SOURCE IMPEDANCE

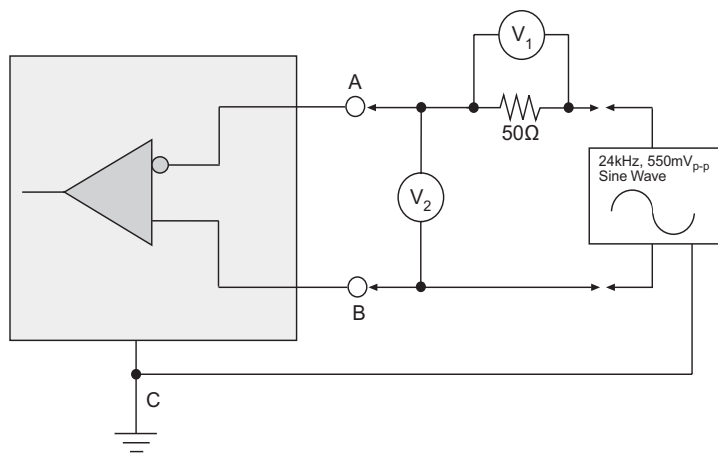


FIGURE 31. V.35 RECEIVER INPUT SHORT-CIRCUIT IMPEDANCE

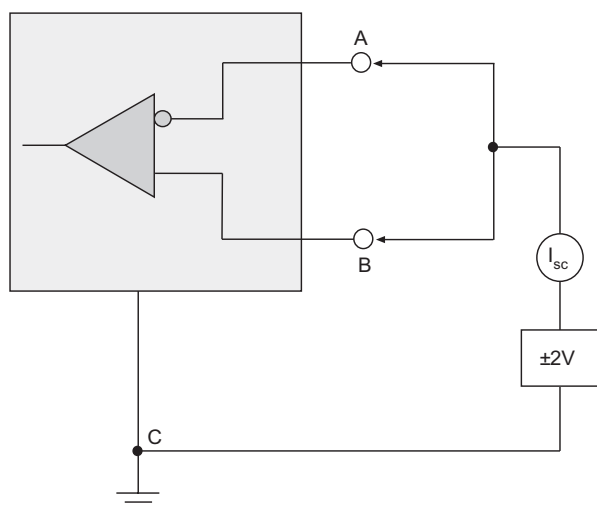
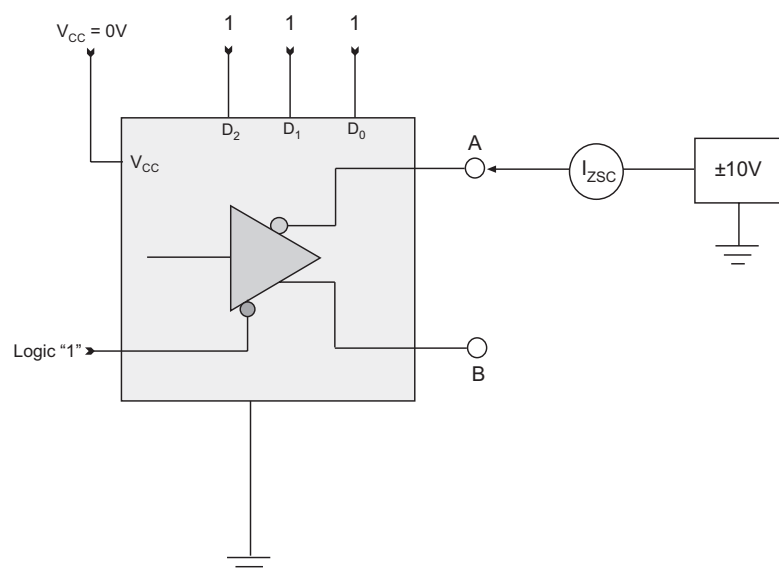


FIGURE 32. DRIVER OUTPUT CURRENT LEAKAGE TEST

Any one of the three conditions for disabling the driver.



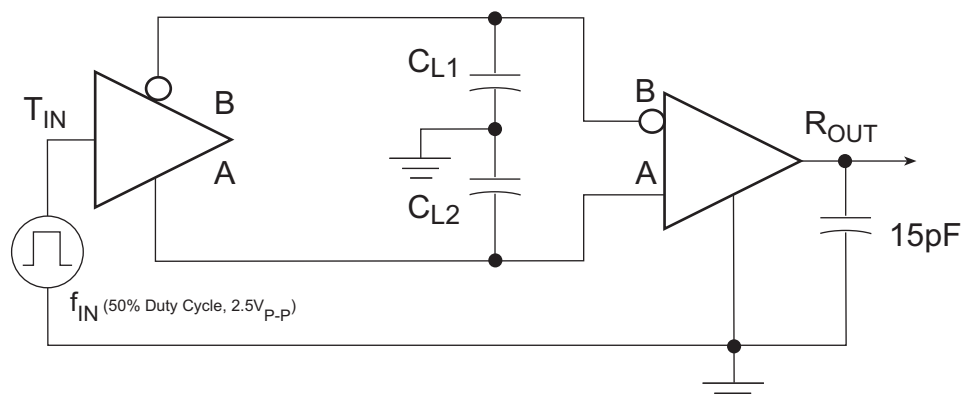
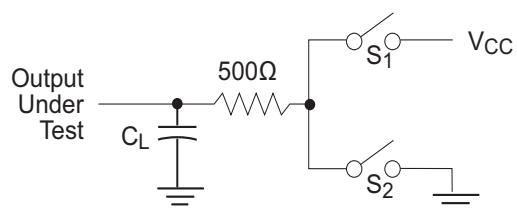
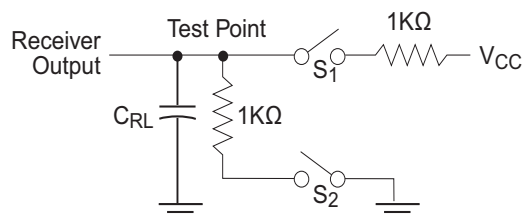
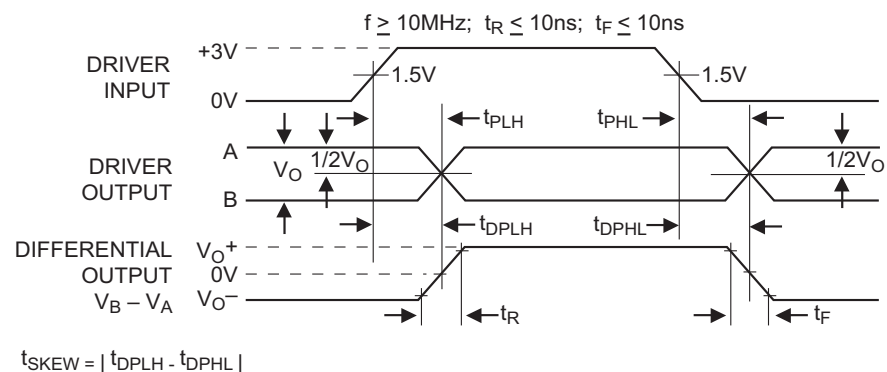
**FIGURE 33. DRIVER / RECEIVER TIMING TEST CIRCUIT**

**FIGURE 34. DRIVER TIMING TEST LOAD CIRCUIT**

**FIGURE 35. RECEIVER TIMING TEST LOAD CIRCUIT**

**FIGURE 36. DRIVER PROPAGATON DELAYS**


FIGURE 37. DRIVER ENABLE AND DISABLE TIMES

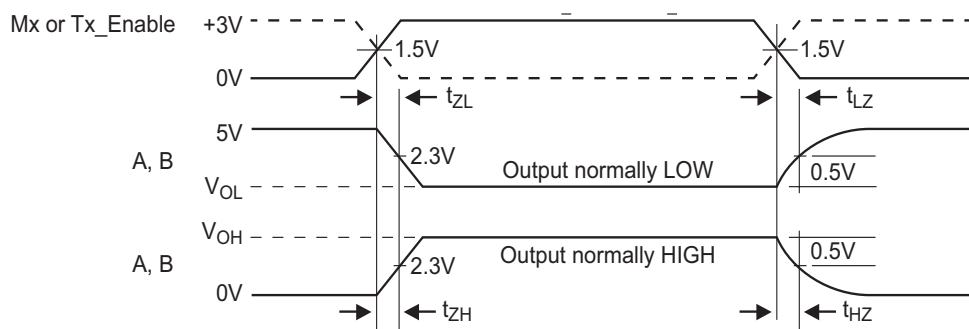


FIGURE 38. RECEIVER PROPAGATION DELAYS

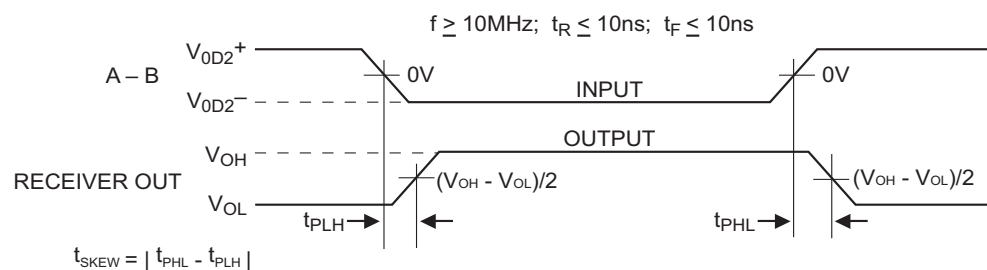


FIGURE 39. RECEIVER ENABLE AND DISABLE TIMES

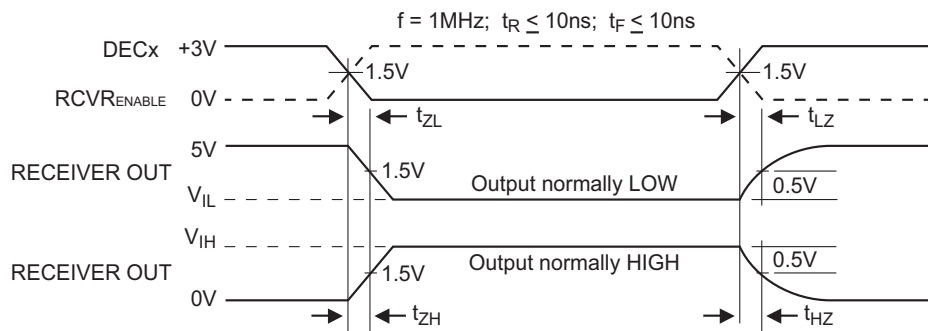


FIGURE 40. V.28 (RS-232) AND V.10 (RS-423) DRIVER ENABLE AND DISABLE TIMES

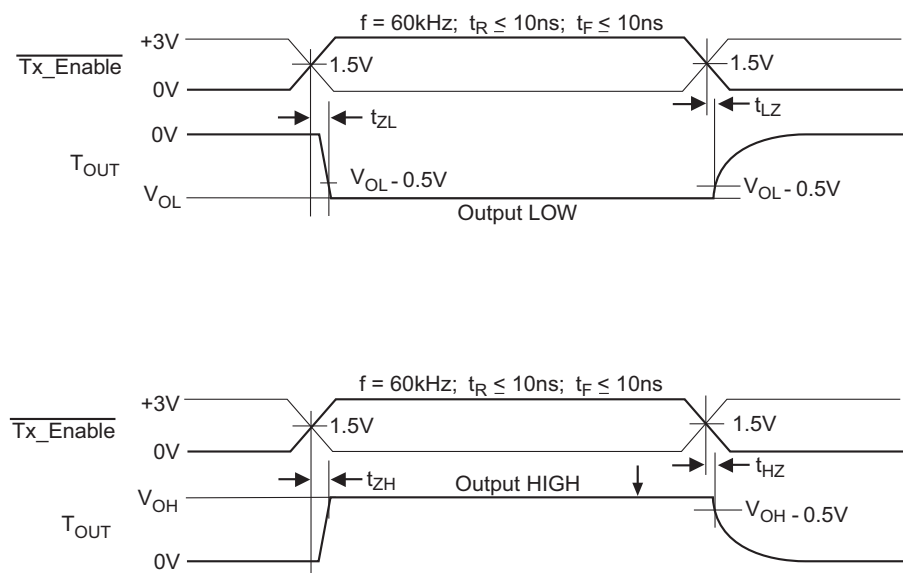


FIGURE 41. TYPICAL V.28 DRIVER OUTPUT WAVEFORM

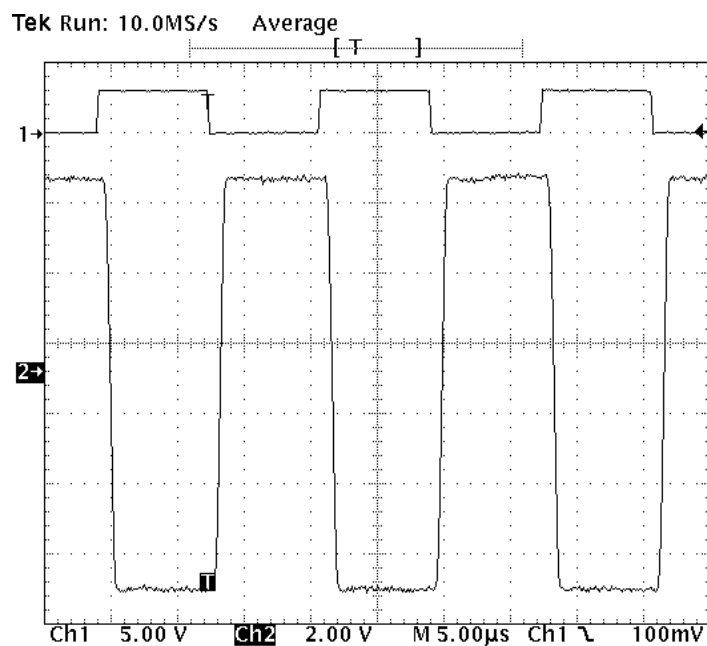


FIGURE 42. TYPICAL V.10 DRIVER OUTPUT WAVEFORM

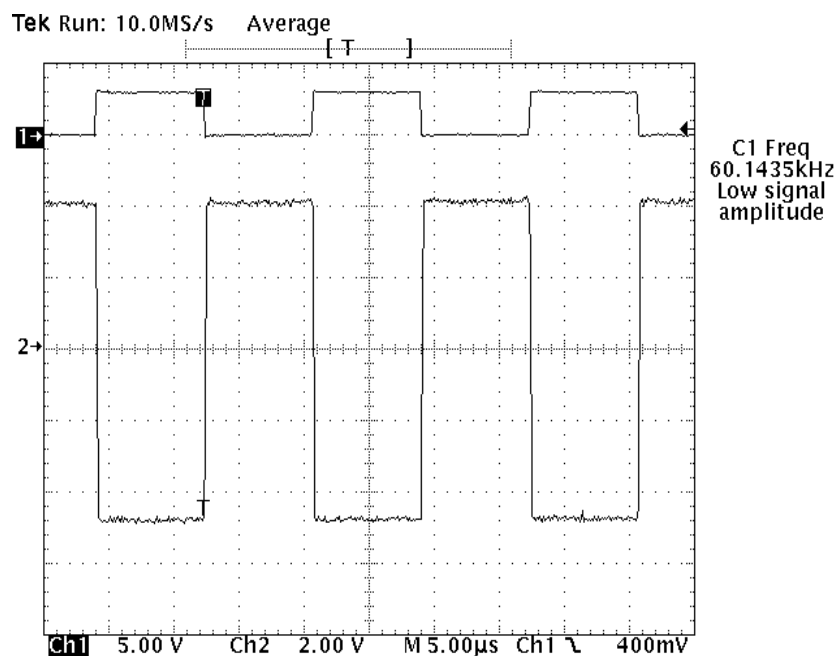


FIGURE 43. TYPICAL V.11 DRIVER OUTPUT WAVEFORM

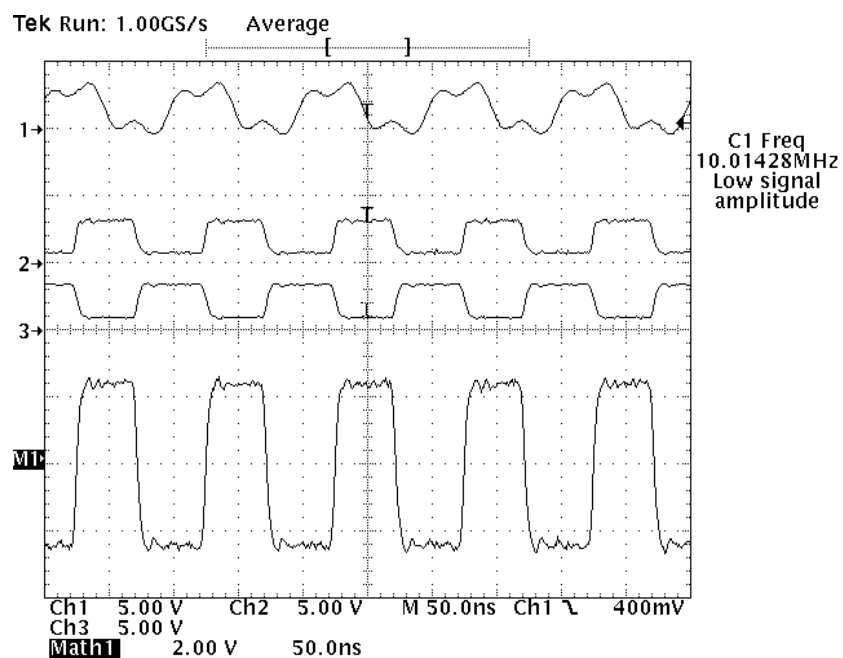


FIGURE 44. TYPICAL V.35 DRIVER OUTPUT WAVEFORM

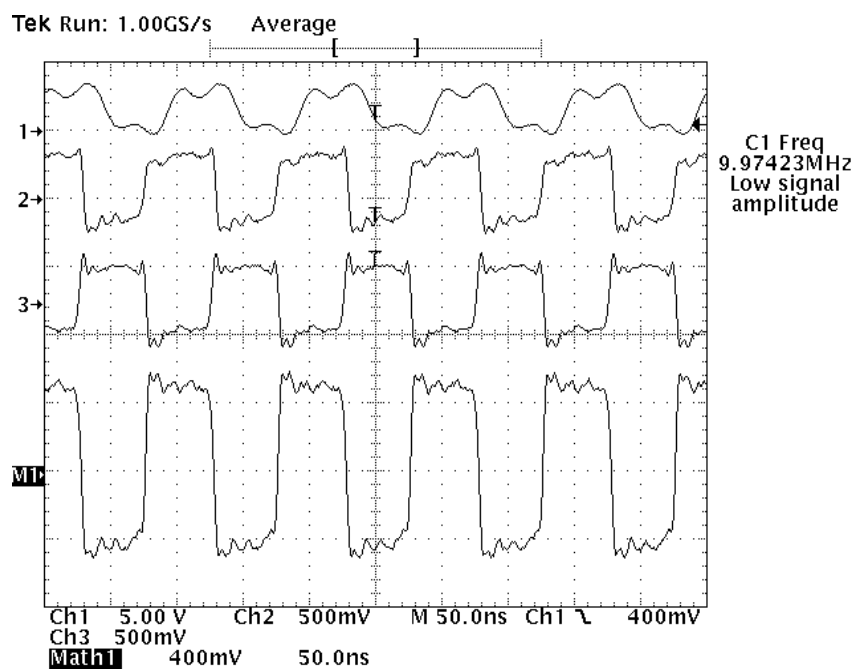
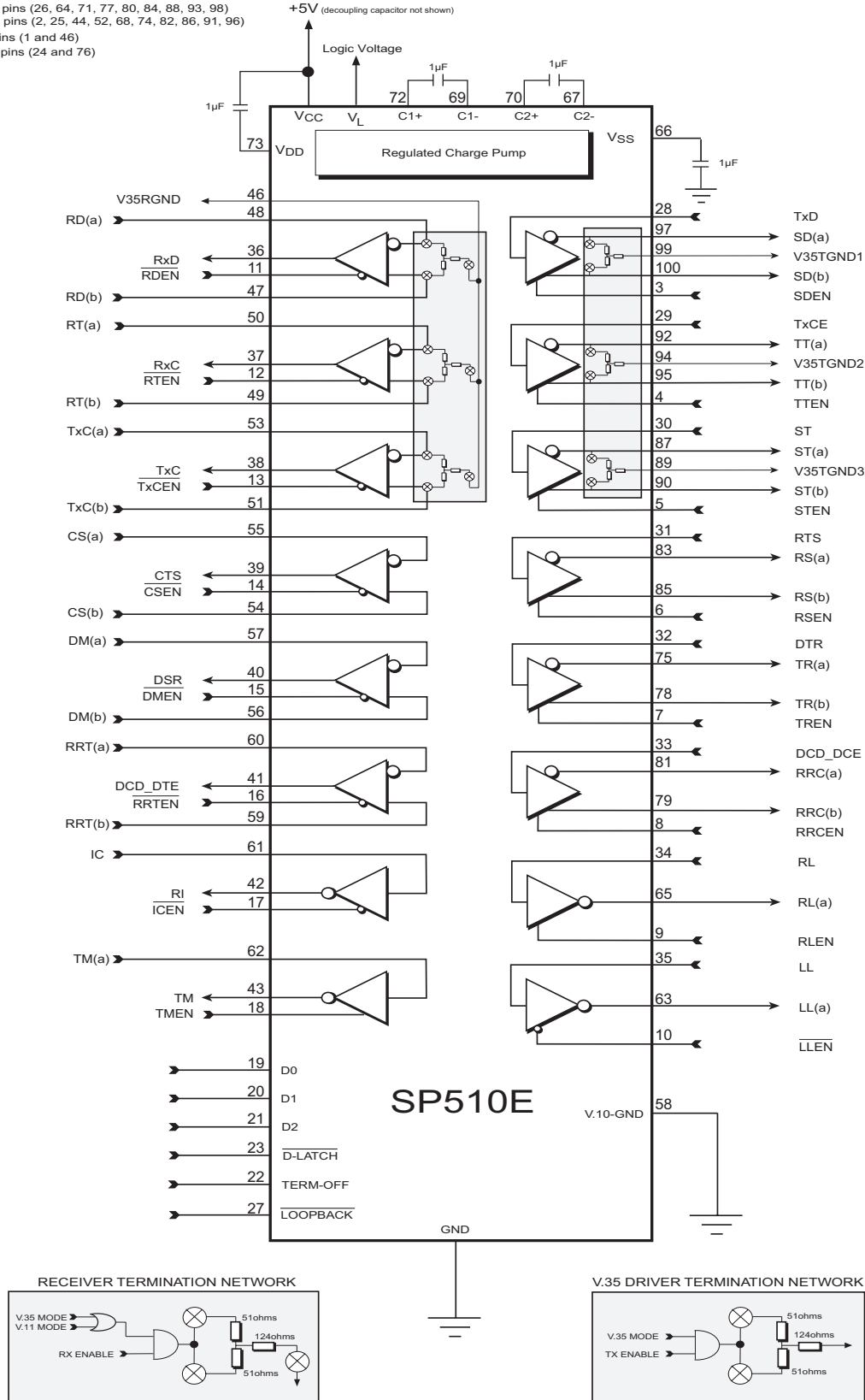
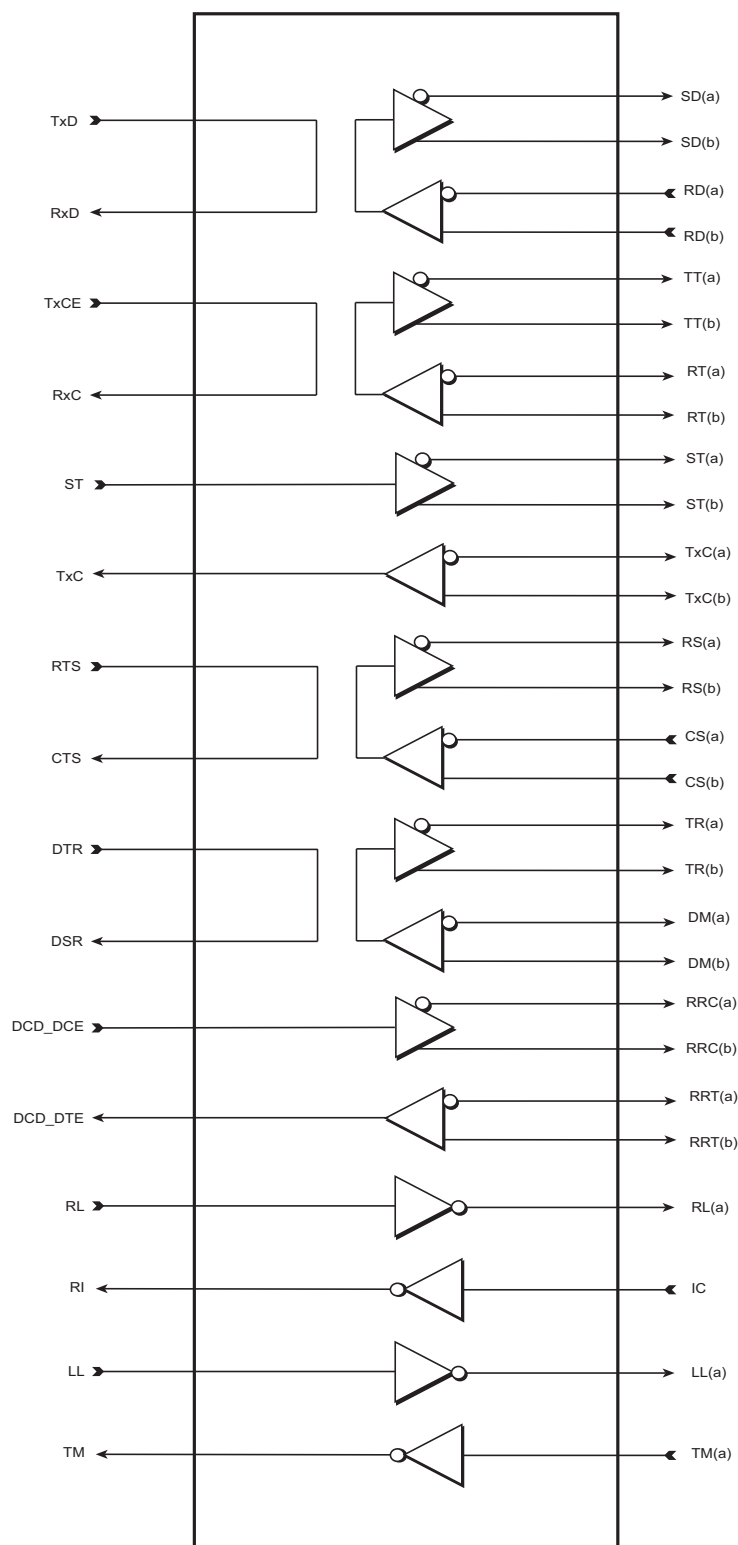


FIGURE 45. FUNCTIONAL DIAGRAM

VCC pins (26, 64, 71, 77, 80, 84, 88, 93, 98)  
GND pins (2, 25, 44, 52, 68, 74, 82, 86, 91, 96)  
VL pins (1 and 46)  
N.C. pins (24 and 76)



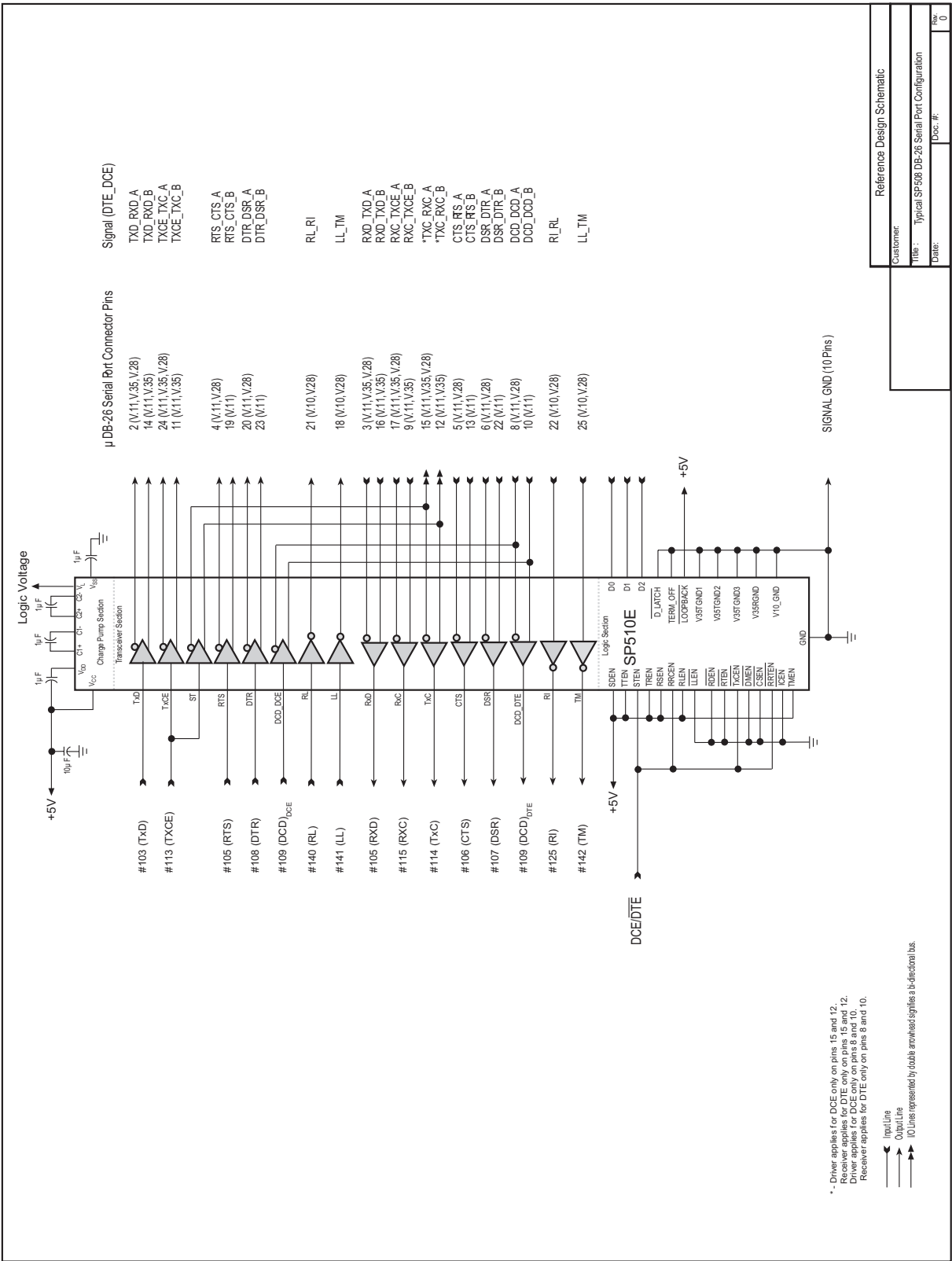
**FIGURE 46. SP510E LOOPBACK PATH**


SP510E  
ULTRA HIGH SPEED MULTIPROTOCOL TRANSCEIVER



REV. 1.0.0

FIGURE 48. TYPICAL CONFIGURATION TO SERIAL PORT CONNECTOR WITH DCE/DTE PROGRAMMABILITY

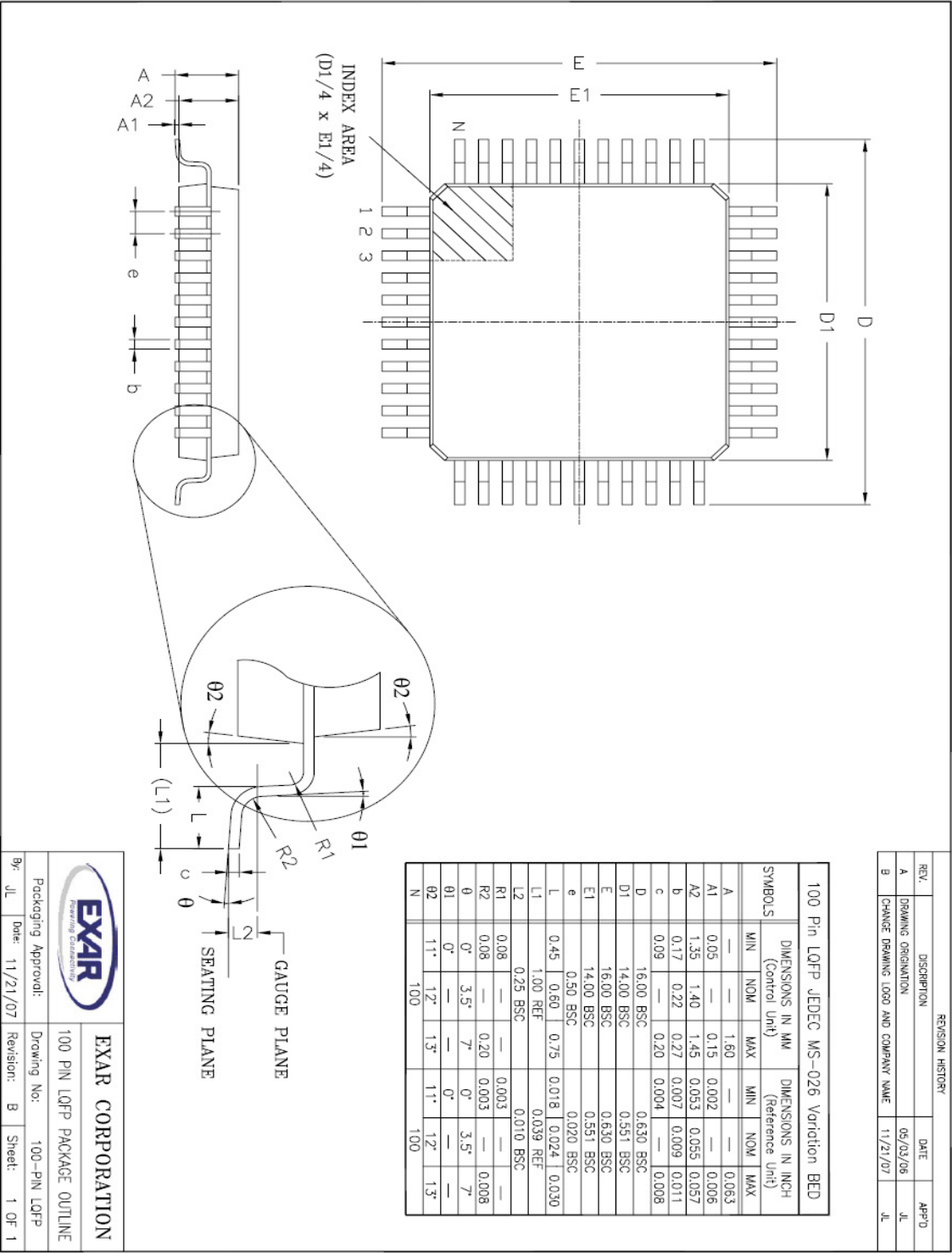


**Thermal Considerations**

High speed devices like the SP510E dissipate heat during normal operation. Actual power dissipation is a function of the switching frequency and loading. For maximum system performance and reliability designers should ensure sufficient air flow. Other commonly used methods for managing heat include heat sinks for higher powered devices, forced air flow (fans) and lower density board stuffing.

**PCB Design**

The use of multi layer printed circuit boards is recommended to provide both a better ground plane and a thermal path for heat dissipation. If possible, the ground plane should face the bottom of the package to form the thermal conduction plane. Two-sided printed circuit boards may be used where board dimensions and package count are small, but multi-layer boards allow for improved signal routing as well as improved signal integrity. A multi-layer board allows microstrip line techniques for high speed signal interconnections when the high speed signal lines on the inner layers.



**REVISION HISTORY**

| DATE      | REVISION | DESCRIPTION        |
|-----------|----------|--------------------|
| July 2012 | 1.0.0    | Production Release |

**NOTICE**

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