

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus™* Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16501 . . . WD PACKAGE
 SN74LVT16501 . . . DGG OR DL PACKAGE
 (TOP VIEW)

| | | | |
|----------|----|----|----------|
| OEAB | 1 | 56 | GND |
| LEAB | 2 | 55 | CLKAB |
| A1 | 3 | 54 | B1 |
| GND | 4 | 53 | GND |
| A2 | 5 | 52 | B2 |
| A3 | 6 | 51 | B3 |
| V_{CC} | 7 | 50 | V_{CC} |
| A4 | 8 | 49 | B4 |
| A5 | 9 | 48 | B5 |
| A6 | 10 | 47 | B6 |
| GND | 11 | 46 | GND |
| A7 | 12 | 45 | B7 |
| A8 | 13 | 44 | B8 |
| A9 | 14 | 43 | B9 |
| A10 | 15 | 42 | B10 |
| A11 | 16 | 41 | B11 |
| A12 | 17 | 40 | B12 |
| GND | 18 | 39 | GND |
| A13 | 19 | 38 | B13 |
| A14 | 20 | 37 | B14 |
| A15 | 21 | 36 | B15 |
| V_{CC} | 22 | 35 | V_{CC} |
| A16 | 23 | 34 | B16 |
| A17 | 24 | 33 | B17 |
| GND | 25 | 32 | GND |
| A18 | 26 | 31 | B18 |
| OEBA | 27 | 30 | CLKBA |
| LEBA | 28 | 29 | GND |

description

The 'LVT16501 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.



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**SN54LVT16501, SN74LVT16501
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

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description (continued)

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, and CLKBA. The output enables are complementary (OEAB is active high and \overline{OEBA} is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the input/output (I/O) pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN54LVT16501 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT16501 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE[†]

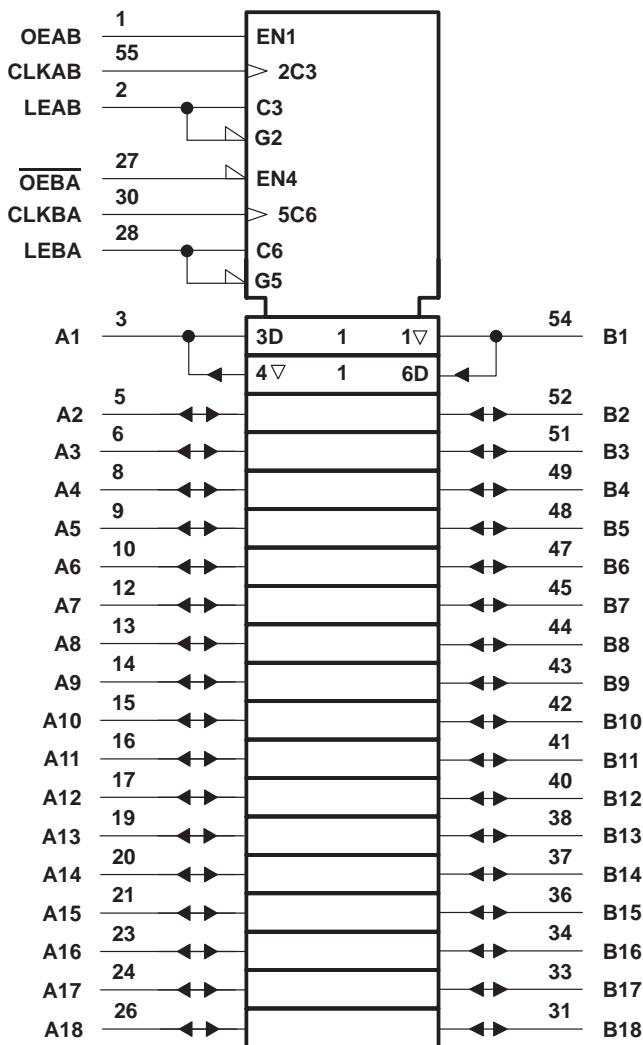
| INPUTS | | | | OUTPUT |
|--------|------|-------|---|------------------|
| OEAB | LEAB | CLKAB | A | B |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↑ | L | L |
| H | L | ↑ | H | H |
| H | L | H | X | B_0^{\ddagger} |
| H | L | L | X | $B_0^{\$}$ |

[†] A-to-B data flow is shown; B-to-A flow is similar but uses \overline{OEBA} , LEBA, and CLKBA.

[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

[§] Output level before the indicated steady-state input conditions were established

logic symbol†

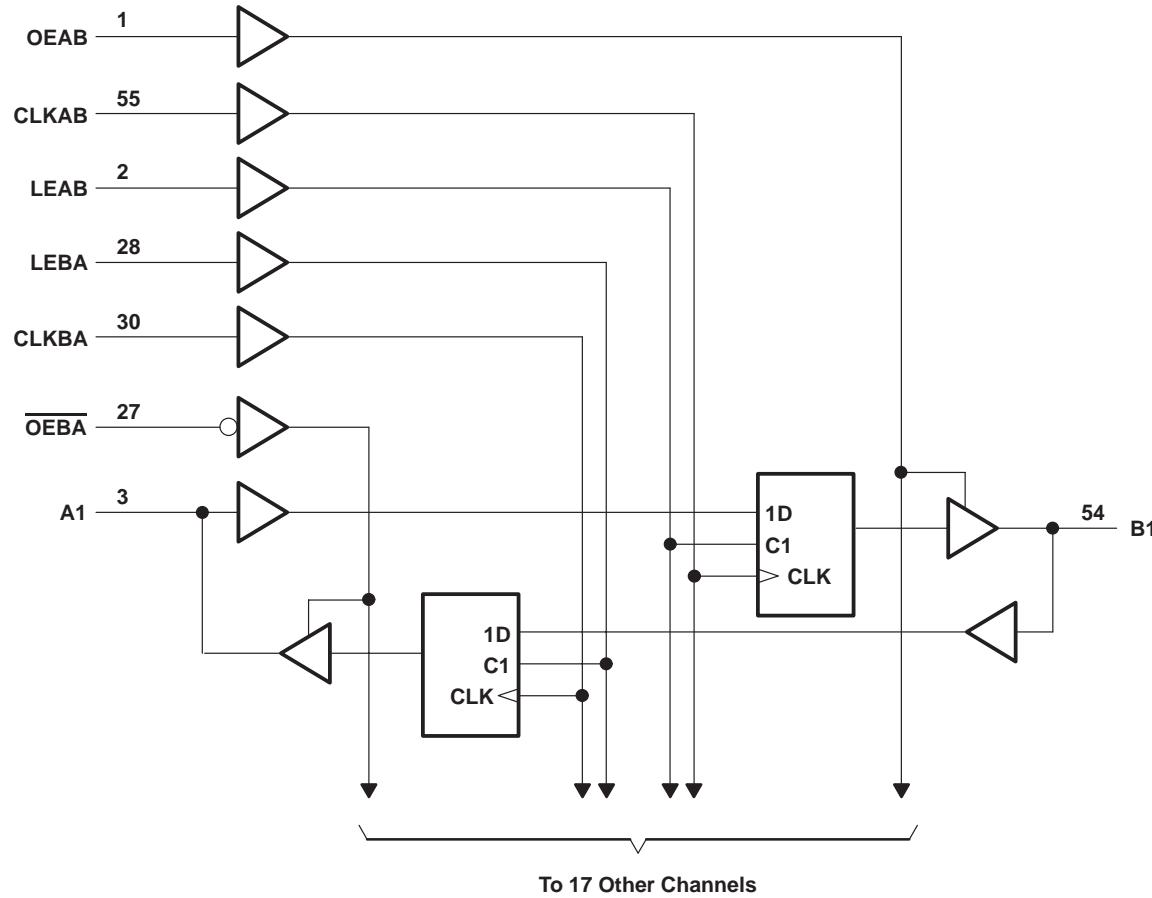


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT16501, SN74LVT16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

1. Input and Output Negative Voltage Ratings must be observed. The Input and Output Clamp Current Ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

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3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
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recommended operating conditions (see Note 4)

| | | SN54LVT16501 | | SN74LVT16501 | | UNIT |
|-----------------|------------------------------------|-----------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V _I | Input voltage | | 5.5 | | 5.5 | V |
| I _{OH} | High-level output current | | -24 | | -32 | mA |
| I _{OL} | Low-level output current | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | 10 | ns/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

**SN54LVT16501, SN74LVT16501
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54LVT16501 | | | SN74LVT16501 | | | UNIT |
|--------------------|--|---|-----------------------|---------|----------------|-----------|---------------|---------------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V_{IK} | $V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$ | | | -1.2 | | | -1.2 | V |
| V_{OH} | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$ | $V_{CC} - 0.2$ | | | $V_{CC} - 0.2$ | | | V |
| | $V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$ | 2.4 | | | 2.4 | | | |
| | $V_{CC} = 3 \text{ V}$ | $I_{OH} = -24 \text{ mA}$ | 2 | | | | 2 | |
| | | $I_{OH} = -32 \text{ mA}$ | | | | | | |
| V_{OL} | $V_{CC} = 2.7 \text{ V}$ | $I_{OL} = 100 \mu\text{A}$ | | 0.2 | | 0.2 | | V |
| | | $I_{OL} = 24 \text{ mA}$ | | 0.5 | | 0.5 | | |
| | $V_{CC} = 3 \text{ V}$ | $I_{OL} = 16 \text{ mA}$ | | 0.4 | | 0.4 | | |
| | | $I_{OL} = 32 \text{ mA}$ | | 0.5 | | 0.5 | | |
| | | $I_{OL} = 48 \text{ mA}$ | | 0.55 | | | | |
| | | $I_{OL} = 64 \text{ mA}$ | | | | 0.55 | | |
| | | | | | | | | |
| I_I | Control pins | $V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ or GND | | ± 1 | | ± 1 | | μA |
| | | $V_{CC} = 0$ or 3.6 V , $V_I = 5.5 \text{ V}$ | | 10 | | 10 | | |
| | A or B ports‡ | $V_{CC} = 3.6 \text{ V}$ | $V_I = 5.5 \text{ V}$ | 120 | | 20 | | |
| | | | $V_I = V_{CC}$ | 1 | | 1 | | |
| | | $V_I = 0$ | | -5 | | -5 | | |
| I_{off} | $V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V | | | | | ± 100 | μA | |
| $I_I(\text{hold})$ | A or B ports | $V_{CC} = 3 \text{ V}$ | $V_I = 0.8 \text{ V}$ | 75 | | 75 | | μA |
| | | | $V_I = 2 \text{ V}$ | -75 | | -75 | | |
| I_{OZH} | $V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$ | | | | | 1 | μA | |
| I_{OZL} | $V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$ | | | | | -1 | μA | |
| I_{CC} | $V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ or GND | $I_O = 0$ | Outputs high | 0.12 | | 0.12 | | mA |
| | | | Outputs low | 5 | | 5 | | |
| | | | Outputs disabled | 0.12 | | 0.12 | | |
| $\Delta I_{CC}^§$ | $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND | | | 0.2 | | 0.2 | mA | |
| C_i | $V_I = 3 \text{ V or } 0$ | | | 3.5 | | 3.5 | pF | |
| C_{io} | $V_O = 3 \text{ V or } 0$ | | | 12 | | 12 | pF | |

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at V_{CC} or GND

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | SN54LVT16501 | | | | SN74LVT16501 | | | | UNIT | | |
|--------------------|-----------------|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|-------------------------|-----|------|-----|-----|
| | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| f _{clock} | Clock frequency | | | 0 | 150 | 0 | 125 | 0 | 150 | 0 | 125 | MHz |
| t _W | Pulse duration | LE high | | 3.3 | | 3.3 | | 3.3 | | ns | | |
| | | CLK high or low | | 3.3 | | 3.3 | | 3.3 | | | | |
| t _{SU} | Setup time | A before CLKAB↑ | | 1.6 | | 2.1 | | 1.6 | | ns | | |
| | | B before CLKBA↑ | | 1.6 | | 2.1 | | 1.6 | | | | |
| | | A or B before LE↓, CLK high | | 3.1 | | 2.7 | | 2.6 | | | | |
| | | A or B before LE↓, CLK low | | 2.6 | | 2.0 | | 2 | | | | |
| t _H | Hold time | A or B after CLK↑ | | 2 | | 2.1 | | 2 | | ns | | |
| | | A or B after LE↓ | | 1.3 | | 1.2 | | 0.9 | | | | |

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

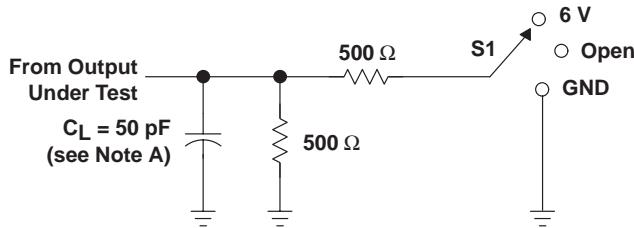
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVT16501 | | | | SN74LVT16501 | | | | UNIT | |
|------------------|-----------------|----------------|------------------------------------|-----|-------------------------|-----|------------------------------------|------|-------------------------|-----|------|--|
| | | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | | |
| f _{max} | | | 150 | | 125 | | 150 | | 125 | | MHz | |
| t _{PLH} | B or A | A or B | 1.7 | 5.4 | 6.8 | 1.7 | 3 | 5.4 | 6.8 | ns | | |
| | | | 1.6 | 6 | 7.8 | 1.6 | 3.2 | 5.9 | 7.7 | | | |
| t _{PLH} | LEBA or LEAB | A or B | 2.3 | 7.3 | 9 | 2.3 | 4 | 7 | 8.5 | ns | | |
| | | | 2.7 | 8.2 | 9.8 | 2.7 | 4.3 | 7.9 | 9.7 | | | |
| t _{PLH} | CLKBA or CLKAB | A or B | 2.5 | 8.3 | 9.7 | 2.5 | 4.1 | 7.9 | 9.2 | ns | | |
| | | | 3.5 | 9.4 | 10.7 | 3.5 | 5.4 | 8.9 | 10.4 | | | |
| t _{PZH} | OEBA or OEAB | A or B | 1.2 | 5.1 | 6.1 | 1.2 | 3 | 5 | 5.9 | ns | | |
| | | | 1.5 | 5.9 | 7 | 1.5 | 3 | 5.8 | 6.9 | | | |
| t _{PZL} | OEBA or OEAB | A or B | 2.7 | 7.5 | 8.5 | 2.7 | 4.6 | 7.4 | 8.3 | ns | | |
| | | | 2.8 | 6.8 | 7.5 | 2.8 | 4.7 | 6.7 | 7.2 | | | |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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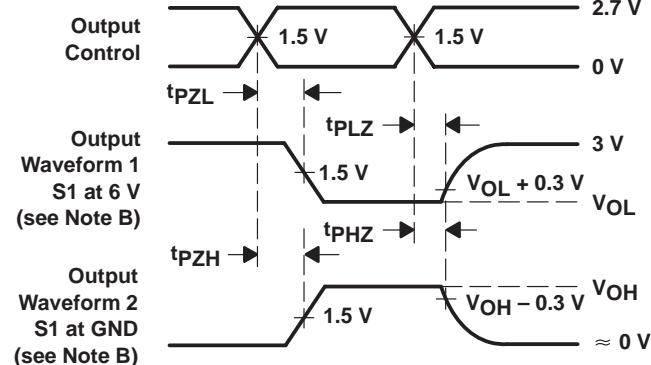
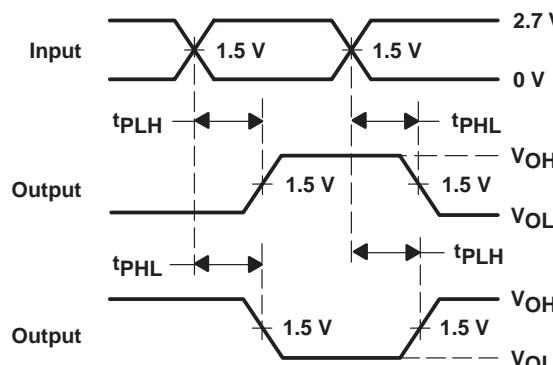
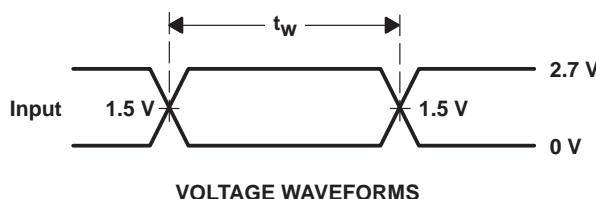
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PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |

LOAD CIRCUIT



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74LVT16501DGGRE4 | NRND | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT16501DGGR | NRND | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT16501DL | NRND | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT16501DLG4 | OBsolete | SSOP | DL | 56 | | TBD | Call TI | Call TI |
| SN74LVT16501DLR | NRND | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVT16501DLRG4 | OBsolete | SSOP | DL | 56 | | TBD | Call TI | Call TI |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

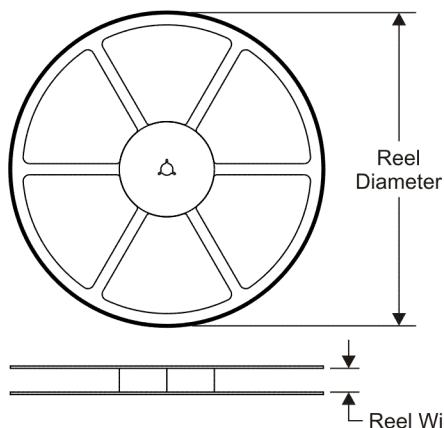
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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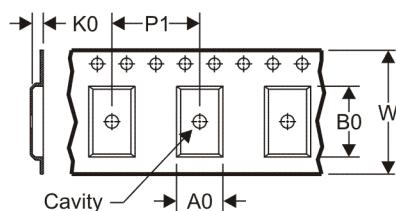
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

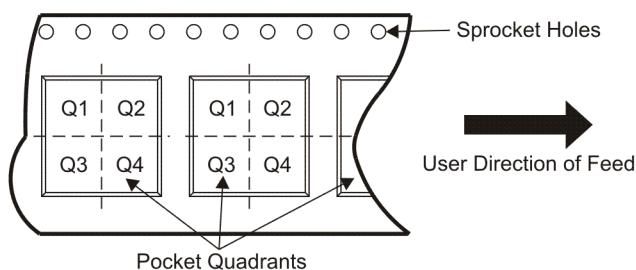


TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

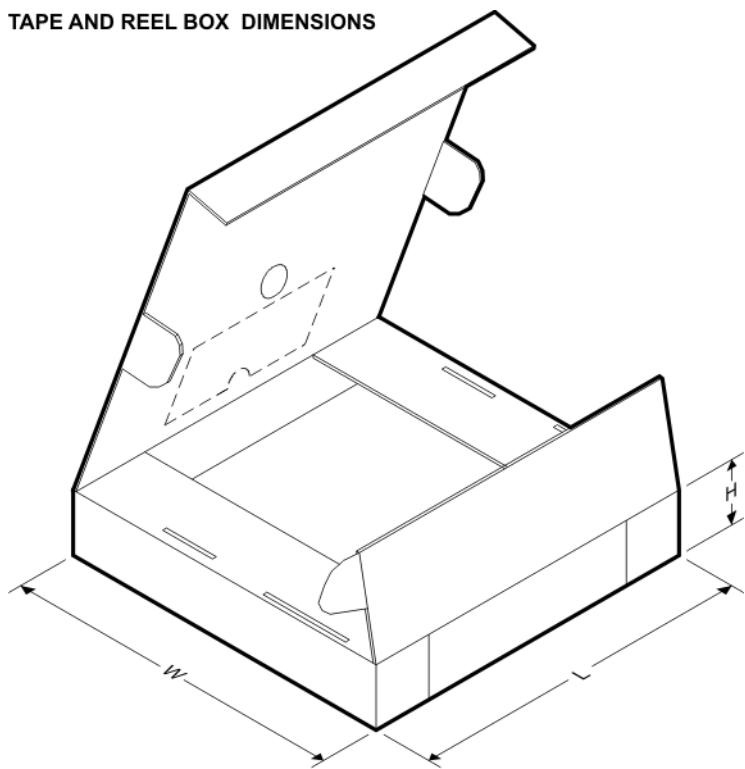
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVT16501DGGR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74LVT16501DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



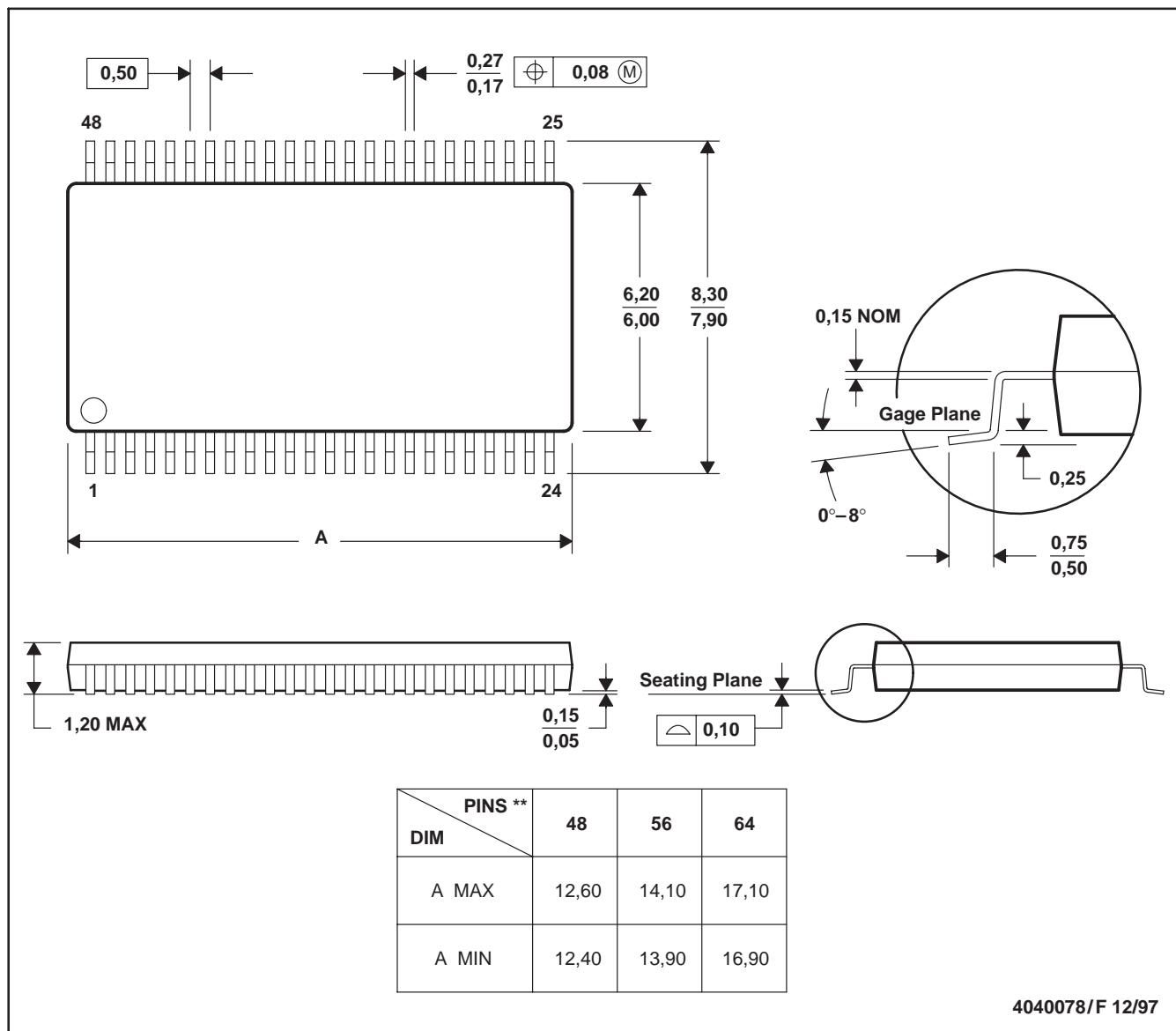
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVT16501DGGR | TSSOP | DGG | 56 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LVT16501DLR | SSOP | DL | 56 | 1000 | 346.0 | 346.0 | 49.0 |

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

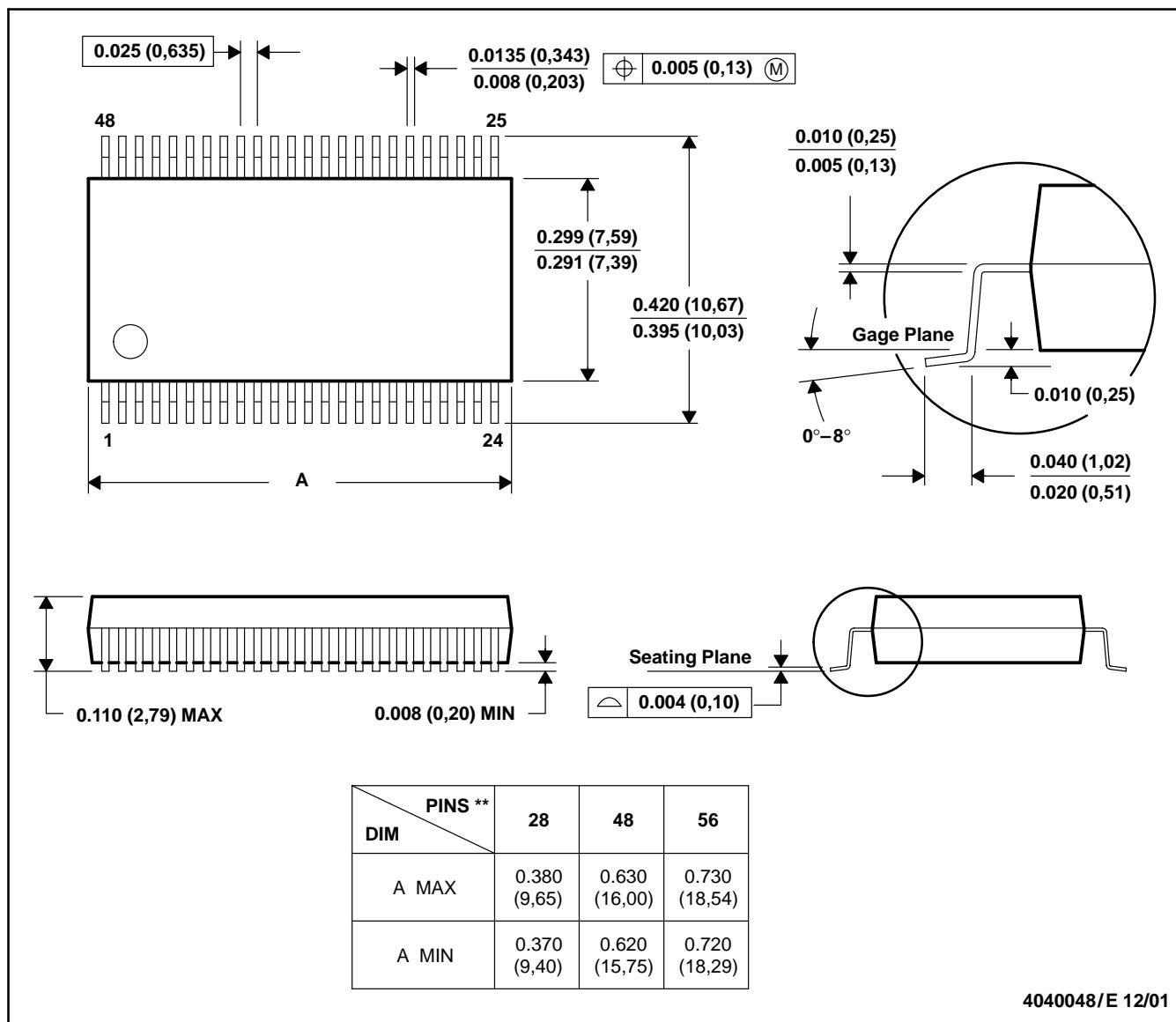


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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