

# MC100LVEL17

## 3.3V ECL Quad Differential Receiver

The MC100LVEL17 is a 3.3 V ECL, quad differential receiver. The device is functionally equivalent to the E116 device with the capability of operation from either a -3.3 V or +3.3 V supply voltage.

Under open input conditions, the  $\bar{D}$  input will be biased at  $V_{CC}/2$  and the D input will be pulled down to  $V_{EE}$ . This operation will force the Q output LOW and ensure stability.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

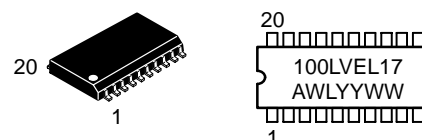
- 325 ps Propagation Delay
- High Bandwidth Output Transitions
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to -3.8 V
- Internal Input Pulldown Resistors D Inputs; Pullup and Pulldown on  $\bar{D}$  Inputs
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$



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### MARKING DIAGRAM\*



**SO-20L  
DW SUFFIX  
CASE 751D**

A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

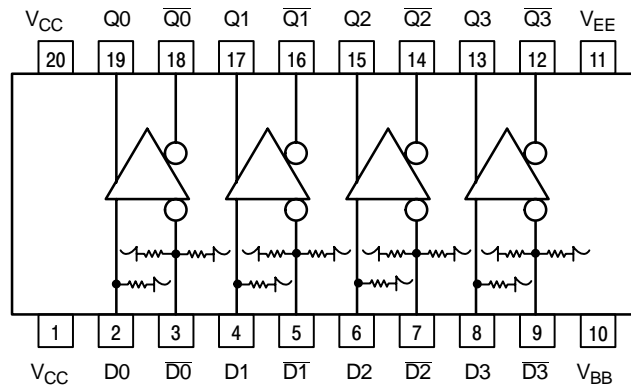
\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC100LVEL17DW	SO-20L	38 Units/Rail
MC100LVEL17DWR2	SO-20L	1000 Tape & Reel

<sup>†</sup>For additional tape and reel information, refer to Brochure BRD8011/D.

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\* All V<sub>CC</sub> pins are tied together on the die.

Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Logic Diagram and Pinout: (Top View)**

## PIN DESCRIPTION

PIN	FUNCTION
D <sub>n</sub> , $\overline{D}_n$	ECL Differential Data Inputs
Q <sub>n</sub> , $\overline{Q}_n$	ECL Differential Data Outputs
V <sub>BB</sub>	Reference Voltage Output
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply

## ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 2 kV > 200 V > 4 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in
Transistor Count	141
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

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## MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8 to 0	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-8 to 0	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 to 0 -6 to 0	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SO-20L SO-20L	90 60	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SO-20L	30 to 35	°C/W
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

## LVPECL DC CHARACTERISTICS V<sub>CC</sub> = 3.3 V; V<sub>EE</sub> = 0.0 V (Note 3)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		26	31		26	31		27	33	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 4)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V <sub>OL</sub>	Output LOW Voltage (Note 4)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V <sub>BB</sub>	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 5)										
	V <sub>pp</sub> < 500 mV	1.3		2.9	1.2		2.9	1.2		2.9	V
	V <sub>pp</sub> ≥ 500 mV	1.5		2.9	1.4		2.9	1.4		2.9	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current										
	Dn Dn	0.5 -300			0.5 -300			0.5 -300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary ±0.3 V.

4. Outputs are terminated through a 50 ohm resistor to V<sub>CC</sub>-2 volts.

5. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V<sub>ppmin</sub> and 1 V.

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## LVNECL DC CHARACTERISTICS $V_{CC} = 0.0\text{ V}$ ; $V_{EE} = -3.3\text{ V}$ (Note 6)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		26	31		26	31		27	33	mA
$V_{OH}$	Output HIGH Voltage (Note 7)	- 1085	- 1005	- 880	- 1025	- 955	- 880	- 1025	- 955	- 880	mV
$V_{OL}$	Output LOW Voltage (Note 7)	- 1830	- 1695	- 1555	- 1810	- 1705	- 1620	- 1810	- 1705	- 1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	- 1165		- 880	- 1165		- 880	- 1165		- 880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	- 1810		- 1475	- 1810		- 1475	- 1810		- 1475	mV
$V_{BB}$	Output Voltage Reference	- 1.38		- 1.26	- 1.38		- 1.26	- 1.38		- 1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 8)										
	$V_{pp} < 500\text{ mV}$	- 2.0		- 0.4	- 2.1		- 0.4	- 2.1		- 0.4	V
	$V_{pp} \geq 500\text{ mV}$	- 1.8		- 0.4	- 1.9		- 0.4	- 1.9		- 0.4	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$D_n$	0.5		0.5			0.5			$\mu\text{A}$
		$\overline{D_n}$	- 300		- 300			- 300			$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

7. Outputs are terminated through a 50 ohm resistor to  $V_{CC}-2$  volts.

8.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

## AC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$ ; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$ ; $V_{EE} = -3.3\text{ V}$ (Note 9)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency					1.75					GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay D to Q Diff S.E.	330 280		530 580	350 300		550 600	360 310		560 610	ps
$t_{SKEW}$	Skew Output-to-Output (Note 10) Part-to-Part (Diff) (Note 10) Duty Cycle (Diff) (Note 11)			75 200 25			75 200 25			75 200 25	ps
$t_{JITTER}$	Random Clock Jitter (RMS)					0.7					ps
$V_{PP}$	Input Swing (Note 12)	150		1000	150		1000	150		1000	mV
$t_r$ $t_f$	Output Rise/Fall Times Q (20% - 80%)	280		550	280		550	280		550	ps

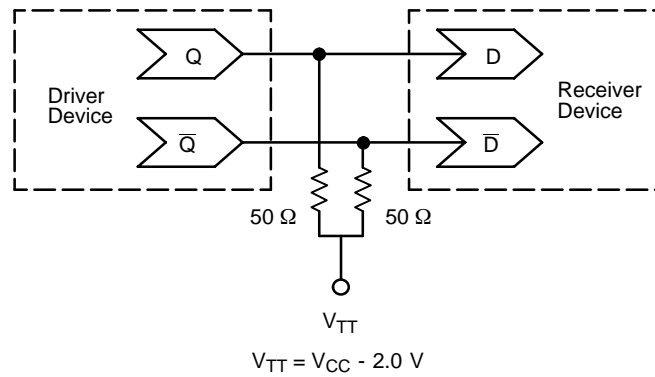
9.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

10. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.

11. Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.

12.  $V_{pp(min)}$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .

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**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 - Termination of ECL Logic Devices.)

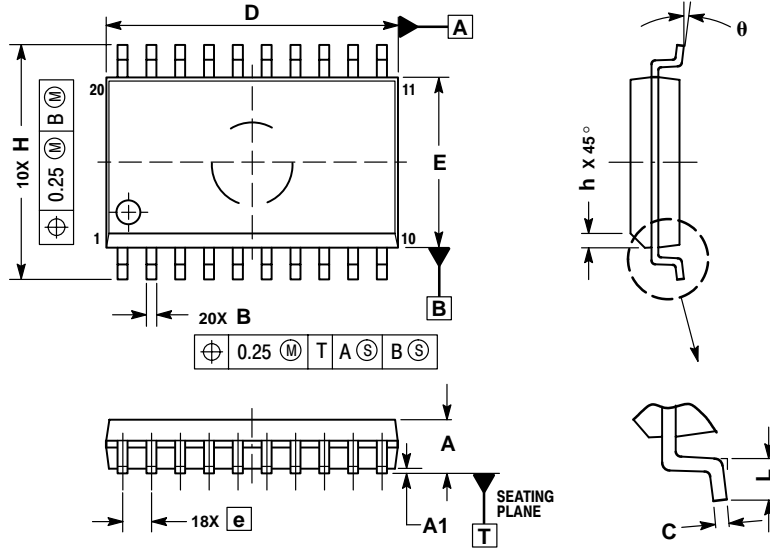
### Resource Reference of Application Notes

<b>AN1404</b>	- ECLinPS Circuit Performance at Non-Standard $V_{IH}$ Levels
<b>AN1405</b>	- ECL Clock Distribution Techniques
<b>AN1406</b>	- Designing with PECL (ECL at +5.0 V)
<b>AN1503</b>	- ECLinPS I/O SPICE Modeling Kit
<b>AN1504</b>	- Metastability and the ECLinPS Family
<b>AN1560</b>	- Low Voltage ECLinPS SPICE Modeling Kit
<b>AN1568</b>	- Interfacing Between LVDS and ECL
<b>AN1596</b>	- ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
<b>AN1650</b>	- Using Wire-OR Ties in ECLinPS Designs
<b>AN1672</b>	- The ECL Translator Guide
<b>AND8001</b>	- Odd Number Counters Design
<b>AND8002</b>	- Marking and Date Codes
<b>AND8020</b>	- Termination of ECL Logic Devices
<b>AND8090</b>	- AC Characteristics of ECL Devices

# MC100LVEL17

## PACKAGE DIMENSIONS


**SO-20L  
DW SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751D-05  
ISSUE F



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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