

# MC100LVEL17

## 3.3V ECL Quad Differential Receiver

The MC100LVEL17 is a 3.3 V ECL, quad differential receiver. The device is functionally equivalent to the E116 device with the capability of operation from either a -3.3 V or +3.3 V supply voltage.

Under open input conditions, the  $\overline{D}$  input will be biased at  $V_{CC}/2$  and the D input will be pulled down to  $V_{EE}$ . This operation will force the Q output LOW and ensure stability.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

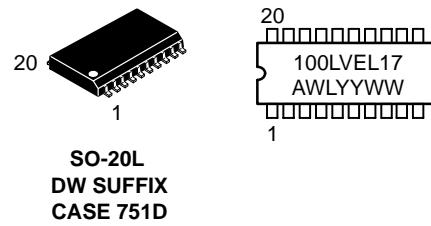
- 325 ps Propagation Delay
- High Bandwidth Output Transitions
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to -3.8 V
- Internal Input Pulldown Resistors D Inputs; Pullup and Pulldown on  $\overline{D}$  Inputs
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$



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### MARKING DIAGRAM\*



SO-20L  
DW SUFFIX  
CASE 751D

A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

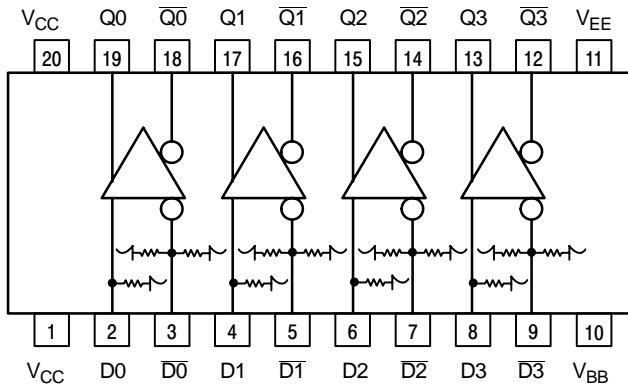
\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

| Device          | Package | Shipping <sup>†</sup> |
|-----------------|---------|-----------------------|
| MC100LVEL17DW   | SO-20L  | 38 Units/Rail         |
| MC100LVEL17DWR2 | SO-20L  | 1000 Tape & Reel      |

<sup>†</sup>For additional tape and reel information, refer to Brochure BRD8011/D.

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\* All V<sub>CC</sub> pins are tied together on the die.

Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Logic Diagram and Pinout: (Top View)**

## PIN DESCRIPTION

| PIN                          | FUNCTION                      |
|------------------------------|-------------------------------|
| D <sub>n</sub> , $\bar{D}_n$ | ECL Differential Data Inputs  |
| Q <sub>n</sub> , $\bar{Q}_n$ | ECL Differential Data Outputs |
| V <sub>BB</sub>              | Reference Voltage Output      |
| V <sub>CC</sub>              | Positive Supply               |
| V <sub>EE</sub>              | Negative Supply               |

## ATTRIBUTES

| Characteristics   | Value   |
|---|---|
| Internal Input Pulldown Resistor                              | 75 k $\Omega$   |
| Internal Input Pullup Resistor                                | 75 k $\Omega$   |
| ESD Protection  | Human Body Model<br>Machine Model<br>Charged Device Model |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Level 1   |
| Flammability Rating   | Oxygen Index: 28 to 34                                    |
| Transistor Count  | 141   |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |   |

1. For additional information, see Application Note AND8003/D.

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## MAXIMUM RATINGS (Note 2)

| Symbol        | Parameter  | Condition 1                      | Condition 2                            | Rating            | Units        |
|---------------|--|----------------------------------|--|-------------------|--------------|
| $V_{CC}$      | PECL Mode Power Supply                             | $V_{EE} = 0$ V                   |  | 8 to 0            | V            |
| $V_{EE}$      | NECL Mode Power Supply                             | $V_{CC} = 0$ V                   |  | -8 to 0           | V            |
| $V_I$         | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0$ V<br>$V_{CC} = 0$ V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6 to 0<br>-6 to 0 | V<br>V       |
| $I_{out}$     | Output Current                                     | Continuous<br>Surge              |  | 50<br>100         | mA<br>mA     |
| $I_{BB}$      | $V_{BB}$ Sink/Source                               |                                  |  | $\pm 0.5$         | mA           |
| TA            | Operating Temperature Range                        |                                  |  | -40 to +85        | °C           |
| $T_{stg}$     | Storage Temperature Range                          |                                  |  | -65 to +150       | °C           |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 LFPM<br>500 LFPM               | SO-20L<br>SO-20L                       | 90<br>60          | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | Standard Board                   | SO-20L                                 | 30 to 35          | °C/W         |
| $T_{sol}$     | Wave Solder  | <2 to 3 sec @ 248°C              |  | 265               | °C           |

2. Maximum Ratings are those values beyond which device damage may occur.

## LVPECL DC CHARACTERISTICS $V_{CC} = 3.3$ V; $V_{EE} = 0.0$ V (Note 3)

| Symbol      | Characteristic   | -40 °C       |      |      | 25°C |      |      | 85°C |      |      | Unit |
|-------------|--|--------------|------|------|------|------|------|------|------|------|------|
|             |  | Min          | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| $I_{EE}$    | Power Supply Current   |              | 26   | 31   |      | 26   | 31   |      | 27   | 33   | mA   |
| $V_{OH}$    | Output HIGH Voltage (Note 4)                                 | 2215         | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV   |
| $V_{OL}$    | Output LOW Voltage (Note 4)                                  | 1470         | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV   |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                            | 2135         |      | 2420 | 2135 |      | 2420 | 2135 |      | 2420 | mV   |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                             | 1490         |      | 1825 | 1490 |      | 1825 | 1490 |      | 1825 | mV   |
| $V_{BB}$    | Output Voltage Reference                                     | 1.92         |      | 2.04 | 1.92 |      | 2.04 | 1.92 |      | 2.04 | V    |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 5) |              |      |      |      |      |      |      |      |      |      |
|             |  | Vpp < 500 mV | 1.3  |      | 2.9  | 1.2  |      | 2.9  | 1.2  |      | V    |
| $I_{IH}$    | Input HIGH Current   |              |      | 150  |      |      | 150  |      |      | 150  | μA   |
|             |  | Dn           | 0.5  |      | 0.5  |      | 0.5  |      |      |      | μA   |
| $I_{IL}$    | Input LOW Current  | Dn           | -300 |      | -300 |      | -300 |      |      |      | μA   |
|             |  | Dn           |      |      |      |      |      |      |      |      | μA   |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3$  V.
4. Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.
5.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

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## LVNECL DC CHARACTERISTICS $V_{CC} = 0.0$ V; $V_{EE} = -3.3$ V (Note 6)

| Symbol      | Characteristic   | -40 °C          |        |        | 25°C   |        |        | 85°C   |        |        | Unit |
|-------------|--|-----------------|--------|--------|--------|--------|--------|--------|--------|--------|------|
|             |  | Min             | Typ    | Max    | Min    | Typ    | Max    | Min    | Typ    | Max    |      |
| $I_{EE}$    | Power Supply Current   |                 | 26     | 31     |        | 26     | 31     |        | 27     | 33     | mA   |
| $V_{OH}$    | Output HIGH Voltage (Note 7)                                 | - 1085          | - 1005 | - 880  | - 1025 | - 955  | - 880  | - 1025 | - 955  | - 880  | mV   |
| $V_{OL}$    | Output LOW Voltage (Note 7)                                  | - 1830          | - 1695 | - 1555 | - 1810 | - 1705 | - 1620 | - 1810 | - 1705 | - 1620 | mV   |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                            | - 1165          |        | - 880  | - 1165 |        | - 880  | - 1165 |        | - 880  | mV   |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                             | - 1810          |        | - 1475 | - 1810 |        | - 1475 | - 1810 |        | - 1475 | mV   |
| $V_{BB}$    | Output Voltage Reference                                     | - 1.38          |        | - 1.26 | - 1.38 |        | - 1.26 | - 1.38 |        | - 1.26 | V    |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 8) |                 |        |        |        |        |        |        |        |        |      |
|             | $V_{pp} < 500$ mV  | - 2.0           |        | - 0.4  | - 2.1  |        | - 0.4  | - 2.1  |        | - 0.4  | V    |
| $I_{IH}$    | Input HIGH Current   |                 |        | 150    |        |        | 150    |        |        | 150    | μA   |
|             | Input LOW Current  | Dn              | 0.5    |        |        | 0.5    |        |        | 0.5    |        | μA   |
|             |  | $\overline{Dn}$ | - 300  |        |        | - 300  |        |        | - 300  |        | μA   |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3$  V.
7. Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.
8.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{pp\min}$  and 1 V.

## AC CHARACTERISTICS $V_{CC} = 3.3$ V; $V_{EE} = 0.0$ V or $V_{CC} = 0.0$ V; $V_{EE} = -3.3$ V (Note 9)

| Symbol                 | Characteristic   | -40 °C       |            |                 | 25°C       |            |                 | 85°C       |            |                 | Unit       |    |
|------------------------|--|--------------|------------|-----------------|------------|------------|-----------------|------------|------------|-----------------|------------|----|
|                        |  | Min          | Typ        | Max             | Min        | Typ        | Max             | Min        | Typ        | Max             |            |    |
| $f_{max}$              | Maximum Toggle Frequency   |              |            |                 |            | 1.75       |                 |            |            |                 | GHz        |    |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>D to Q  | Diff<br>S.E. | 330<br>280 |                 | 530<br>580 | 350<br>300 |                 | 550<br>600 | 360<br>310 |                 | 560<br>610 | ps |
| $t_{SKEW}$             | Skew<br>Output-to-Output (Note 10)<br>Part-to-Part (Diff) (Note 10)<br>Duty Cycle (Diff) (Note 11) |              |            | 75<br>200<br>25 |            |            | 75<br>200<br>25 |            |            | 75<br>200<br>25 | ps         |    |
| $t_{JITTER}$           | Random Clock Jitter (RMS)  |              |            |                 |            | 0.7        |                 |            |            |                 | ps         |    |
| $V_{PP}$               | Input Swing (Note 12)  | 150          |            | 1000            | 150        |            | 1000            | 150        |            | 1000            | mV         |    |
| $t_r$<br>$t_f$         | Output Rise/Fall Times Q<br>(20% - 80%)  | 280          |            | 550             | 280        |            | 550             | 280        |            | 550             | ps         |    |

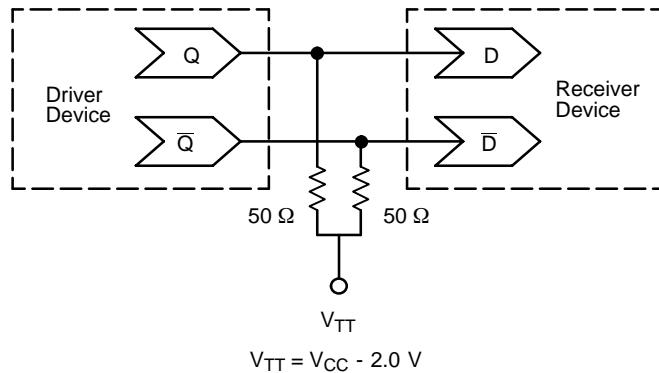
9.  $V_{EE}$  can vary  $\pm 0.3$  V.

10. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.

11. Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.

12.  $V_{pp\min}$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .

## MC100LVEL17



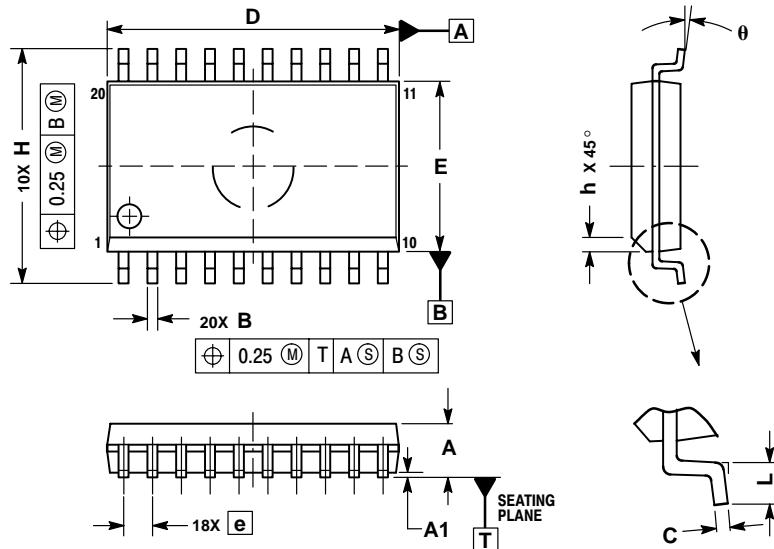
**Figure 2. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020 - Termination of ECL Logic Devices.)**

### Resource Reference of Application Notes

- AN1404** - ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** - ECL Clock Distribution Techniques
- AN1406** - Designing with PECL (ECL at +5.0 V)
- AN1503** - ECLinPS I/O SPICE Modeling Kit
- AN1504** - Metastability and the ECLinPS Family
- AN1560** - Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** - Interfacing Between LVDS and ECL
- AN1596** - ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** - Using Wire-OR Ties in ECLinPS Designs
- AN1672** - The ECL Translator Guide
- AND8001** - Odd Number Counters Design
- AND8002** - Marking and Date Codes
- AND8020** - Termination of ECL Logic Devices
- AND8090** - AC Characteristics of ECL Devices

## PACKAGE DIMENSIONS

**SO-20L**  
**DW SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751D-05**  
**ISSUE F**



## NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| MILLIMETERS |          |       |
|-------------|----------|-------|
| DIM         | MIN      | MAX   |
| A           | 2.35     | 2.65  |
| A1          | 0.10     | 0.25  |
| B           | 0.35     | 0.49  |
| C           | 0.23     | 0.32  |
| D           | 12.65    | 12.95 |
| E           | 7.40     | 7.60  |
| e           | 1.27 BSC |       |
| H           | 10.05    | 10.55 |
| h           | 0.25     | 0.75  |
| L           | 0.50     | 0.90  |
| θ           | 0 °      | 7 °   |

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