



AZ100LVEL16VT ARIZONA MICROTEK, INC.

ECL/PECL Oscillator Gain Stage & Buffer with Selectable Enable

FEATURES

- High Bandwidth for $\geq 1\text{GHz}$
- **Similar Operation as AZ100LVEL16VR Except in Disabled Condition: Q_{HG} is High**
- Operating Range of 3.0V to 5.5V
- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Available in a 3x3 mm or 2x2 mm MLP Package

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
MLP 8	AZ100LVEL16VTNA	TNA
MLP 8 T&R	AZ100LVEL16VTNAR1	TNA
MLP 8	AZ100LVEL16VTNB	TNB
MLP 8 T&R	AZ100LVEL16VTNBR1	TNB
MLP 8	AZ100LVEL16VTNC	TNC
MLP 8 T&R	AZ100LVEL16VTNCR1	TNC
MLP 16	AZ100LVEL16VTL	AZM16T
MLP 16 T&R	AZ100LVEL16VTLR1	AZM16T
MLP 16 T&R	AZ100LVEL16VTLR2	AZM16T
DIE	AZ100LVEL16VTX	N/A

DESCRIPTION

The AZ100LVEL16VT is a specialized oscillator gain stage with high gain output buffer including an enable. The $Q_{HG}/\bar{Q}_{HG}$ outputs have a voltage gain several times greater than the $Q/\bar{Q}$ outputs.

MLP 16, 3x3 mm Package (VTL) or DIE (VTX)

The AZ100LVEL16VTL and AZ100LVEL16VTX provide a selectable enable input (EN) that allows continuous oscillator operation. See truth table for the Enable function. If Enable pull-up is desired in the CMOS/TTL mode, an external $\leq 20\text{ k}\Omega$ resistor connecting EN to V_{CC} will override the on-chip pull-down resistor. When disabled, the Q_{HG} output is forced high and the $\bar{Q}_{HG}$ output is forced low. The AZ100LVEL16VTL/VTX also provides a V_{BB} and $470\ \Omega$ internal bias resistors from D to V_{BB} and $\bar{D}$ to V_{BB} . The V_{BB} pin can support 1.5 mA sink/source current. Bypassing V_{BB} to ground with a $0.01\ \mu\text{F}$ capacitor is recommended.

The outputs Q and $\bar{Q}$ each have a selectable on-chip pull-down current source. See truth table below for current source functions. External resistors may also be used to increase pull-down current to a maximum total of 25 mA.

Outputs Q_{HG} and $\bar{Q}_{HG}$ each have an optional on-chip pull-down current source of 10 mA. When pad/pin V_{EEP} is left open (NC), the output current sources are disabled and the $Q_{HG}/\bar{Q}_{HG}$ operate as standard PECL/ECL. When V_{EEP} is connected to V_{EE} , the current sources are activated. The $Q_{HG}/\bar{Q}_{HG}$ pull-down current can be decreased, by using a resistor to connect V_{EEP} to V_{EE} . (See graph on page 5.)

MLP 8, 2x2 mm Package, VTNA, VTNB & VTNC Versions

All MLP 8, 2x2mm versions of the AZ100LVEL16VT provide an enable input that allows continuous oscillator operation. VTNA and VTNB utilize an enable ($\bar{EN}$) that operates in the PECL/ECL mode. When the $\bar{EN}$ input is LOW, the $\bar{Q}$ and $Q_{HG}/\bar{Q}_{HG}$ outputs follow the data inputs. When $\bar{EN}$ is HIGH, the Q_{HG} output is forced high and the $\bar{Q}_{HG}$ output is forced low. VTNC utilizes an enable (EN) that operates in the CMOS/TTL mode. When the EN input is HIGH, the $\bar{Q}$ and $Q_{HG}/\bar{Q}_{HG}$ outputs follow the data inputs. When EN is LOW, the Q_{HG} output is forced high and the $\bar{Q}_{HG}$ output is forced low.

For VTNA, both D and $\bar{D}$ inputs are brought out and tied to the V_{BB} pin through $470\ \Omega$ internal bias resistors. In VTNB and VTNC, the $\bar{D}$ input is internally tied directly to the V_{BB} pin and the D input is tied to the V_{BB} pin through a $470\ \Omega$ internal bias resistor. Bypassing V_{BB} to ground with a $0.01\ \mu\text{F}$ capacitor is recommended.

All MLP 8, 2x2mm versions (VTNA, VTNB & VTNC) have the Q, Q_{HG} , and $\bar{Q}_{HG}$ current sources disabled, while the $\bar{Q}$ output operates with a 4 mA current source to V_{EE} .

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

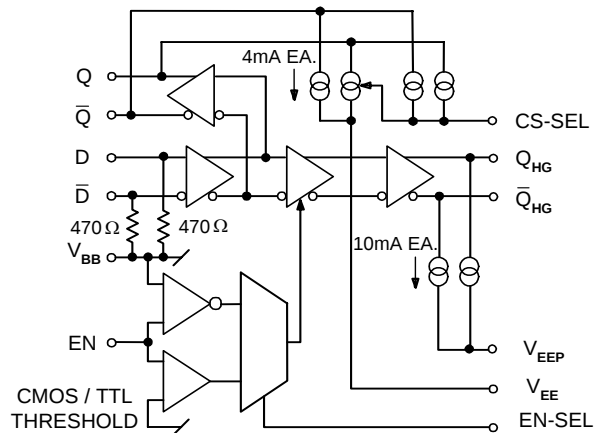
ENABLE TRUTH TABLE
MLP 16 (VTNL) or DIE (VTNX)

EN-SEL	EN	Q/Q̄	Q _{HG}	Q̄ _{HG}
NC	PECL Low, V _{EE} or NC	Data	Data	Data
NC	PECL High or V _{CC}	Data	High	Low
V _{EE} *	CMOS Low or V _{EE}	Data	High	Low
V _{EE} *	CMOS High or V _{CC}	Data	Data	Data
V _{EE} *	NC, no external pull-up	Data	High	Low
V _{EE} *	NC, with ≤20kΩ to V _{CC}	Data	Data	Data

*Connections to V_{CC} or V_{EE} must be less than 1Ω.

PIN DESCRIPTION

PIN	FUNCTION
D/D̄	Data Inputs
Q/Q̄	Data Outputs
Q _{HG} /Q̄ _{HG}	Data Outputs w/High Gain
V _{BB}	Reference Voltage Output
EN-SEL	Selects Enable Logic
EN/EN̄	Enable Input
CS-SEL	Selects Q and Q̄ Current Source Magnitude
V _{EEP}	Optional Q _{HG} and Q̄ _{HG} Current Sources
V _{EE}	Negative Supply
V _{CC}	Positive Supply



MLP 16 (VTNL) or DIE (VTNX)

CURRENT SOURCE TRUTH TABLE
MLP 16 (VTNL) or DIE (VTNX)

CS-SEL	Q	Q̄
NC	4mA typ.	4mA typ.
V _{EE} *	8mA typ.	8mA typ.
V _{CC} *	0	4mA typ.

*Connections to V_{CC} or V_{EE} must be less than 1Ω.

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V _{CC}	PECL Power Supply (V _{EE} = 0V)	0 to +8.0	Vdc
V _I	PECL Input Voltage (V _{EE} = 0V)	0 to +6.0	Vdc
V _{EE}	ECL Power Supply (V _{CC} = 0V)	-8.0 to 0	Vdc
V _I	ECL Input Voltage (V _{CC} = 0V)	-6.0 to 0	Vdc
I _{OUT}	Output Current Q _{HG} /Q̄ _{HG} --- Continuous	50	mA
	--- Surge	100	
	Output Current Q/Q̄ --- Continuous	25	
	--- Surge	50	
T _A	Operating Temperature Range	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

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100K ECL DC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$, $V_{CC} = GND$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ²	-1045	-835	-995	-835	-995	-835	-995	-835	mV
V_{OH}	Output HIGH Voltage ⁴	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V_{OL}	Output LOW Voltage ^{2,4}	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D/D, EN/EN (PECL) EN (CMOS/TTL)	-1165 $V_{EE}+2000$	-880 V_{CC}	-1165 $V_{EE}+2000$	-880 V_{CC}	-1165 $V_{EE}+2000$	-880 V_{CC}	-1165 $V_{EE}+2000$	-880 V_{CC}	mV
V_{IL}	Input LOW Voltage D/D, EN/EN (PECL) EN (CMOS/TTL)	-1810 V_{EE}	-1475 $V_{EE} + 800$	-1810 V_{EE}	-1475 $V_{EE} + 800$	-1810 V_{EE}	-1475 $V_{EE} + 800$	-1810 V_{EE}	-1475 $V_{EE} + 800$	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IL}	Input LOW Current EN ³	0.5		0.5		0.5		0.5		μA
I_{IH}	Input HIGH Current EN ³		150		150		150		150	μA
I_{EE}	Power Supply Current ¹		48		48		48		54	mA

1. Specified with V_{EEP} and CS-SEL open for VTL and VTX. Subtract 4mA for VTNA, VTNB & VTNC.
2. Specified with V_{EEP} and CS-SEL connected to V_{EE} for VTL and VTX only.
3. Specified with EN-SEL open for VTL and VTX only.
4. Specified with $Q_{HG}/\bar{Q}_{HG}$ connected with 50 Ω to $V_{CC} - 2V$ for VTNA, VTNB & VTNC.

100K LVPECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +3.3V$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ^{1,3}	2255	2465	2305	2465	2305	2465	2305	2465	mV
V_{OH}	Output HIGH Voltage ^{1,5}	2215	2420	2275	2420	2275	2420	2275	2420	mV
V_{OL}	Output LOW Voltage ^{1,3,5}	1375	1745	1400	1655	1480	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage D/D, EN/EN (PECL) ¹ EN (CMOS/TTL)	2135 2000	2420 V_{CC}	2135 2000	2420 V_{CC}	2135 2000	2420 V_{CC}	2135 2000	2420 V_{CC}	mV
V_{IL}	Input LOW Voltage D/D, EN/EN (PECL) ¹ EN (CMOS/TTL)	1490 GND	1825 800	1490 GND	1825 800	1490 GND	1825 800	1490 GND	1825 800	mV
V_{BB}	Reference Voltage ¹	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IL}	Input LOW Current EN ⁴	0.5		0.5		0.5		0.5		μA
I_{IH}	Input HIGH Current EN ⁴		150		150		150		150	μA
I_{EE}	Power Supply Current ²		48		48		48		54	mA

1. For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with V_{EEP} and CS-SEL open for VTL and VTX. Subtract 4mA for VTNA, VTNB & VTNC.
3. Specified with V_{EEP} and CS-SEL connected to V_{EE} for VTL and VTX only.
4. Specified with EN-SEL open for VTL and VTX only.
5. Specified with $Q_{HG}/\bar{Q}_{HG}$ connected with 50 Ω to $V_{CC} - 2V$ for VTNA, VTNB & VTNC.

100K PECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +5.0V$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ^{1,3}	3955	4165	4005	4165	4005	4165	4005	4165	mV
V_{OH}	Output HIGH Voltage ^{1,5}	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage ^{1,3,5}	3075	3445	3100	3338	3100	3338	3100	3338	mV
V_{IH}	Input HIGH Voltage D/D, EN/EN (PECL) ¹ EN (CMOS/TTL)	3835 2000	4120 V_{CC}	3835 2000	4120 V_{CC}	3835 2000	4120 V_{CC}	3835 2000	4120 V_{CC}	mV
V_{IL}	Input LOW Voltage D/D, EN/EN (PECL) ¹ EN (CMOS/TTL)	3190 GND	3525 800	3190 GND	3525 800	3190 GND	3525 800	3190 GND	3525 800	mV
V_{BB}	Reference Voltage ¹	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IL}	Input LOW Current EN ⁴	0.5		0.5		0.5		0.5		μA
I_{IH}	Input HIGH Current EN ⁴		150		150		150		150	μA
I_{EE}	Power Supply Current ²		48		48		48		54	mA

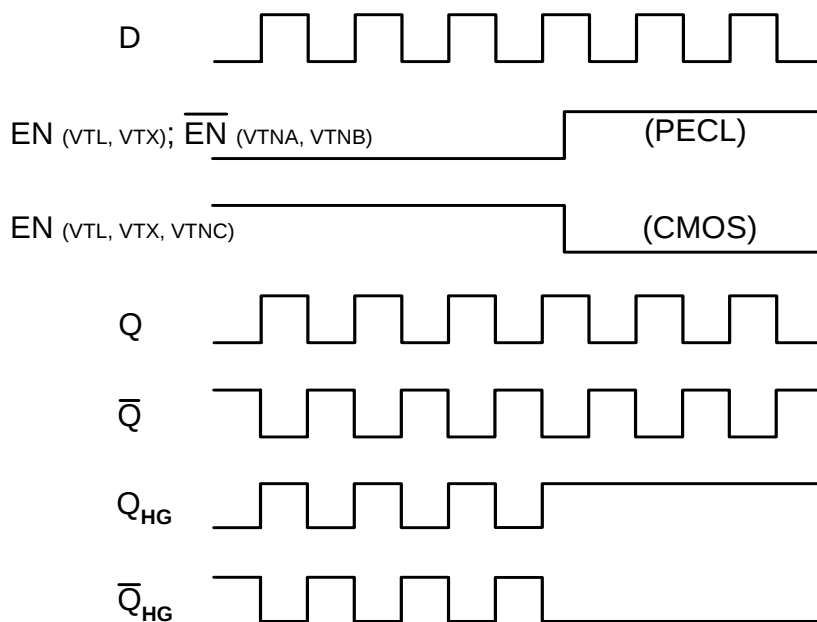
1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with V_{EEP} and CS-SEL open for VTL and VTX. Subtract 4mA for VTNA, VTNB & VTNC.
3. Specified with V_{EEP} and CS-SEL connected to V_{EE} for VTL and VTX only.
4. Specified with EN-SEL open for VTL and VTX only.
5. Specified with $Q_{HG}/\bar{Q}_{HG}$ connected with 50 Ω to $V_{CC} - 2V$ for VTNA, VTNB & VTNC.

AZ100LVEL16VT

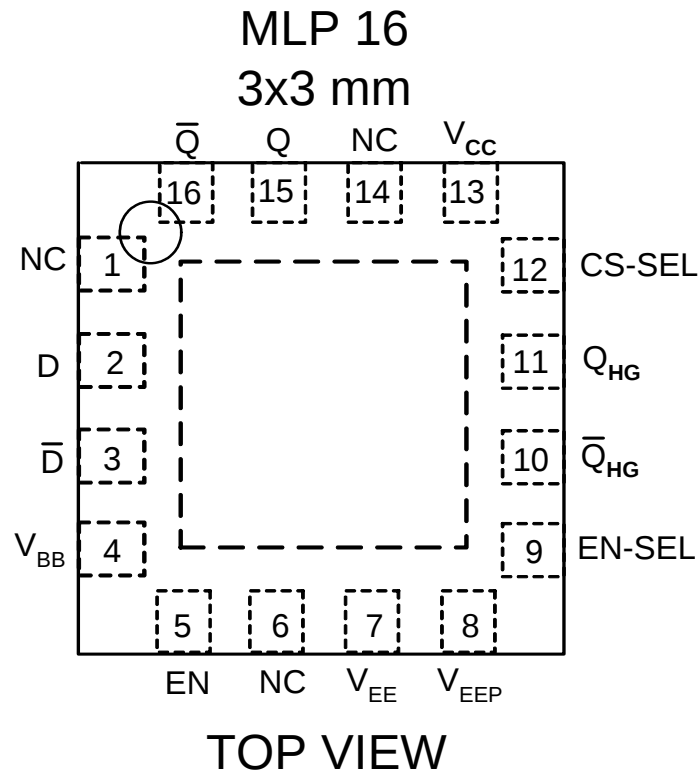
AC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$; $V_{CC} = GND$ or $V_{EE} = GND$; $V_{CC} = +3.0V$ to $+5.5V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay D to Q/ $\bar{Q}$ Outputs ¹ (SE) D to $Q_{HG}/\bar{Q}_{HG}$ Outputs ¹ (SE)			400 550			400 550			400 550			430 630	ps
t_{SKEW}	Duty Cycle Skew ² (SE)		5	20		5	20		5	20		5	20	ps
V_{PP}	Minimum Input Swing ³ DIFF SE	80 160			80 160			80 160			80 160			mV
t_r / t_f	Output Rise/Fall Times ¹ (20% - 80%)	100		260	100		260	100		260	100		260	ps

- For V_{TL} and V_{TX} , output specified with V_{EEP} and CS-SEL connected to V_{EE} with an AC coupled 50 Ω load. For $VTNA$, $VTNB$ & $VTNC$, AC coupled 50 Ω on $\bar{Q}$ to $V_{CC} - 2V$ and DC coupled 50 Ω to $V_{CC} - 2V$ on $Q_{HG}/\bar{Q}_{HG}$.
- Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
- V_{PP} is the minimum peak-to-peak input swing for which AC parameters guaranteed. The device has a voltage gain of ≈ 20 to Q/ $\bar{Q}$ outputs and a voltage gain of ≈ 100 to $Q_{HG}/\bar{Q}_{HG}$ outputs.

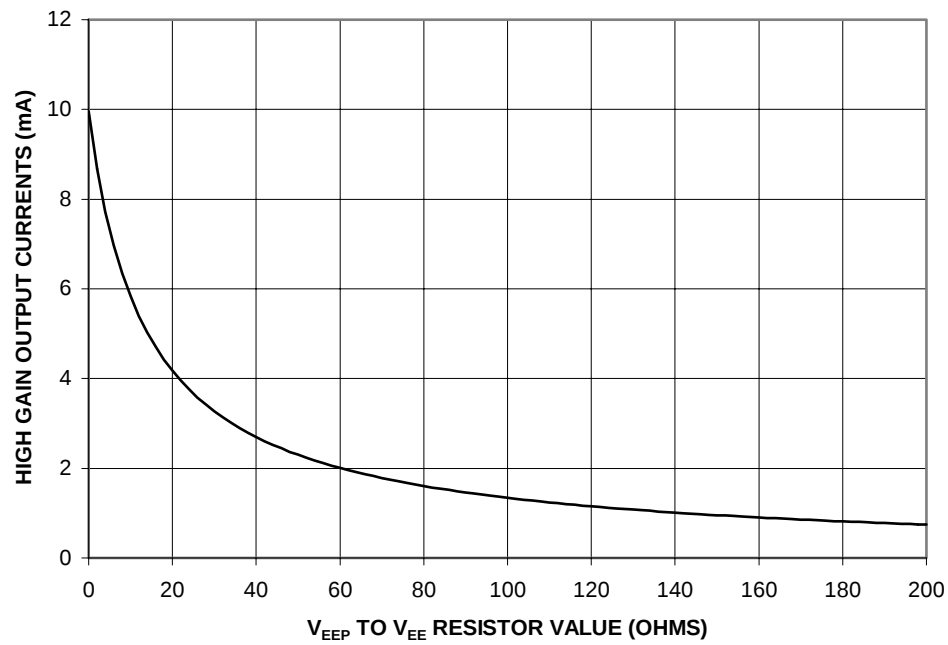


TIMING DIAGRAM

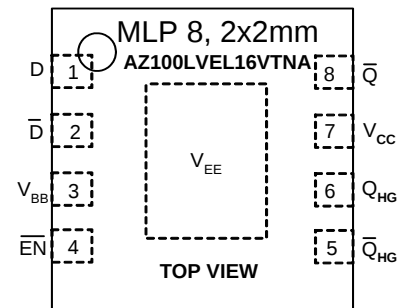
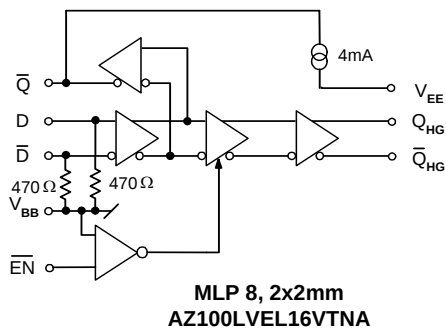


Bottom Center Pad may be left open or tied to V_{EE}

ADJUSTABLE HIGH GAIN OUTPUT CURRENT

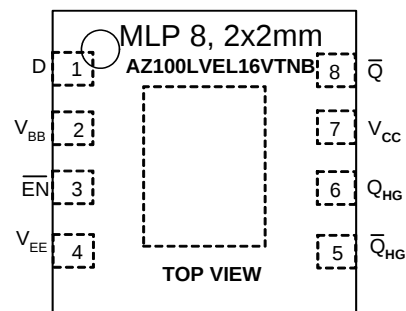
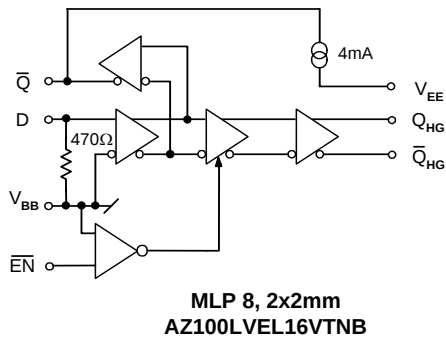


LOGIC DIAGRAMS AND PINOUTS FOR 2x2mm PACKAGE



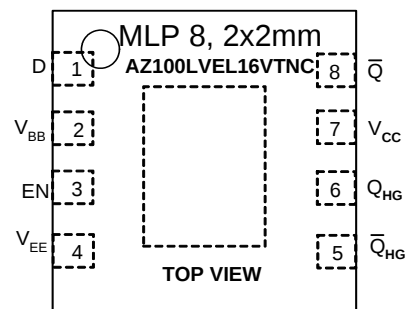
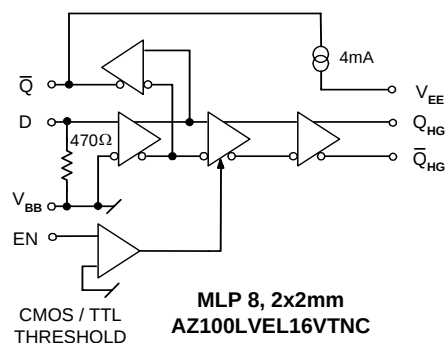
EN operation follows PECL functionality. See Timing Diagram above.

Bottom Center Pad is the V_{EE} return.



EN operation follows PECL functionality. See Timing Diagram above.

Bottom Center Pad may be left open or tied to V_{EE} . Pin 4 is the V_{EE} return.

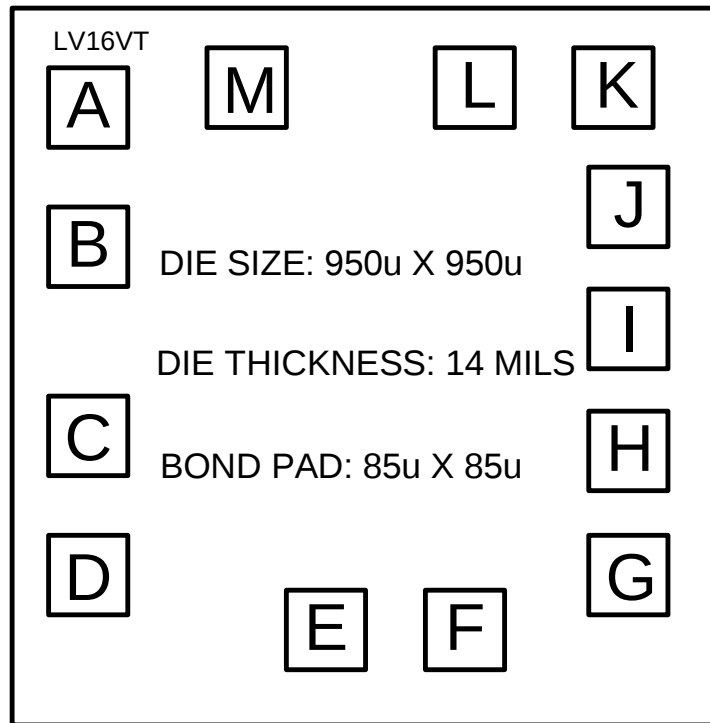


EN operation follows CMOS/TTL functionality. See Timing Diagram above.

Bottom Center Pad may be left open or tied to V_{EE} . Pin 4 is the V_{EE} return.

DIE PAD COORDINATES

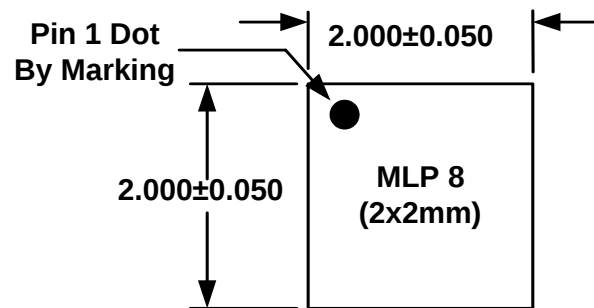
AZ100LVEL16VT DIE:



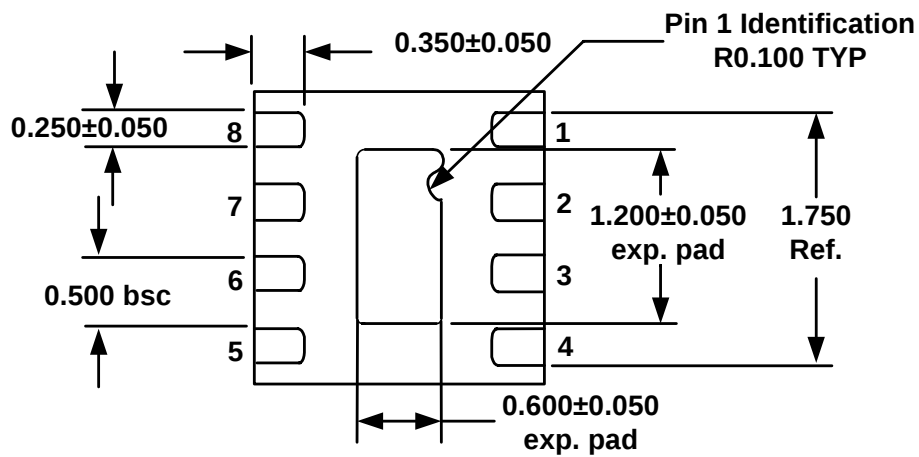
PAD CENTER COORDINATES

NAME	PAD DESIGNATION	X(Microns)	Y(Microns)
A	D	-342.5	312.5
B	$\bar{D}$	-342.5	144.5
C	V_{BB}	-342.5	-87.0
D	EN	-342.5	-255.0
E	V_{EE}	-33.5	-312.5
F	V_{EEP}	126.5	-312.5
G	EN-SEL	312.5	-248.5
H	$\bar{Q}_{HG}$	312.5	-98.5
I	Q_{HG}	312.5	51.5
J	CS-SEL	312.5	201.5
K	V_{CC}	302.5	342.5
L	Q	142.5	342.5
M	$\bar{Q}$	-140.5	342.5

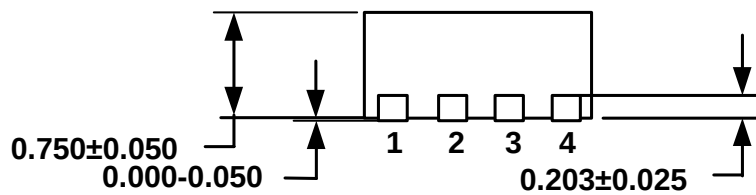
PACKAGE DIAGRAM
MLP 8 DUAL 2x2mm



TOP VIEW



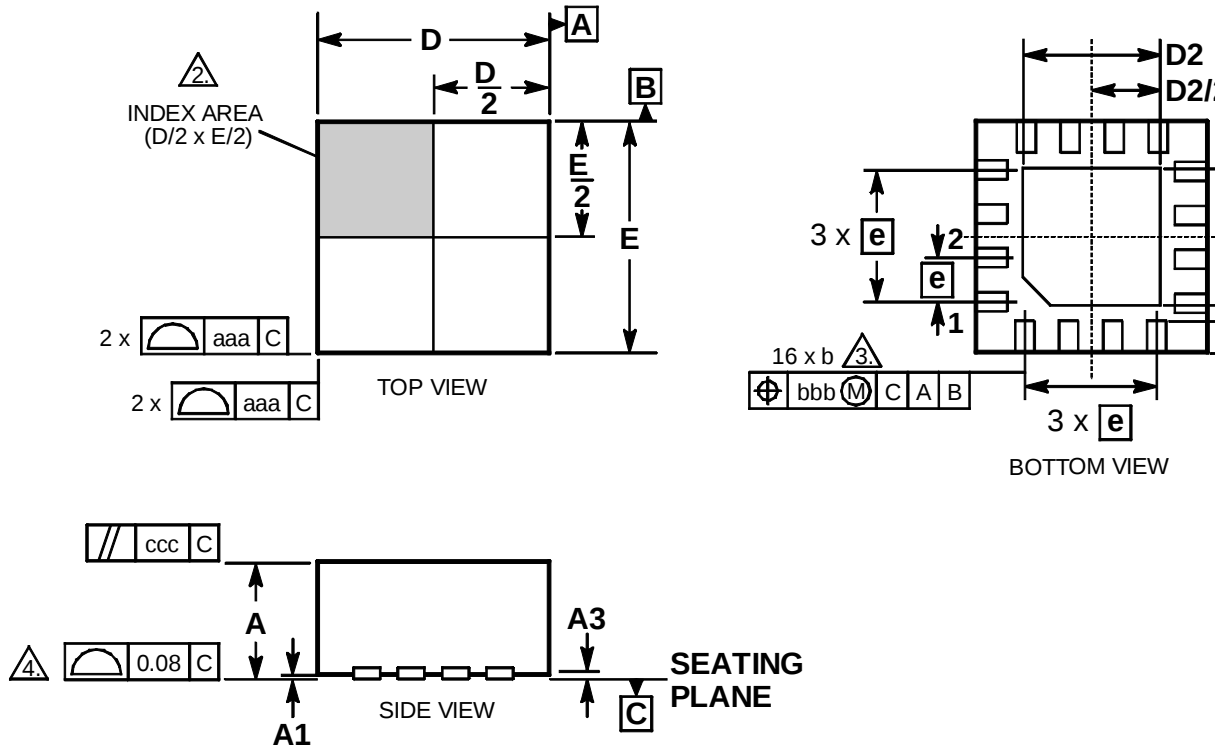
BOTTOM VIEW



SIDE VIEW

Note: All dimensions are in mm

**PACKAGE DIAGRAM
MLP 16**



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
- $\triangle 2$. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
- $\triangle 3$. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM THE PAD TIP.
- $\triangle 4$. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	

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