

- Member of the Texas Instruments Widebus™ Family
- Load Clock and Unload Clock Can Be Asynchronous or Coincident
- 256 Words by 18 Bits
- Low-Power Advanced CMOS Technology
- Full, Empty, and Half-Full Flags
- Programmable Almost-Full/Almost-Empty Flag
- Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously
- Data Rates up to 50 MHz
- 3-State Outputs
- Pin-to-Pin Compatible With SN74ACT7804 and SN74ACT7814
- Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Spacing

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7806 is a 256-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 256. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 128 or more words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or fewer words or (256 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (255 – Y) words.

DL PACKAGE
(TOP VIEW)

RESET	1	56	$\overline{\text{OE}}$
D17	2	55	Q17
D16	3	54	Q16
D15	4	53	Q15
D14	5	52	GND
D13	6	51	Q14
D12	7	50	V _{CC}
D11	8	49	Q13
D10	9	48	Q12
V _{CC}	10	47	Q11
D9	11	46	Q10
D8	12	45	Q9
GND	13	44	GND
D7	14	43	Q8
D6	15	42	Q7
D5	16	41	Q6
D4	17	40	Q5
D3	18	39	V _{CC}
D2	19	38	Q4
D1	20	37	Q3
D0	21	36	Q2
HF	22	35	GND
$\overline{\text{PEN}}$	23	34	Q1
AF/AE	24	33	Q0
LDCK	25	32	UNCK
NC	26	31	NC
NC	27	30	NC
FULL	28	29	$\overline{\text{EMPTY}}$

NC – No internal connection



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 **TEXAS
INSTRUMENTS**

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SN74ACT7806

256 × 18

STROBED FIRST-IN, FIRST-OUT MEMORY

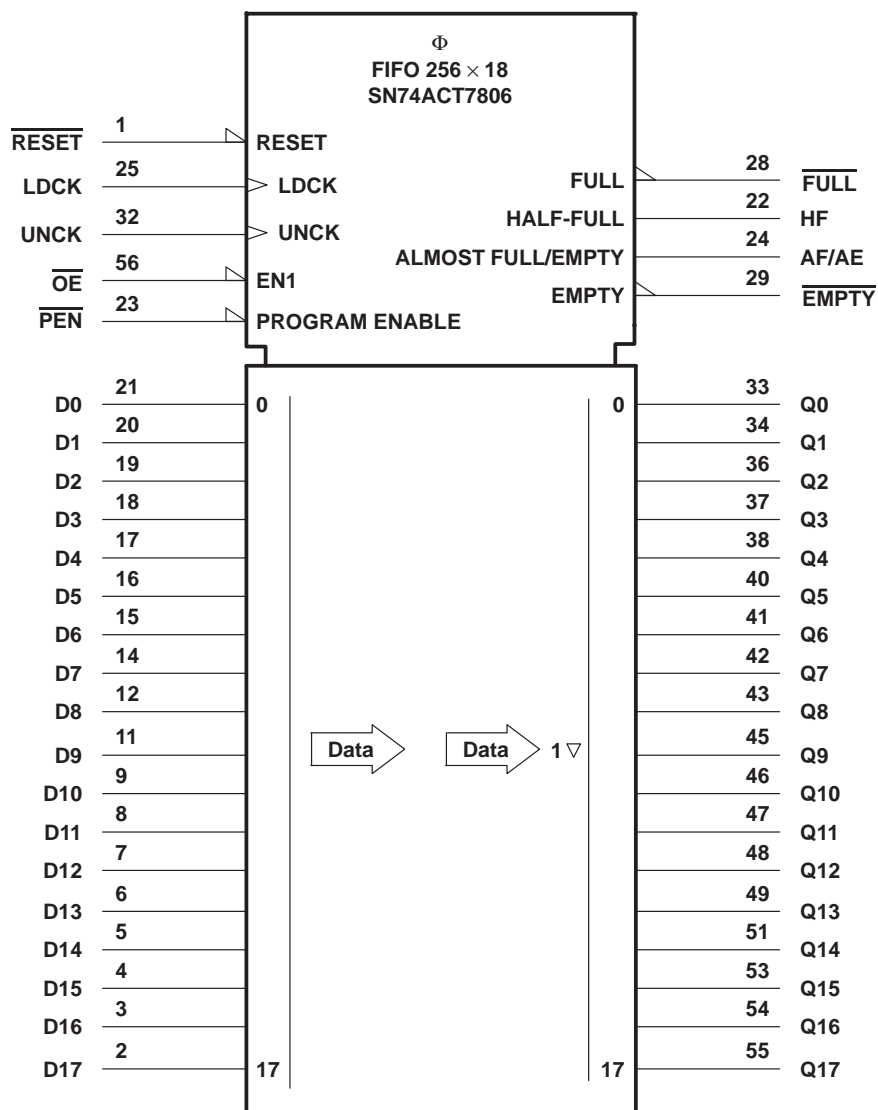
SCAS438C – APRIL 1992 – REVISED APRIL 1998

description (continued)

A low level on the reset ($\overline{\text{RESET}}$) input resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) input is high.

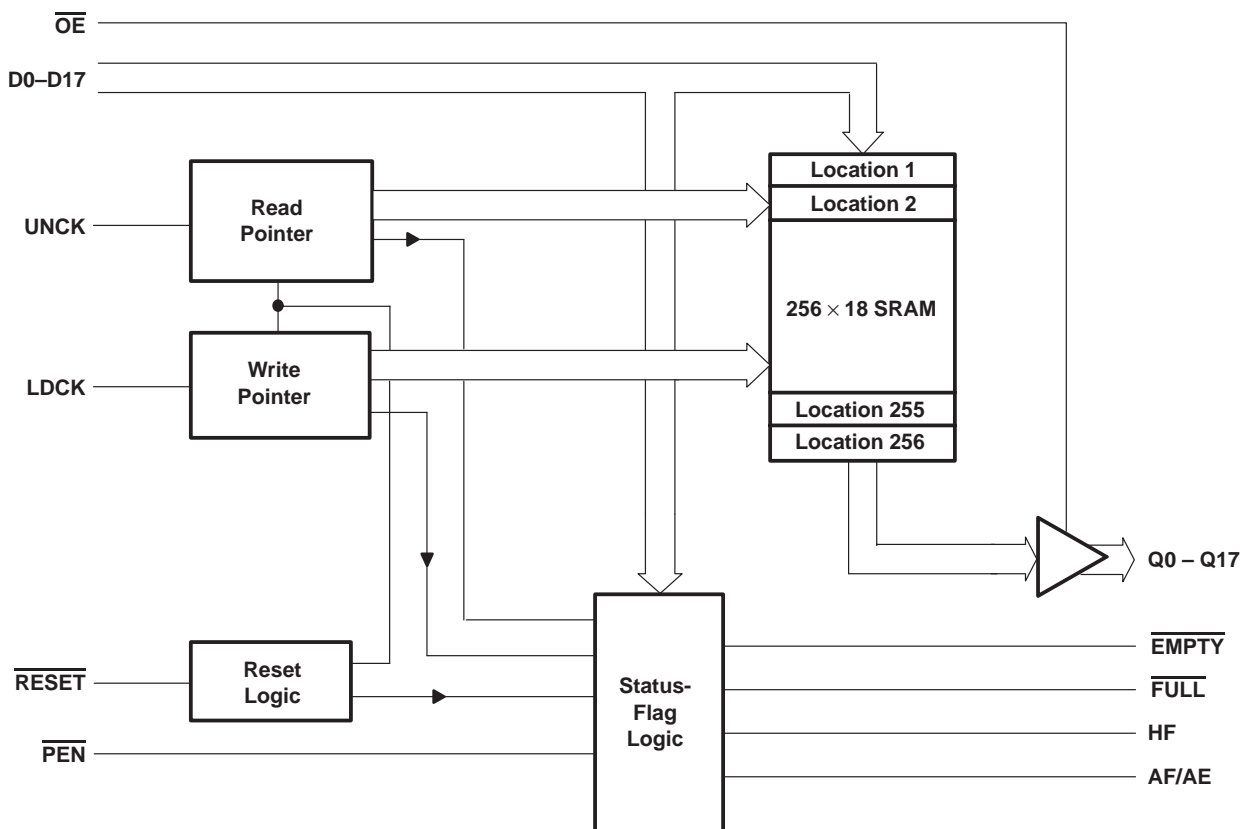
The SN74ACT7806 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth-offset values can be programmed for AF/AE, or the default value of 32 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or fewer words or (256 – Y) or more words. AF/AE is high after reset.
D0–D17	2–9, 11–12, 12–14	I	18-bit data input port
$\overline{\text{EMPTY}}$	29	O	Empty flag. $\overline{\text{EMPTY}}$ is high when the FIFO memory is not empty; $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty or upon assertion of $\overline{\text{RESET}}$.
$\overline{\text{FULL}}$	28	O	Full flag. $\overline{\text{FULL}}$ is high when the FIFO memory is not full or upon assertion of $\overline{\text{RESET}}$; $\overline{\text{FULL}}$ is low when the FIFO memory is full.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 128 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
$\overline{\text{OE}}$	56	I	Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D6 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on this input resets the FIFO and drives $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.

offset values for AF/AE

The AF/AE flag has two programmable limits, the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or fewer words or (256 – Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D6 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D6 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 127 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 32, $\overline{\text{PEN}}$ must be held high.

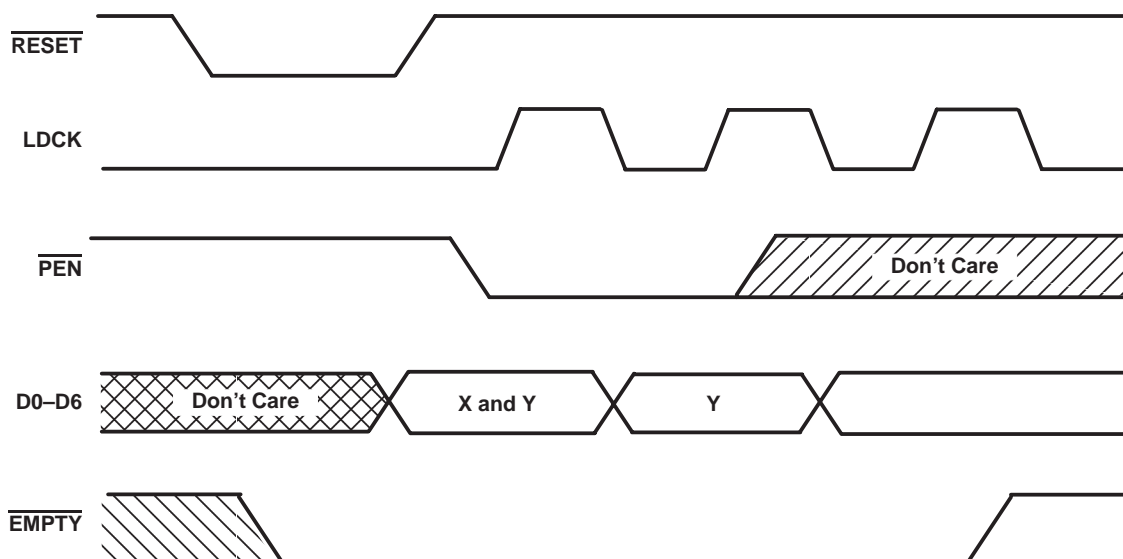
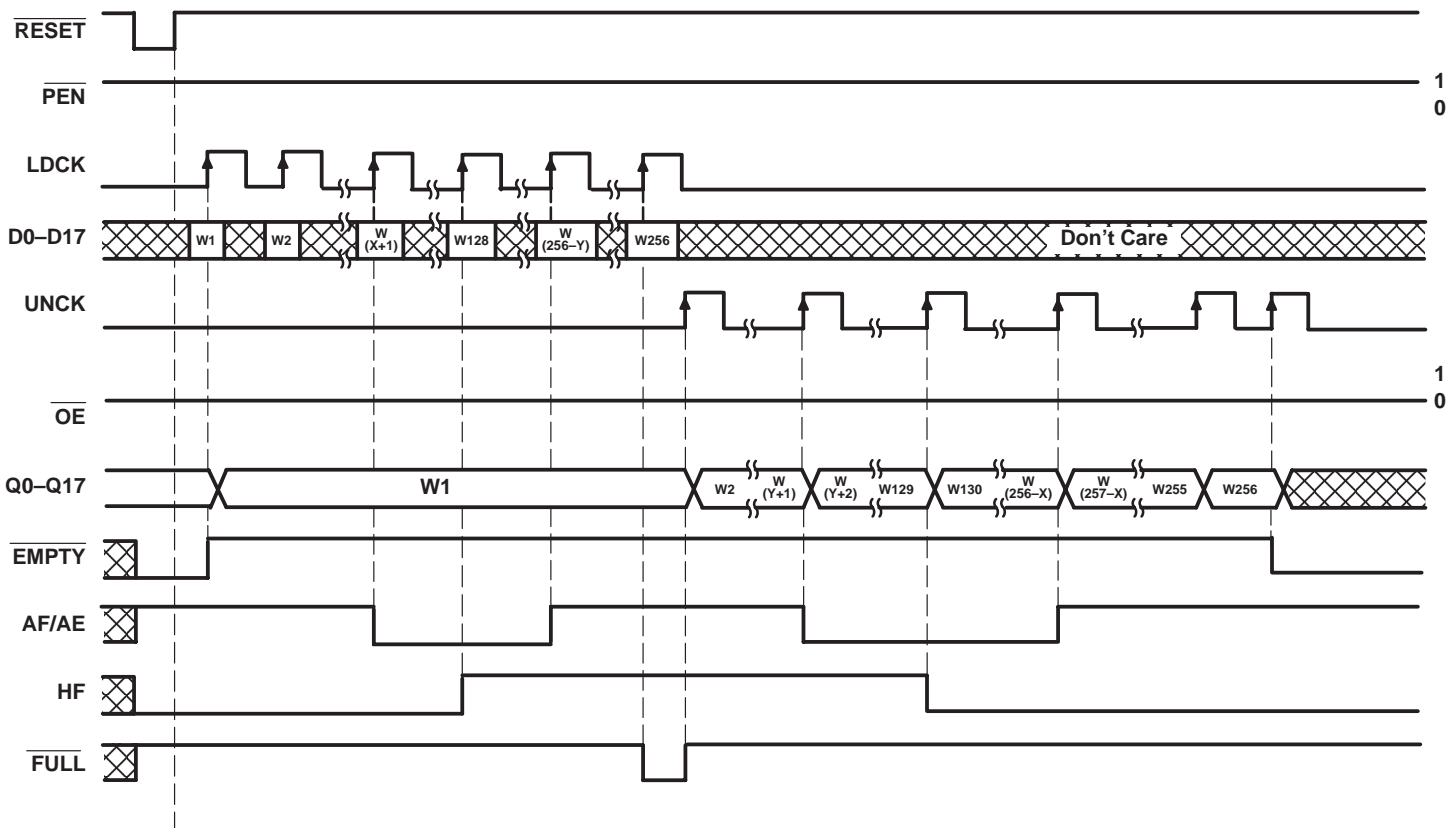


Figure 1. Programming X and Y Separately



Define the AF/AE Flag Using
the Default Value of X and Y

Figure 2. Write, Read, and Flag Timing Reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I	–0.5 V to 7 V
Voltage range applied to a disabled 3-state output	–0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1)	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			'ACT7806-20		'ACT7806-25		'ACT7806-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2		2		V
V _{IL}	Low-level input voltage		0.8		0.8		0.8		V
I _{OH}	High-level output current	Q outputs, flags	−8		−8		−8		mA
I _{OL}	Low-level output current	Q outputs	16		16		16		mA
		Flags	8		8		8		
T _A	Operating free-air temperature		0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			V
V_{OL}	Flags	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 8\text{ mA}$			0.5	V
	Q outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 16\text{ mA}$			0.5	
I_I		$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or 0			±5	µA
I_{OZ}		$V_{CC} = 5.5\text{ V}$, $V_O = V_{CC}$ or 0			±5	µA
I_{CC}		$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC} - 0.2\text{ V}$ or 0			400	µA
$\Delta I_{CC}§$		$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND			1	mA
C_i		$V_I = 0$, $f = 1\text{ MHz}$		4		pF
C_o		$V_O = 0$, $f = 1\text{ MHz}$		8		pF

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

timing requirements over recommended operating conditions (see Figures 1 through 3)

			'ACT7806-20		'ACT7806-25		'ACT7806-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		50		40		25		MHz
t _w	Pulse duration	LDCK high or low	7		8		12		ns
		UNCK high or low	7		8		12		
		PEN low	7		8		12		
		RESET low	10		10		12		
t _{su}	Setup time	D0–D17 before LDCK↑	5		5		5		ns
		PEN before LDCK↑	5		5		5		
		LDCK inactive before RESET high	5		6		6		
t _h	Hold time	D0–D17 after LDCK↑	0		0		0		ns
		LDCK inactive after RESET high	5		6		6		
		PEN low after LDCK↑	3		3		3		
		PEN high after LDCK↓	0		0		0		

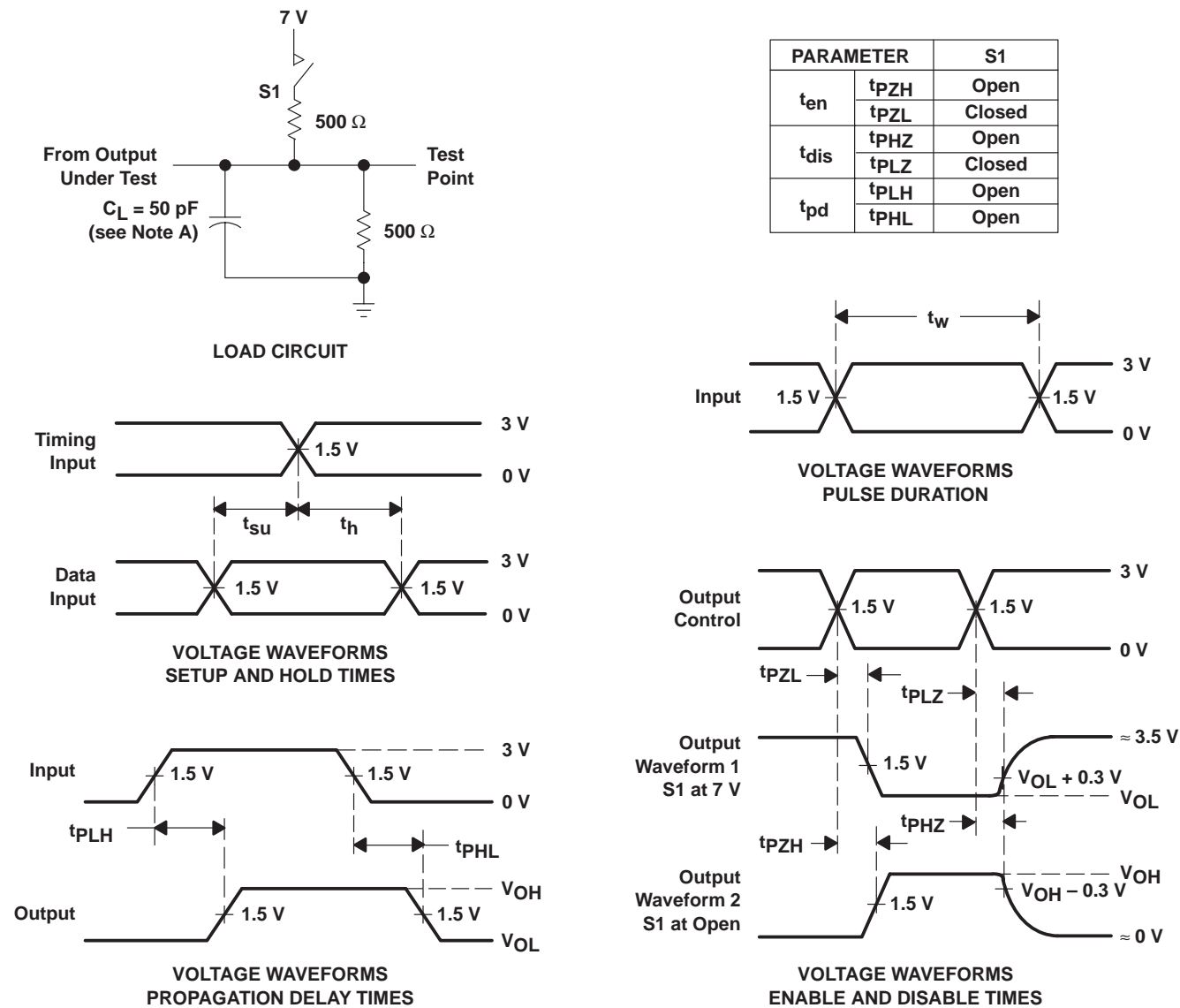
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figures 5 and 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7806-20			'ACT7806-25		'ACT7806-40		UNIT
			MIN	TYP \dagger	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		50			40		25		MHz
t_{pd}	LDCK \uparrow	Any Q	9		20	9	22	9	24	ns
	UNCK \uparrow		6	11.5	15	6	18	6	20	
t_{pd}^\ddagger	UNCK \uparrow	Any Q	10.5							ns
t_{PLH}	LDCK \uparrow	$\overline{\text{EMPTY}}$	6		15	6	17	6	19	ns
t_{PHL}	UNCK \uparrow	$\overline{\text{EMPTY}}$	6		15	6	17	6	19	ns
	$\overline{\text{RESET}}$ low		4		16	4	18	4	20	
	LDCK \uparrow	$\overline{\text{FULL}}$	6		15	6	17	6	19	
t_{PLH}	UNCK \uparrow	$\overline{\text{FULL}}$	6		15	6	17	6	19	ns
	$\overline{\text{RESET}}$ low		4		18	4	20	4	22	
t_{pd}	LDCK \uparrow	AF/AE	7		18	7	20	7	22	ns
	UNCK \uparrow		7		18	7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low	AF/AE	2		10	2	12	2	14	ns
	LDCK \uparrow	HF	5		18	5	20	5	22	
t_{PHL}	UNCK \uparrow	HF	7		18	7	20	7	22	ns
	$\overline{\text{RESET}}$ low		3		12	3	14	3	16	
t_{en}	$\overline{\text{OE}}$	Any Q	2		9	2	10	2	11	ns
t_{dis}	$\overline{\text{OE}}$	Any Q	2		10	2	11	2	12	ns

 \dagger All typical values are at $V_{\text{CC}} = 5$ V, $T_A = 25^\circ\text{C}$. \ddagger This parameter is measured at $C_L = 30$ pF (see Figure 4).operating characteristics, $V_{\text{CC}} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	$C_L = 50$ pF, $f = 5$ MHz	53	pF

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

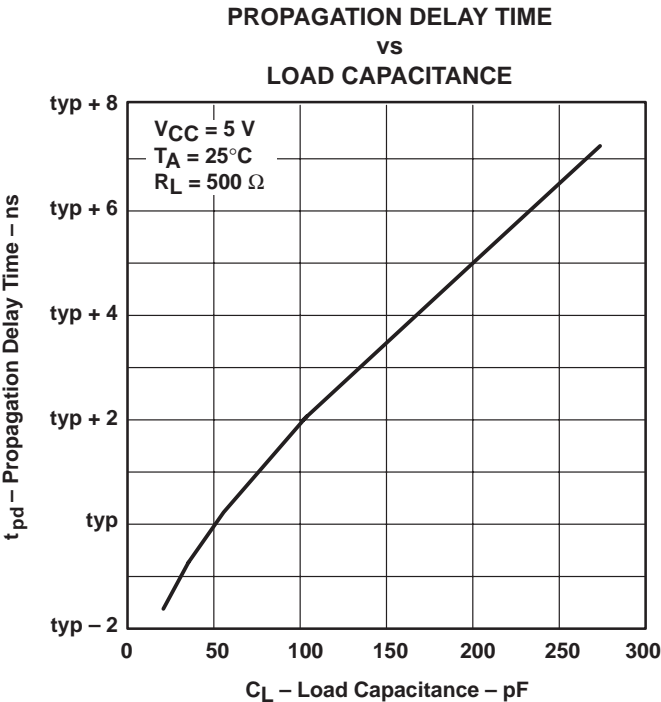


Figure 4

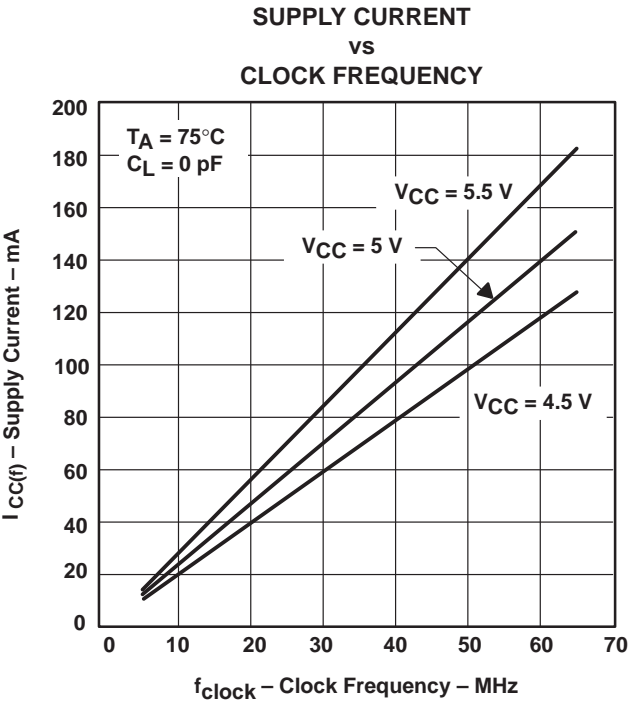


Figure 5

APPLICATION INFORMATION

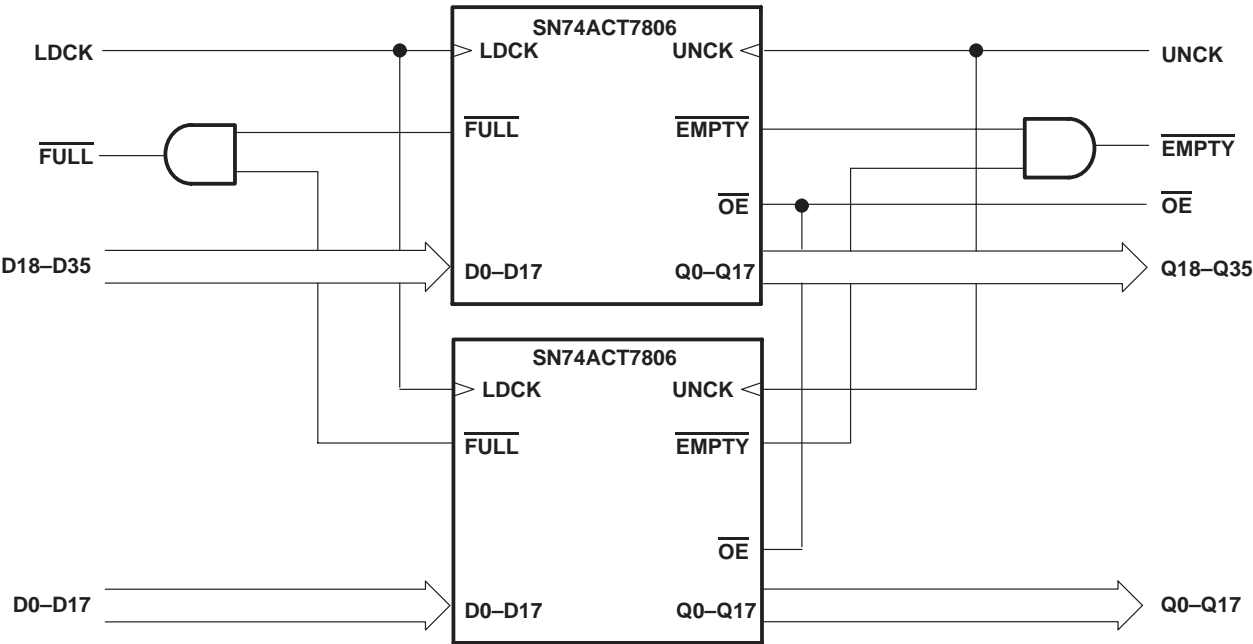


Figure 6. Word-Width Expansion: 256 × 36 Bits

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ACT7806-20DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT7806-20
SN74ACT7806-20DL.A	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT7806-20
SN74ACT7806-40DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT7806-40
SN74ACT7806-40DL.A	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT7806-40

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ACT7806-20DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ACT7806-20DL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ACT7806-40DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ACT7806-40DL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

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