UM10403

90 Watt notebook adapter with TEA1752T and TEA1791T

Rev. 01 — 28 May 2010 **User manual**

Document information

Info	Content
Keywords	GreenChip III, TEA1752T, GreenChip SR, TEA1791T, PFC, flyback, synchronous rectification, high efficiency, adapter, notebook, PC power
Abstract	This manual provides the specification, performance, schematics, bill of materials and PCB layout of a 90 W notebook adapter using the TEA1752T and TEA1791T. For design details on the TEA1752T and TEA1791T please refer to the application notes.

Revision history

Rev	Date	Description
01	28 May 2010	First Draft

Contact information

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1. Introduction

WARNING

Lethal voltage and fire ignition hazard

The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire.

This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel that is qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

This manual describes a universal input, 19.5 V, 4.62 A single output power supply using TEA1752T and TEA1791T devices from the GreenChip-III and GreenChip-SR family of NXP Semiconductors. It contains the specification of the power supply, circuit diagram, the component list to build the supply, the PCB layout and component positions, documentation of the PFC choke and transformer, along with test data and oscilloscope pictures of the most important waveforms.

The GreenChip-3 combines the control and drive for both the PFC and the flyback stages into a single device. The TEA1752T: provides complete SMPS control functionality to comply with the IEC61000-3-2 harmonic current emission requirements, obtain a significant reduction of components, save PCB space and give a cost benefit. It also offers extremely low power consumption in no-load mode, which makes it suitable for the low-power consumer markets. The built-in green functions ensure high efficiency at all power levels, which results in a design that can easily meet all existing and proposed energy efficiency standards such as: CoC (Europe), ENERGY STAR (US), CEC (California), MEPS (Australian and New Zealand), and CECP (China).

The GreenChip SR is a synchronous rectification control IC that needs no external components to tune the timing. Used in notebook adapter designs, the GreenChip SR offers a wide VCC operating range between 8.5 V and 38 V, minimizing the number of external components required and enabling simpler designs. In addition, the high driver output voltage (10 V) makes the GreenChip SR compatible with all brands of MOSFETs.

Fig 1. 90 W TEA1752T and TEA1791T demo board

2. Specification

- Mains input voltage: 90 V to 264 V; 47 Hz to 63 Hz
- DC output: 19.5 V; ±2 %
- Maximum continuous output current: 4.62 A
- Peak output current: ≥ 5.7 A
- Efficiency: > 88.5 % at maximum load
- ENERGY STAR active mode efficiency: > 89.5 %
- No load power consumption: ≤ 0.2 W
- Dynamic load response (peak-to-peak): 700 mV
- Output ripple and noise (peak-to-peak): 100 mV
- CISPR22 class B conducted EMI (−15 dB margin)
- EN61000-4-2 immunity against ESD (≥ ±12 kV air discharge)
- EN61000-3-2 A14 (harmonics) compliance
- Short Circuit Protection (SCP); input power < 1.2 W during SCP test
- OverCurrent Protection (OCP); input power < 2.2 W during OCP test
- Latched output OverVoltage Protection (OVP): < 24 V
- Latched OverTemperature Protection (OTP); ≤ 120 °C
- Fast Latch Reset (FLR): < 2 s

3. Performance data

3.1 Test setup

3.1.1 Test equipment

- AC source: Agilent 6812B
- Power meter: Yokogawa WT210 with Harmonics option
- DC electronic load: Chroma, Model 63103
- Digital oscilloscope: Yokogawa DL1640L
- Current probe Yokogawa 701933 30A; 50MHz
- 100 MHz, high voltage differential probe: Yokogawa 700924
- 500 MHz, low voltage differential probe: Yokogawa 701920
- Multimeter: Keithley 2000
- EMC receiver: Rohde & Schwarz ESPI-3 + LISN ENV216

3.1.2 Test conditions

- Adapter on the lab-table with the heat sinks downwards
- The adapter has no casing
- Ambient temperature between 20 °C and 25 °C
- Measurements were made after stabilization of temperature according to "test method for calculating the efficiency of single-voltage external AC-DC and AC-AC power supplies" of ENERGY STAR

3.2 Efficiency

3.2.1 ENERGY STAR efficiency

To market adapters as ENERGY STAR efficient they have to pass the active mode and no-load criteria as stated in the ENERGY STAR standard for External Power Supplies; EPS2.0. The minimum active-mode efficiency is defined as the arithmetic average efficiency at 25 %, 50 %, 75 % and 100 % of the rated output power as printed on the nameplate of the adapter.

3.2.1.1 Active mode efficiency

Test Conditions:

The adapter is set to maximum load and well pre-heated until temperature stabilization is achieved. Temperature stabilization is established for every load step before recording any measurements.

Remark: The output voltage is measured at the end of the output cable (2×20 mΩ).

Criteria to pass:

To comply with ENERGY STAR EPS2.0, the arithmetic average of the four efficiency measurements must be greater than, or equal to, 87 %. Universal mains adapters have to pass the criteria at both 115 V; 60 Hz and 230 V; 50 Hz. To meet this criteria, the PFC must be off at 25 % load and preferably on at 50 % load.

Table 1. Active mode efficiency at 115 V; 60 Hz

Load (%)	I_O (A)	V_O (V)	P_O (W)	P_I (W)	Efficiency (%)	Power factor
100	4.628	19.173	88.72	98.94	89.67	0.986
75	3.472	19.246	66.81	73.74	90.61	0.979
50	2.315	19.318	44.73	49.33	90.67	0.965
25	1.160	19.383	22.49	24.69	91.08	0.450
Average	-	-	-	-	90.51	-

Table 2. Active mode efficiency at 230 V; 50 Hz

Load (%)	I_O (A)	V_O (V)	P_O (W)	P_I (W)	Efficiency (%)	Power factor
100	4.628	19.175	88.73	98.41	90.17	0.945
75	3.472	19.247	66.82	74.31	89.92	0.921
50	2.316	19.319	44.73	50.49	88.60	0.878
25	1.160	19.385	22.49	24.75	90.87	0.378
Average	-	-	-	-	89.89	-

Table 3. PFC on and off level as a function of the mains input voltage

Mains supply V; Hz	90; 60	100; 50	115; 60	230; 50	264; 50
Output current (A) (PFC on)	1.75	1.83	1.88	1.91	1.86
Output current (A) (PFC off)	1.35	1.36	1.34	1.35	1.31

3.2.1.2 No-load input power

Test Conditions:

The adapter is set to maximum load and pre-heated. After 5 minutes the load is removed. The no-load input power measurements were recorded after stabilization of the input power reading.

Criteria to pass:

To comply with ENERGY STAR EPS2.0, the input power must be less than 0.5 W. Universal mains adapters have to pass the criteria at both 115 V; 60 Hz and 230 V; 50 Hz.

The adapter is set to maximum load and pre-heated. After 5 minutes the load is removed. The no-load input power measurements were recorded after stabilization of the input power reading.

Table 4. No-load input power

No-load input power as a function of the mains input voltage.

Mains supply V; Hz	90; 60	100; 50	115; 60	230; 50	264; 50
Input power P_I (W)	0.137	0.139	0.142	0.182	0.200

3.2.1.3 Full load efficiency PFC plus flyback stage

Test conditions:

Before any measurements were recorded, the adapter is set to maximum load and is preheated till the readings were stabilized.

Remark: The output voltage is measured at the end of the output cable. (2×20 mΩ)

Criteria to pass:

The efficiency (η) must be > 88 % at the maximum continuous output load.

Table 5. PFC plus flyback stage

Total converter efficiency (at full load) as a function of the mains input

Mains supply V; Hz	I_I RMS (A)	P_O (W)	P_I (W)	Efficiency (%)	Power factor
90; 60	1.130	88.74	100.24	88.53	0.989
100; 50	1.013	88.76	99.58	89.14	0.987
115; 60	0.877	88.72	98.94	89.67	0.986
230; 50	0.456	88.73	98.41	90.17	0.945
264; 50	0.402	88.66	98.26	90.24	0.929

3.3 Timing and protection

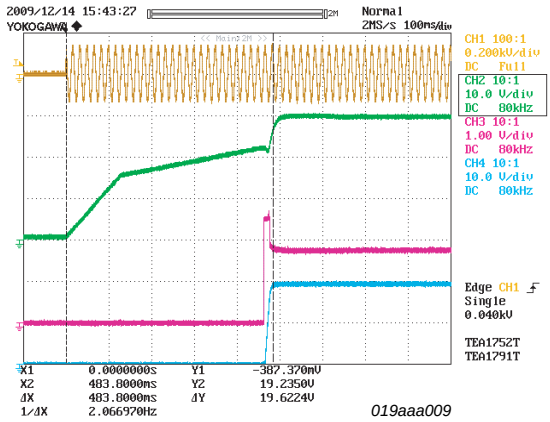
3.3.1 Switch-on delay and output rise time

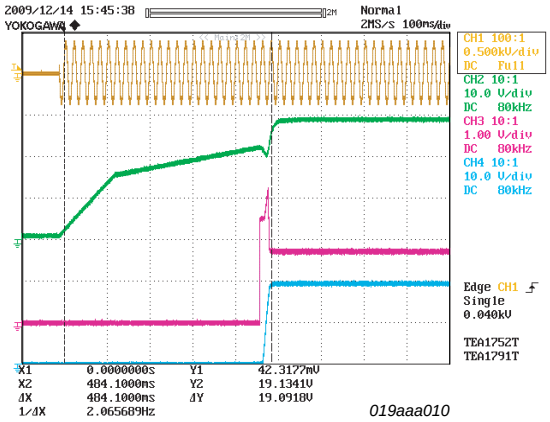
Test conditions:

The electronic load is set to Constant Current (CC) mode and V_{on} = 0 V. The electronic load is set to the maximum continuous output current.

Criteria to pass:

- Switch-on delay: two seconds maximum after the AC mains voltage is applied to the time when the output is within regulation
- Output rise time: The output voltage must rise from 10 % of the maximum to the regulation limit within 30 ms. There must be a smooth and continuous ramp-up of the output voltage. No voltage with a negative polarity must be present at the output during start-up
- No output bounce or hiccup is allowed during switch-on.
- There be must be sufficient margin between the FBCTRL signal and the 4.5 V time-out trigger level to avoid false triggering of the time-out protection due to component tolerances





a. Mains input 90 V; 60 Hz; delay time 484 ms

Load = 4.62 A

CH1: mains input

CH2: VCC pin TEA1752T

CH3:FBCTRL pin TEA1752T

CH4: output voltage

b. Mains input 264 V; 50 Hz; delay time 484 ms

Load = 4.62 A

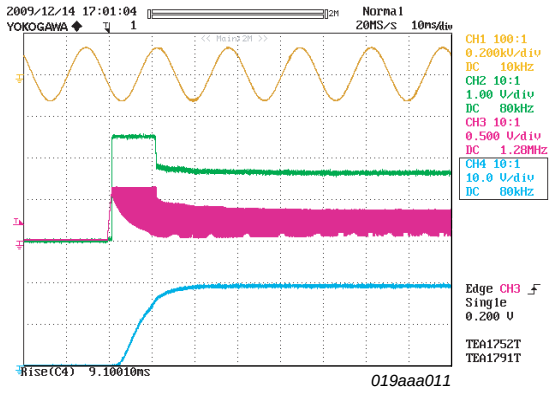
CH1: mains input

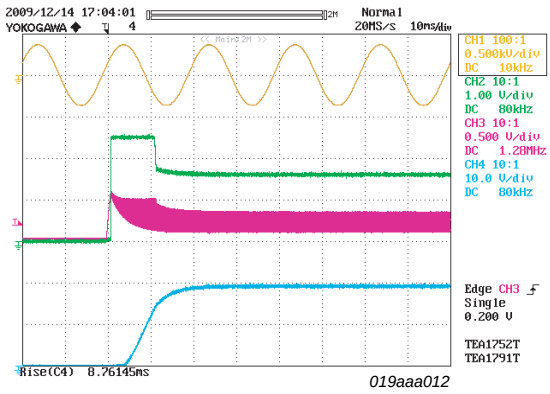
CH2: VCC pin TEA1752T

CH3: FBCTRL pin TEA1752T

CH4: output voltage

Fig 2. Delay between switch-on and output in regulation





a. Mains input 90 V; 60 Hz; output rise time 12.64 ms

Load = 4.63 A

CH1: mains input

CH2: FBCTRL pin TEA1752T

CH3: FBSENSE pin TEA1752T (soft start)

CH4: output voltage

b. Mains input 264 V; 50 Hz; output rise time 12.24 ms

Load = 4.63 A

CH1: mains input

CH2: VCC pin TEA1751T

CH3: FBSENSE pin TEA1751T (soft start)

CH4: output voltage

Fig 3. Output rise time at full load start-up

3.3.2 Brownout and brownout recovery

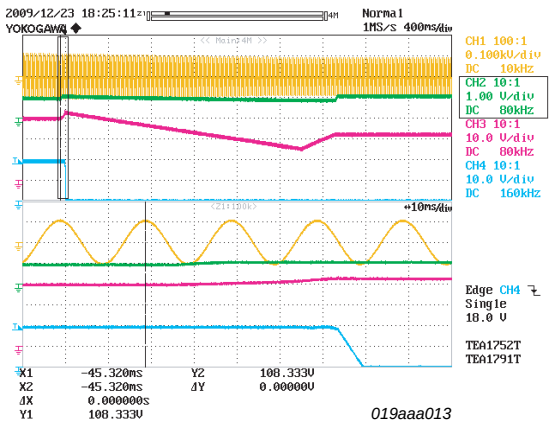
The voltage on the VINSENSE pin is monitored continuously to prevent the PFC from operating at very low mains input voltages.

Test Conditions:

The mains input voltage is decreased from 90 V down to 0 V and then increased from 0 V to 90 V. The electronic load is set to Constant Current (CC) mode and V_{on} = 0 V. The electronic load is set to the maximum continuous output current.

Criteria to pass:

- The adapter must survive the test without damage and excessive heating of component
- The output voltage must remain within the specified regulation limits or switch-off
- No output bounce or hiccup is allowed during switch-on or switch-off
- The adapter must power-up before the AC line input voltage reaches 85 V (maximum)



a. AC mains input from 90 V to 0 V

brownout voltage = $108/(\sqrt{2}) = 76$ V

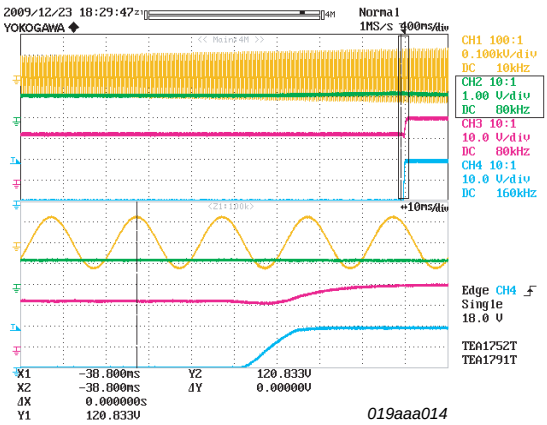
Load = 4.62 A

CH1: mains input

CH2: VINSENSE pin TEA1752T

CH3: VCC pin TEA1752T

CH4: output voltage



b. AC mains input from 0 V to 90 V

brownout recovery voltage = $121/(\sqrt{2}) = 86$ V)

Load = 4.62 A

CH1: mains input

CH2: VINSENSE pin TEA1752T

CH3: VCC pin TEA1752T

CH4: output voltage

Fig 4. Brownout and brownout recovery

3.3.3 Output short circuit protection

To protect the adapter and application against an output short circuit or a single fault open (flyback) feedback loop situations, time-out protection is implemented. When the voltage on FBCTRL pin rises above 4.5 V (typical.), a fault is assumed and switching is blocked.

The time-out protection must not trigger during a normal start-up with the maximum continuous output current.

Test Conditions:

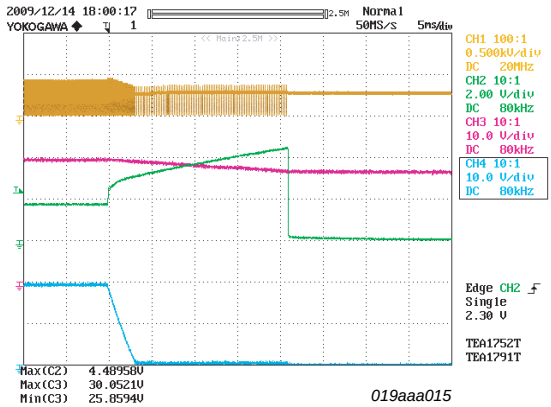
There are two test conditions:

1. The adapter is switched on with 4.62 A output load. After startup a short circuit is applied manually at the end of the output cable
2. Before the adapter is switched on a short circuit is applied to at the end of the output cable

Remark: An output short-circuit is defined as an output impedance of less than 0.1 ohm.

Criteria to pass:

- The adapter must be capable of withstanding a continuous short-circuit at the output without damaging or overstressing the adapter under any input conditions
- The average input power must be less than 3 W during the short-circuit test
- After removal of the short circuit, the adapter must recover automatically



a. Mains input 90 V; 60 Hz

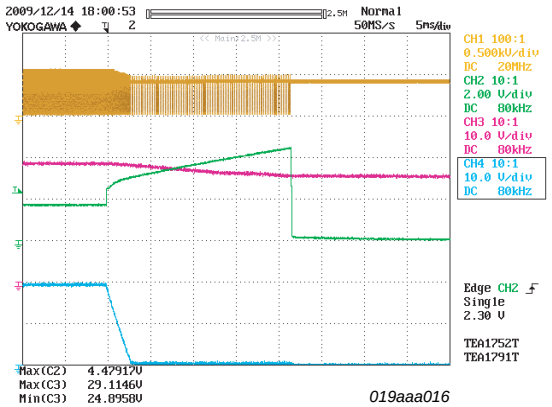
Load before short circuit = 4.62 A

CH1: drain flyback MOSFET

CH2: FBCTRL pin TEA1752T

CH3: VCC pin TEA1752T

CH4: output voltage



b. Mains input 264 V; 50 Hz

Load before short circuit = 4.62 A

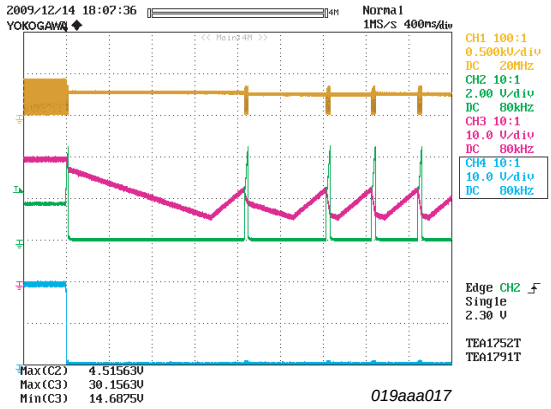
CH1: drain flyback MOSFET

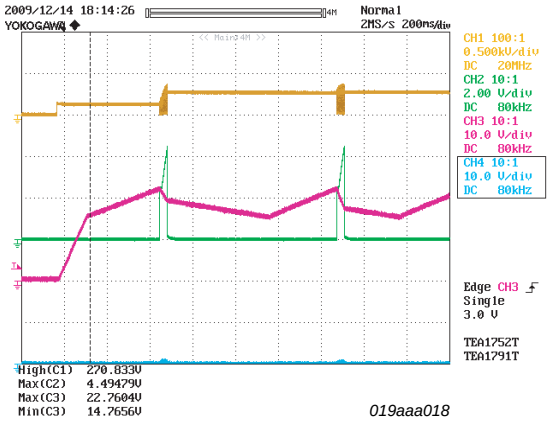
CH2: FBCTRL pin TEA1752T

CH3: FBDRIVER pin TEA1752T

CH4: output voltage

Fig 5. Output short-circuit, triggering of the time-out protection





a. Output short-circuit during normal operation

Load before short circuit= 4.62 A

CH1: drain flyback MOSFET

CH2: FBCTRL pin TEA1752T

CH3: VCC pin TEA1752T

CH4: output voltage

b. Output short-circuit applied before start-up

Load = short circuit

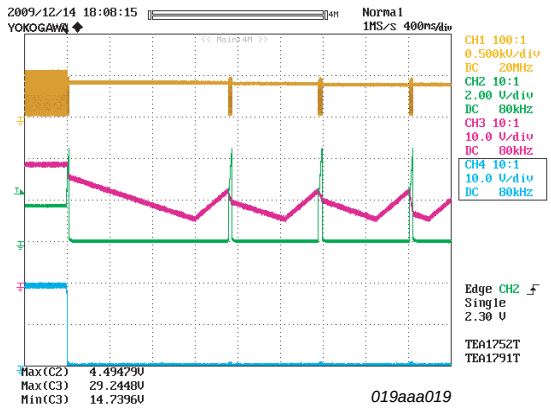
CH1: drain flyback MOSFET

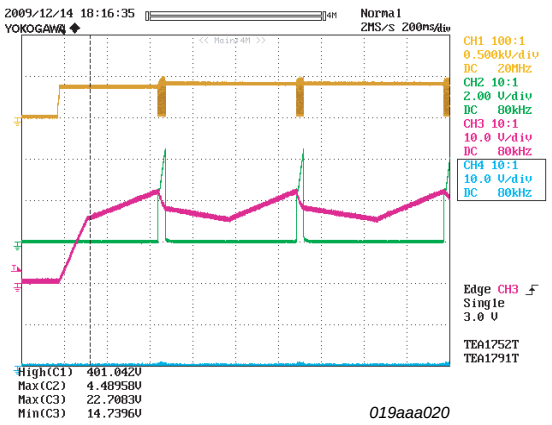
CH2: FBCTRL pin TEA1752T

CH3: VCC pin TEA1752T

CH4: output voltage

Fig 6. Output short-circuit at 90 V; 60 Hz





a. Output short-circuit during normal operation

Load before short circuit = 4.62 A

CH1: drain flyback MOSFET

CH2: FBCTRL pin TEA1752T

CH3: VCC pin TEA1752T

CH4: output voltage

b. Output short-circuit applied before start-up

Load = short circuit

CH1: drain flyback MOSFET

CH2: FBCTRL pin TEA1752T

CH3: VCC pin TEA1752T

CH4: output voltage

Fig 7. Output short-circuit at 264 V; 50 Hz

Table 6. Output short circuit input power

Output short circuit input power as a function of the mains input voltage

Mains supply V; Hz	90; 60	100; 50	115; 60	230; 50	264; 50
Input power P_I (W)	1.113	1.013	0.877	0.456	0.402

3.3.4 Output OverCurrent protection (OCP)

Test Conditions:

- The electronic load is set in Constant Current (CC) mode
- The load is increased from the maximum continuous value in small steps until the over current protection is triggered. The input power is measured after triggering over the over current protection without changing the load setting

Criteria to pass:

- The output power must be limited to less than 150 W, just before the triggering of the over current protection
- The average input power must be less than 3 W once the over current protection has been triggered

Table 7. Output over current protection and input power as a function of the mains input voltage.

Mains supply V; Hz	90; 60	100; 50	115; 60	230; 50	264; 50
Over current trigger level (A)	6.45	6.47	6.47	6.05	6.05
Input power P_I (W)	1.92	1.89	1.82	2.17	2.11

3.3.5 Output OverVoltage Protection (OVP)

Test Conditions:

- The adapter is switched on without a load at the output
- An output over-voltage is created by applying a short circuit across the opto LED of U2

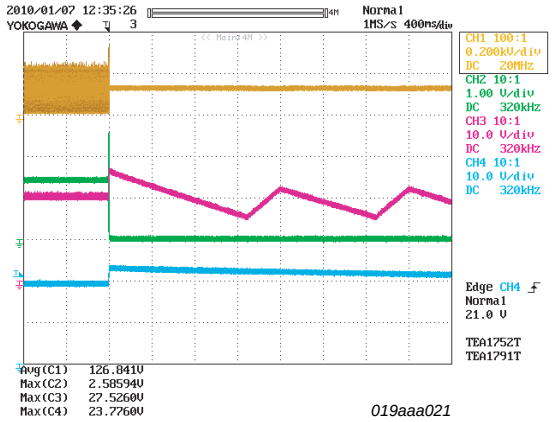
Criteria to pass:

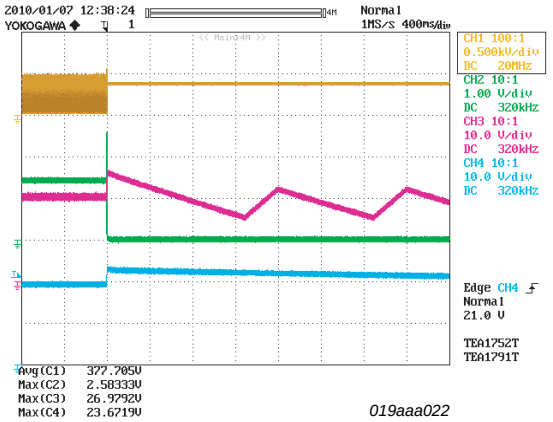
- The output voltage must not exceed 25 V or stabilize between 25 V and the rated output voltage
- The voltage on the TEA1752T VCC pin must not exceed the absolute maximum rating of 38 V
- When OVP is triggered, the primary side controller must shut down and stay in a latched mode
- A single point fault must not cause a sustained overvoltage condition at the output

Table 8. Output over-voltage protection

Output over-voltage at no-load as a function of the mains input voltage with protection mode latched

Mains supply (V; Hz)	90; 60	100; 50	115; 60	230; 50	264; 50
Output OVP trip point (V)	23.8	23.8	23.7	23.8	23.7
VCC maximum during OVP (V)	27.5	27.5	27.5	27.1	27.0





a. Mains input 90 V; 60 Hz

Load before short circuit = 0 A

CH1: drain flyback MOSFET

CH2: FBCTRL pin TEA1752T

CH3: VCC pin TEA1752T

CH4: output voltage

b. Mains input 264 V; 50 Hz

Load before short circuit = 0 A

CH1: drain flyback MOSFET

CH2: FBCTRL pin TEA1752T

CH3: VCC pin TEA1752T

CH4: output voltage

Fig 8. Output OverVoltage Protection

3.3.6 OverTemperature protection (OTP)

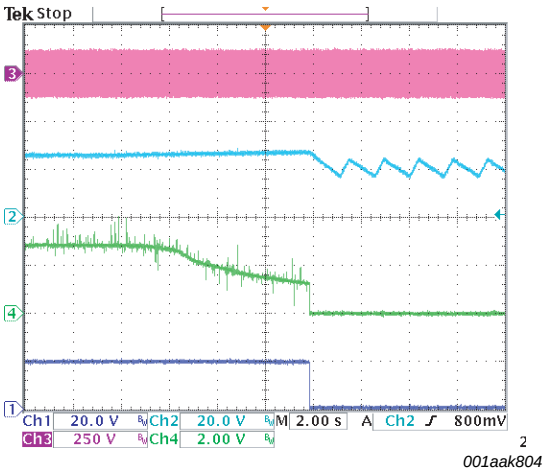
An accurate external over temperature protection (TEA1752T's LATCH pin, RT2, R26 and C19) is provided on the demo board to protect the flyback transformer against overheating (see Figure 14). Normally, the flyback transformer is the most heat sensitive component.

Test Conditions:

The NTC temperature sensor, glued to the transformer, is heated using a heat gun.

Criteria to pass:

The IC must latch off the output at a VLATCH trip level of 1.25V. No output bounce or hiccup is allowed



OTP trigger temperature 108 °C

Load before short-circuit = 0 A

CH1: V_{out}

CH2: TEA1752T VCC pin

CH3: Mains input voltage

CH4: TEA1752T LATCH pin

Fig 9. External OverTemperature Protection (OTP)

3.3.7 Fast latch reset

A Fast Latch Reset function (FLR) enables latched protection to be reset without discharging the bulk elcap. The latch protection is reset as soon as the voltage on VINSENSE pin drops below 0.75 V and is then raised to 0.87 V.

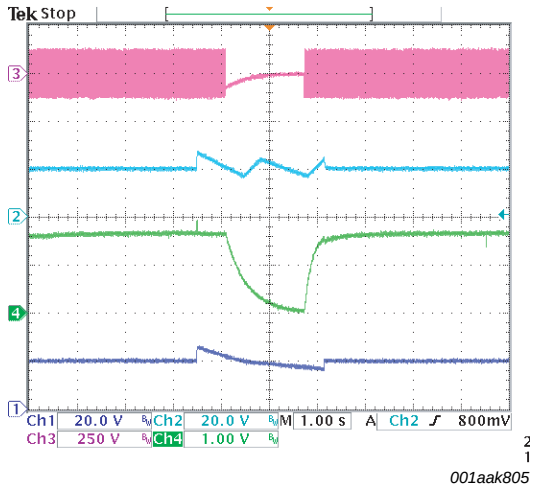
Test conditions:

- The output is not loaded
- The test sequence is as follows:
  - The latch protection is triggered by an OVP caused by a short-circuit across the OPTO led
  - The mains input is switched off and the voltage on pin VINSENSE dropped below 0.75 V
  - The mains input is switched on and, as soon as the voltage on pin VINSENSE rises above 0.87 V, the latch is reset

Remark: Both live and neutral must be switched.

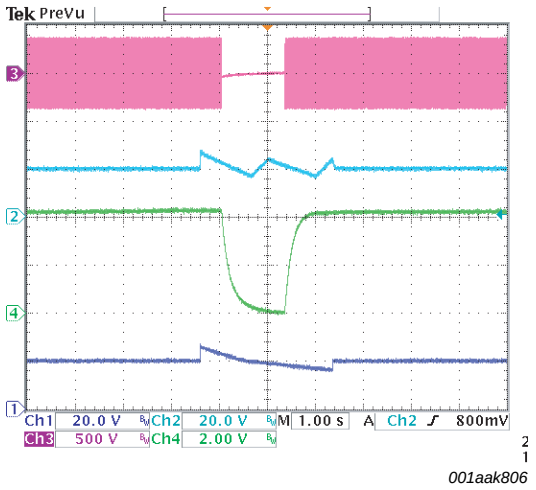
Criteria to pass:

The latch must be reset within 3 seconds after switching off and switching on, the mains input voltage.



a. Mains input 90 V; 60 Hz; FLR = 1.6 s

CH1: V_{out}
CH2: VCC pin TEA1752T
CH3: AC mains input
CH4: VINSENSE pin TEA1752T



b. Mains input 264 V; 50 Hz; FLR = 1.3 s

CH1: V_{out}
CH2: VCC pin TEA1752T
CH3: AC mains input
CH4: VINSENSE pin TEA1752T

Fig 10. Fast Latch Reset (FLR)

3.4 Output regulation and characterization

3.4.1 Load regulation

Test conditions:

- The output voltage deviation is measured while the load current on the output is increased from 0 A to 4.62 A
- The measurement is repeated for different mains input voltages

Remark: The output voltage is measured at the end of the output cable (2 × 20 mΩ).

Criteria to pass:

The output load regulation must remain within 2 %.

The load regulation is calculated using Equation 1.

$$\frac{V_{O(max)} - V_{O(min)}}{V_{O(nom)}} \times 100\ \% \quad (1)$$

where $V_{O(nom)}$ = 19.5 V.

Table 9. Load regulation

Output voltage as a function of the output load and the mains input voltage

Mains supply V; Hz	90; 60	90; 60	264; 50	264; 50
V_O; I_O (V; A)	19.558; 0	19.325; 4.62	19.559; 0	19.324; 4.62

Load regulation at 90 V; 60 Hz is calculated as follows:

$$\frac{19.558V - 19.325V}{19.5V} \times 100\ \% = 1.19\ \% \quad (2)$$

Load regulation at 264 V; 50 Hz is calculated as follows:

$$\frac{19.559V - 19.324V}{19.5V} \times 100\ \% = 1.21\ \% \quad (3)$$

3.4.2 Line regulation

Test conditions:

- The output voltage deviation is measured while the mains voltage on the input is increased from 90 V to 264 V
- The measurement is repeated for different mains input voltages

Remark: The output voltage is measured at the end of the output cable. The load current is 4.62 A.

The line regulation is calculated using the following equation:

$$\frac{V_{O(max)} - V_{O(min)}}{V_{O(nom)}} \times 100\ \% \quad (4)$$

Criteria to pass:

The output voltage deviation must remain within 0.05 %.

Table 10. Line regulation

Output voltage (at full load) as a function of the mains input voltage

Mains supply V; Hz	90; 60	100; 50	115; 60	230; 50	264; 50
V_O (V)	19.325	19.325	19.325	19.324	19.324

Load regulation at 90 V; 60 Hz is calculated using the following equation:

$$\frac{19.325V - 19.324V}{19.5V} \times 100\ \% = 0.005\ \% \quad (5)$$

3.4.3 Ripple and noise PARD (Periodic And Random Deviation)

Ripple and noise are defined as the periodic or random signals over a frequency band of 10 Hz to 20 MHz.

Test Conditions:

- The measurement is made with an oscilloscope set to bandwidth of 20 MHz
- The output is shunted at the end of the output cable, by a 0.1 μF ceramic disk capacitor and a 22 μF electrolytic capacitor, to simulate loading

Criteria to pass:

The output ripple and noise must remain within the specified limits 100 mV (peak-to-peak) at a maximum load current of 4.62 A.

Table 11. Ripple and noise PARD

Ripple and noise (at maximum load) as a function of the mains input voltage.

Mains supply V; Hz	90; 60	100; 50	115; 60	230; 50	264; 50
PARD (mV)	94	94	94	83	83

3.4.4 Dynamic load response

Test Conditions:

- The adapter is subjected to a load change from 0 % to 100 % at a slew rate of 1 A / ms
- The frequency of change is set to give the best readability of the deviation and setting time

Remark: The voltage is measured at the end of the output cable.

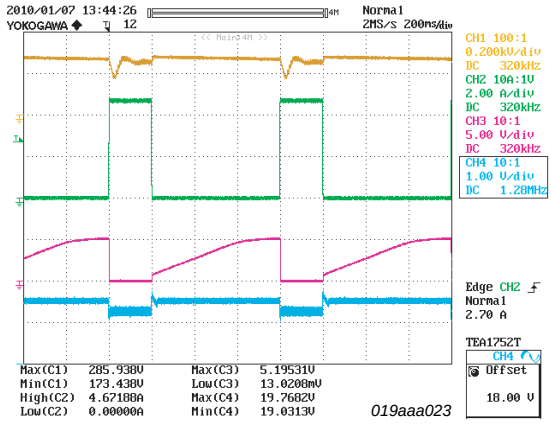
Criteria to pass:

The output is not allowed to have an overshoot or undershoot beyond the specified limits (+1 V to 0.5 V) after a load change.

Table 12. Dynamic load response

Deviation of the output voltage at a load step from 4.62 A to 0 A and from 0 A to 4.62 A

Mains supply V; Hz	90; 60	230; 50
Deviation (mV_{p-p})	700	700



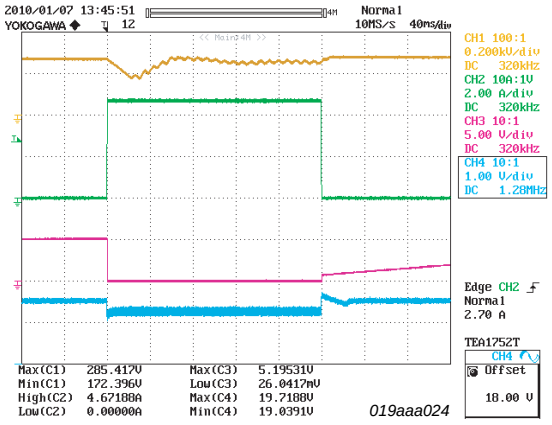
CH1: PFC bus voltage

CH2: output current

Ch3: PFCTIMER pin

Ch4: output voltage

a. Mains input 90 V; 60 Hz



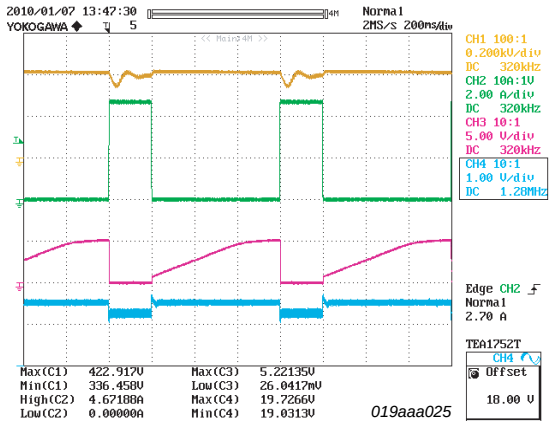
CH1: PFC bus voltage

CH2: output current

Ch3: PFCTIMER pin

Ch4: output voltage

b. Mains input 90 V; 60 Hz (detail picture)



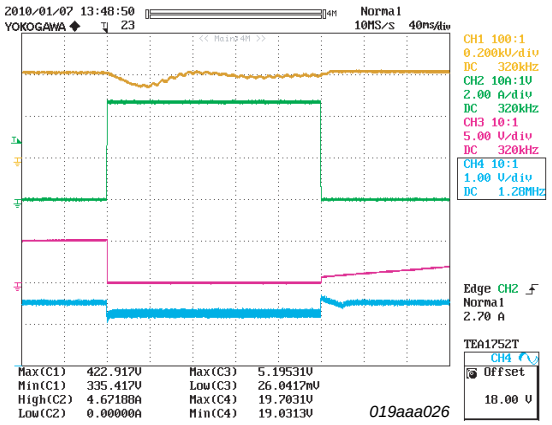
CH1: PFC bus voltage

CH2: output current

Ch3: PFCTIMER pin

Ch4: output voltage

c. Mains input 230 V; 50 Hz



CH1: PFC bus voltage

CH2: output current

Ch3: PFCTIMER pin

Ch4: output voltage

d. Mains input 230 V; 50 Hz (detail picture)

Fig 11. Dynamic load response

4. ElectroMagnetic Compatibility (EMC)

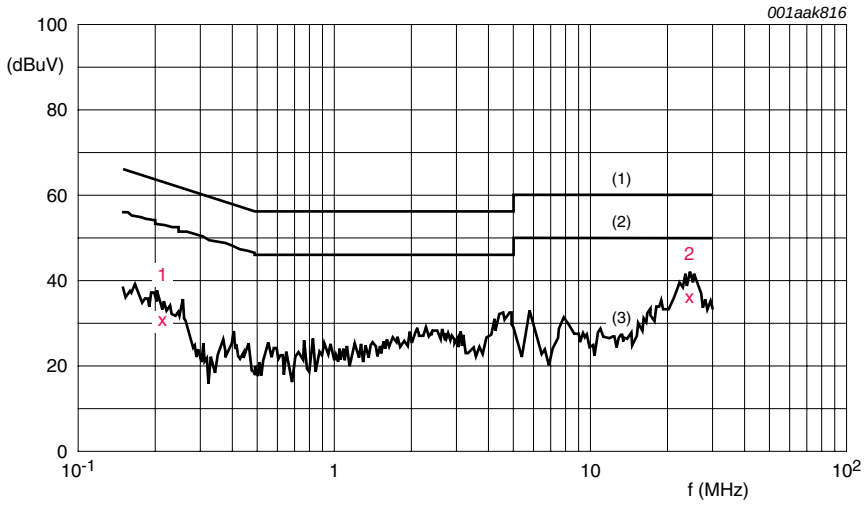
4.1 Conducted emission

Test Conditions:

- The adapter is subjected to maximum load
- The ground connection of the output cable is connected to EMC ground

Criteria to pass:

CISPR22 Class B with -10 dB production margin



(1) QP limit
(2) AV limit
(3) Peak reading

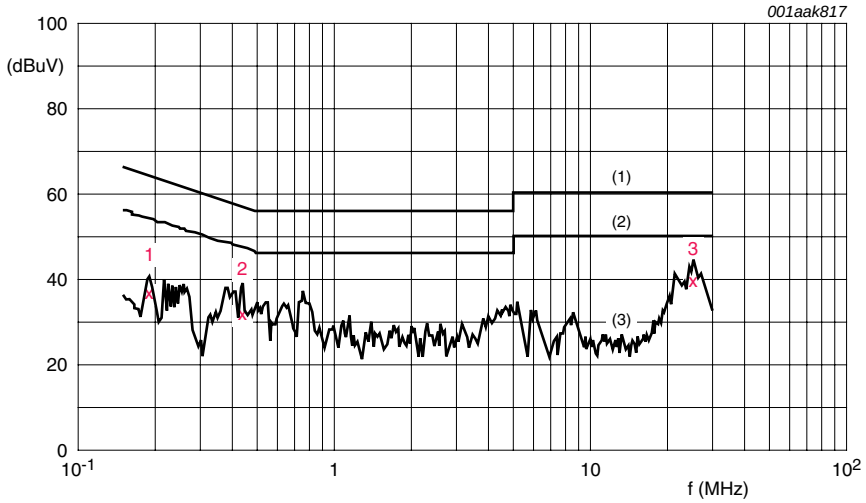
The conducted EMI measurement of 110 V neutral is close to 110 V line

Fig 12. Conducted EMI 110 V line

Table 13. Conducted EMI measurement 110 V line

Refer to Figure 12 points 1 and 2 on the peak reading graph

No.	Frequency	Correction factor	Reading dBμV		Emission dBμV		Limit dBμV		Margins dB	
	MHz	dB	QP	AV	QP	AV	QP	AV	QP	AV
1	0.20112	0.12	32.67	27.68	32.79	27.80	63.56	53.56	−30.77	−25.76
2	24.36328	1.50	35.94	30.50	37.44	32.00	60.00	50.00	−22.56	−18.00



(1) QP limit
(2) AV limit
(3) Peak reading

The conducted EMI measurement of 230 V neutral is close to 230 V line

Fig 13. Conducted EMI 230 V line

Table 14. Conducted EMI measurement 230 V line

Refer to Figure 13 points 1, 2 and 3 on the peak reading graph.

No.	Frequency	Correction factor	Reading dBμV		Emission dBμV		Limit dBμV		Margins dB	
	MHz	dB	QP	AV	QP	AV	QP	AV	QP	AV
1	0.18906	0.09	38.38	37.05	38.47	37.14	64.508	54.08	−25.01	−16.94
2	0.43516	0.20	32.37	24.52	32.57	24.72	5715	47.15	−24.58	−22.43
3	25.11328	1.14	38.45	32.14	39.59	33.28	60.00	50.00	−20.41	−16.72

4.2 Immunity against lighting surges

Test conditions:

- Combination wave: 1.2/50 μs open circuit voltage and 8/20 μs short circuit current
- Test voltage: 2 kV
- L1 to L2: 2 Ω; L1 to PE, L2 to PE and L1 + L2 to PE: 12 Ω
- Phase angle: 0 °, 90 °, 180 ° and 270 °
- Number of tests: 5 positive and 5 negative
- Pulse repetition rate: 20 s

Test result:

- There is no disruption of functionality

4.3 Immunity against ESD

Test conditions:

- ESD air discharge at the ground contact of the output cable

Criteria to pass:

- IEC61000-4-2 air discharge level 3 (8 kV) and level 4 (15 kV)

Table 15. Immunity against ESD

Performance of the adapter at an ESD air discharge

ESD performance	No disruption of function	Auto recovery
Demo board according to schematic	±12 kV	±15 kV
Demo board with 6 M x 10 M across Y-cap	±16.5 kV	-

4.4 Mains harmonic reduction

Test conditions:

- The adapter is set to the maximum continuous load of 4.62 A
- The input voltage is 230 V; 50 Hz

Criteria to pass:

- Compliance with EN61000-3-2 A14 class D

Test result:

- Passed, see Table 16

Table 16. MHR according EN61000-3-2 A14, class D

Harmonic no.	Measured (mA)	Limit (mA)	Harmonic no.	Measured (mA)	Limit (mA)
1	437.2	-	21	1.2	20.1
3	113.5	338.1	23	7.3	18.2
5	37.2	189.0	25	2.3	16.7
7	10.5	99.4	27	5.2	15.3
9	7.3	49.7	29	2.3	14.2
11	9.0	34.8	31	2.5	13.2
13	6.0	34.8	33	0.9	12.4
15	6.7	29.5	35	4.0	11.6
17	3.0	25.5	37	1.2	10.9
19	4.9	22.5	39	3.8	10.3

5. Schematic

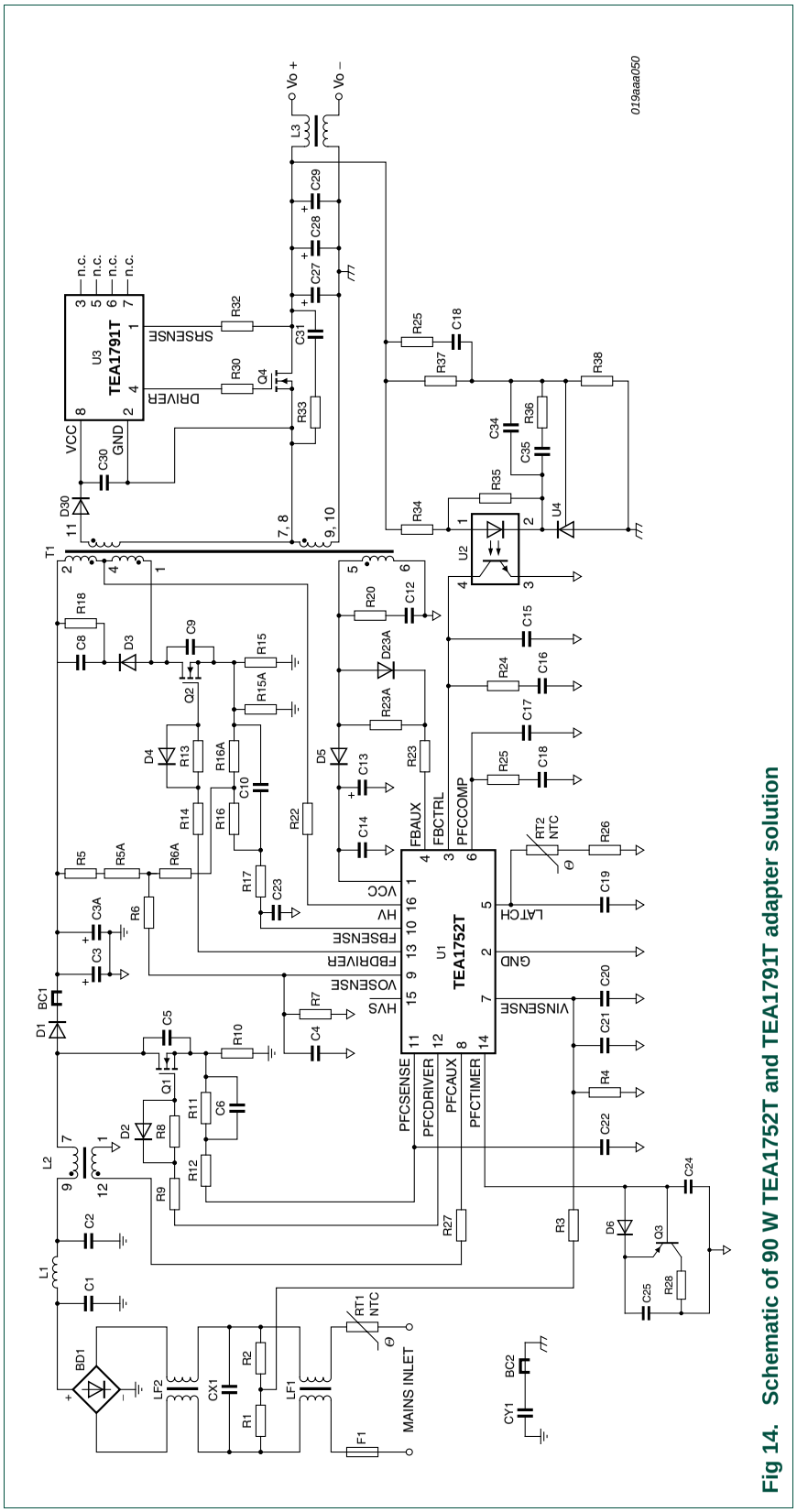


Fig 14. Schematic of 90 W TEA1752T and TEA1791T adapter solution

6. Bill of materials

Table 17. Default bill of materials for a 90 W TEA1752T and TEA1791T adapter solution

Reference	Component	Package	Remark
R1	2 MΩ, 1 %	1206	
R2	2 MΩ, 1 %	1206	
R3	560 kΩ, 1 %	1206	
R4	47 kΩ, 1 %	0603	
R5	2 MΩ, 1 %	1206	
R5A	1.3 MΩ, 1 %	1206	
R6	2.7 MΩ, 1 %	1206	
R6A	2.7 MΩ, 1 %	1206	
R7	60.4 kΩ, 1 %	0603	
R8	10 Ω, 5 %	0805	
R9	10 Ω, 5 %	0805	
R10	0.1 Ω, 5 %; 1 W	axial	metal-oxide film
R11	15 kΩ, 5 %	0603	
R12	1 kΩ, 5 %	0805	
R13	10 Ω, 5 %	0805	
R14	10 Ω, 5 %	0805	
R15	0.1 Ω, 5 %; 1 W	axial	metal-oxide film
R15A	not mounted	-	
R16	51 kΩ, 5 %	0603	
R16A	1 kΩ, 5 %	0603	
R17	1.2 kΩ, 5 %	0603	
R18	43 kΩ, 5 %	1206	
R19	43 kΩ, 5 %	1206	
R20	47 Ω, 5 %	0805	
R21	0 Ω	0805	
R22	10 kΩ, 5 %	0805	
R23	82 kΩ, 1 %	0603	
R23A	220 kΩ, 1 %	0603	
R24	39 kΩ, 5 %	0603	
R25	39 kΩ, 5 %	0603	
R26	10 kΩ, 5 %	0603	
R27	5.1 kΩ, 5 %	1206	
R28	0 Ω	0603	
R29	not mounted	-	
R30	10 Ω, 5 %	0805	
R32	1 kΩ, 5 %	0805	
R33	not Mounted	-	
R34	1 kΩ, 5 %	0603	

Table 17. Default bill of materials for a 90 W TEA1752T and TEA1791T adapter solution *…continued*

Reference	Component	Package	Remark
R35	3 kΩ, 5 %	0603	
R36	10 kΩ, 5 %	0603	
R37	35.7 kΩ, 1 %	0603	
R38	5.23 kΩ, 1 %	0603	
R39	not mounted	-	
RT1	jumper	-	
RT2	NTC 100 kΩ; D = 5 mm	radial lead	TTC050104
C1	film capacitor 0.47 μF; 450 V, 10 %	-	
C2	film capacitor 0.47 μF; 450V, 10 %	-	
C3	electrolytic capacitor 100 μF; 400V; 105 °C	radial 16 × 30 mm	
C3A	10 nF; 1 kV; Z5U	Disk 11.5 mm	
C4	10 nF; 25 V; X7R	0603	
C5	220 pF; 630 V; NP0	1206	
C6	0.1 μF; 25 V; X7R	0603	
C8	3300 pF; 630 V	1206	
C9	100 pF; 630 V; NP0	1206	
C10	0.1 μF; 25 V; X7R	0805	
C12	220 pF; 100 V; NP0	0805	
C13	electrolytic capacitor 47 μF; 35V; 105 °C	radial 5 × 11 mm	low-impedance type
C14	1 μF; 50 V; Y5V	0805	
C15	10 nF; 25 V; X7R	0603	
C16	0.33 μF; 10 V; X7R	0603	timing capacitor; review tolerance
C17	0.33 μF; 10 V; X7R	0603	
C18	0.47 μF; 10 V; X7R	0603	
C19	10 nF; 25 V; X7R	0603	
C20	2.2 μF; 10 V; Y5V	0603	
C21	2.2 μF; 10 V; Y5V	0603	
C22	220 pF; 50 V; NP0	0603	10 V is permitted
C23	220 pF; 50 V; NP0	0603	10 V is permitted
C24	1 nF; 50 V; X7R	0603	10 V is permitted
C25	1 μF; 16 V; X7R	0603	10 V is permitted
C27	electrolytic capacitor 470 μF; 25V; 105 °C	Radial 10 × 12.5 mm	low-impedance type
C28	electrolytic capacitor 470 μF; 25V; 105 °C	Radial 10 × 12.5 mm	low-impedance type
C29	electrolytic capacitor 470 μF; 25V; 105 °C	Radial 10 × 12.5 mm	low-impedance type
C30	1 μF; 50 V; Y5V	0805	
C31	not mounted	-	
C34	0.1 μF; 25 V; X7R	0603	
C35	10 nF; 25 V; X7R	0603	
C36	not mounted	-	
CX1	0.33 μF; 275 V (AC); X2	MKP	

Table 17. Default bill of materials for a 90 W TEA1752T and TEA1791T adapter solution *...continued*

Reference	Component	Package	Remark
CY1	1000 pF; 400 V (AC); Y1	Pitch 10 mm	
BD1	GBU806; 8 A; 600 V	Flat / mini	
D1	MUR460; 4 A; 600 V	DO-201AD	Vishay
D2	1N4148W	SOD-123	
D3	S2M	SMB	
D4	1N4148W	SOD-123	
D5	BAS21	SOT23	NXP Semiconductors, BAS20 is permitted
D6	1N4148	SOD323	
D23A	BAS21	SOT23	NXP Semiconductors, BAS20 is permitted
D27A	not mounted	-	
D30	BAS21	SOT23	NXP Semiconductors
Q1	2SK3568	TO220F	
Q2	2SK3569	TO220F	
Q3	PMBT4403	SOT23	NXP Semiconductors
Q4	PSMN015-100P	TO220	NXP Semiconductors
U1	TEA1752T	SO16	NXP Semiconductors, GreenChip-III PFC and flyback controller
U2	LTV817B	DIP4-W	CTR 130-260, spacing 10.16 mm
U3	TEA1791T	SO8	NXP Semiconductors, GreenChip SR controller
U4	D431	SOT-23R	Double Microelectronics
T1	flyback transformer 450 μH	PQ3220	see specification
L1	inductor 210 μH	T50-52	
L2	PFC inductor 250 μH	RM10	see specification
L3	inductor CM 200 μH	T12*6*4	
LF1	inductor CM 500 μH	T12*6*4	
LF2	inductor CM 12.8 MH	T16*12*18	
BC1	bead core R5B/XP N4/AMAX	RH 4*6*2	placed at cathode of D1
BC2	bead core S6H/JK N6/AMAX	RH 3.5*4.2*1.3	placed at lead of CY1
F1	fuse T 3.15 A; 250 V	LT5	

7. Transformer and inductor specifications

7.1 Flyback transformer T1 specifications

- Primary inductance: 450 μH (±5 %)
- Leakage inductance: 6 μH (max)
- Core/bobbin: PQ3220
- Core material: PC44
- HI-POT primary - secondary: 3 kV; 5 mA; 3 s

Manufacturer: Send Power Electronics. Co., LTD, Taiwan ROC.

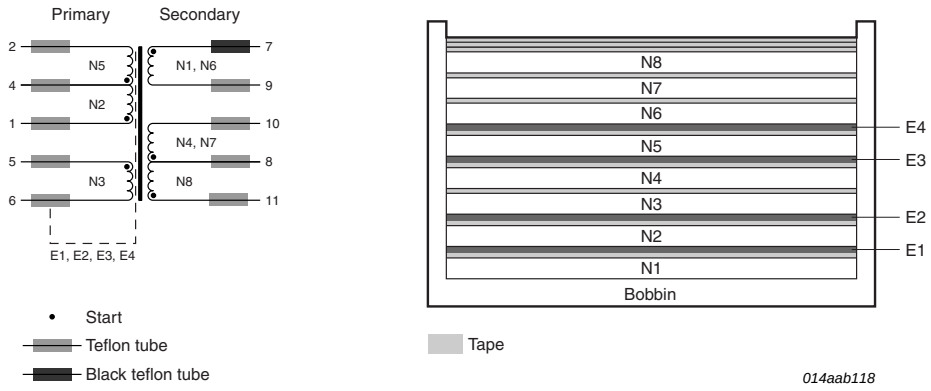


Fig 15. Flyback transformer schematic

Table 18. Flyback transformer winding details

Winding order		Pin number		Wire type	Number of wires	Number of turns		Remarks
		Start	Finish			Winding	MYLAR tape	
1:	N1	7	9	TIW 0.3 mm ∅	2	6	1	TEX-E
2:	E1	-	6	Copper foil 0.025 mm × 7 mm		1	1	finished with wire 0.3 mm ∅
3:	N2	1	4	2-UEW 0.5mm ∅	1	16	1	
4:	E2	-	6	Copper foil 0.025 mm × 7 mm		1	1	finished with wire 0.3 mm ∅
5:	N3	5	6	2-UEW 0.25mm ∅	2	7	1	
6:	N4	8	10	TIW 0.3 mm ∅	2	6	1	TEX-E
7:	E3	-	6	Copper foil 0.025 mm × 7 mm		1	1	finished with wire 0.3 mm ∅
8:	N5	4	2	2-UEW 0.5mm ∅	1	16	1	
9:	E4	-	6	Copper foil 0.025 mm × 7 mm		1	1	finished with wire 0.3 mm ∅
10:	N6	7	9	TIW 0.3 mm ∅	2	6	1	TEX-E
11:	N7	8	10	TIW 0.3 mm ∅	2	6	1	TEX-E
12:	N8	11	8	TIW 0.3 mm ∅	1	5	3	TEX-E; close winding method

7.2 PFC inductor L2 specifications

- Primary inductance: 250 μH (±10 %).
- Core/bobbin: RM10.
- Core material: NC-2H.

Manufacturer: Send Power Electronics. Co., LTD, Taiwan ROC.

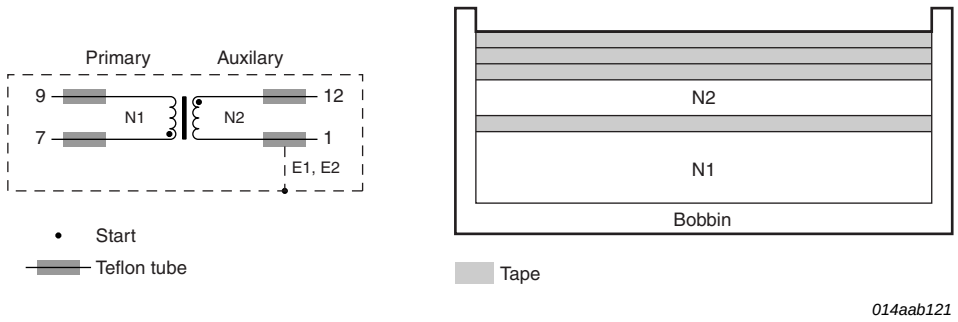


Fig 16. PFC inductor L2 schematic

Table 19. PFC inductor L2 winding details

Winding order		Pin no.		Winding type	Number of wires	Number turns		Remarks
		Start	Finish			Winding	MYLAR tape	
1	N1	9	7	USTC 0.1 mm ∅	30	40 turns	1 turn	-
2	N2	12	1	2-UEW 0.22 mm ∅	2	2.5 turns	3 turns	-

8. PCB layout

The SMPS printed circuit board is a single sided board. Dimensions are 125 mm x 59 mm.

The PCBs are 1.6 mm FR2 with single sided 2 oz. copper (70 m) layer.

The Gerber file set for production of the PCB is available through the local NXP Semiconductors sales office

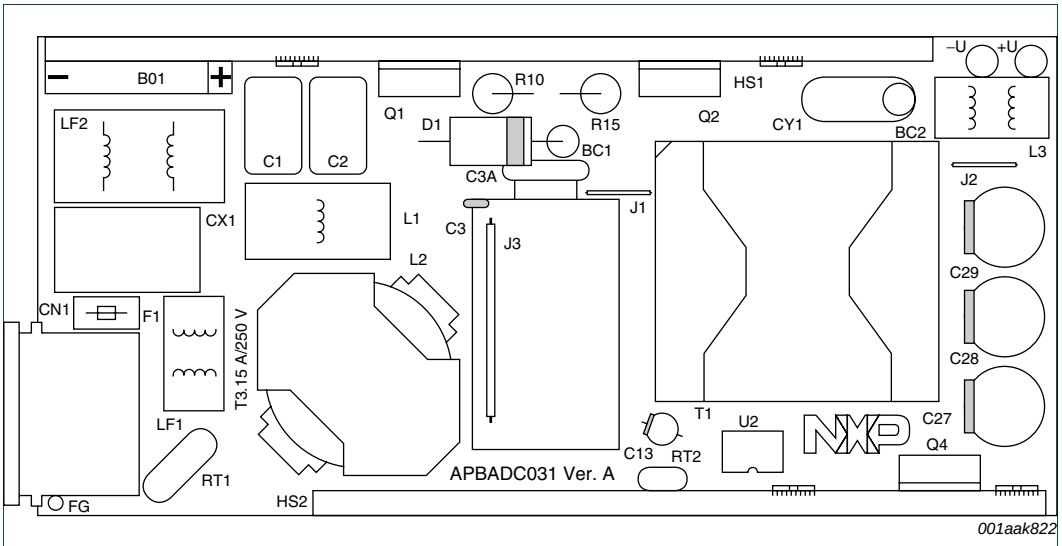


Fig 17. Demo board top silk (top view)

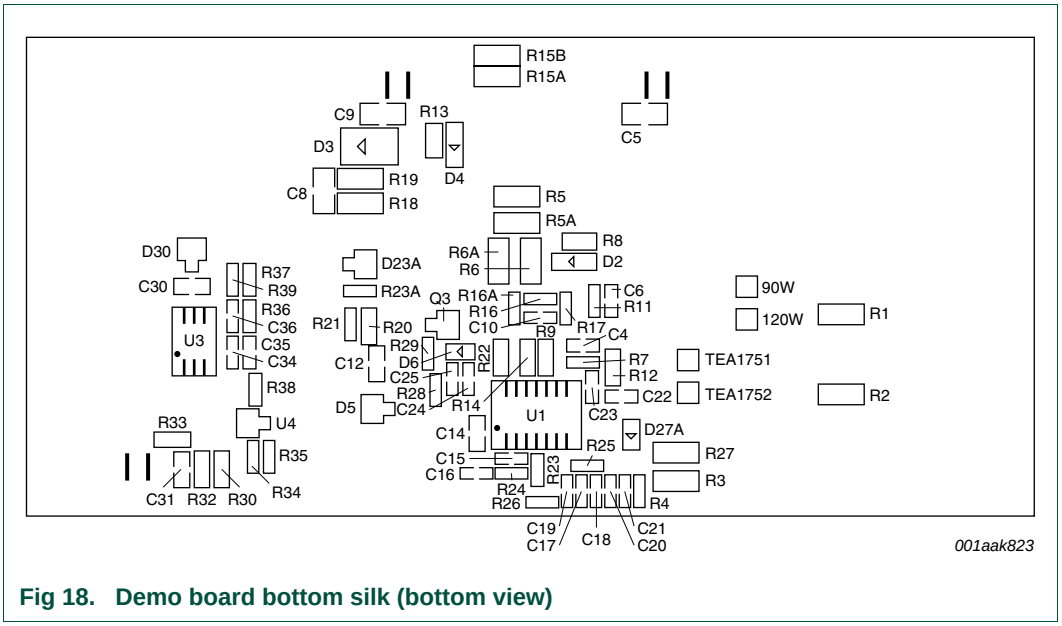
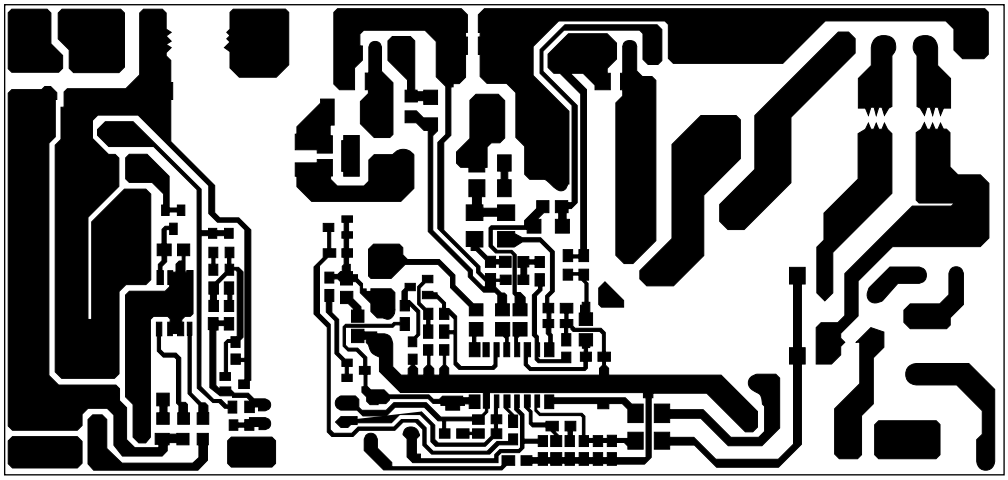


Fig 18. Demo board bottom silk (bottom view)



001aak824

Fig 19. Demo board bottom copper (bottom view)

9. Abbreviations

Table 20. Abbreviations table

Acronym	Description
CC	Constant Current
CR	Constant Resistance
CV	Constant Voltage
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	ElectroMagnetic Susceptibility
ESD	ElectroStatic discharge
FLR	Fast Latch Reset
LISN	Line Impedance Standardization Network
MHR	Mains Harmonic Reduction
OTP	OverTemperature Protection
OCP	OverCurrent Protection
OVP	OverVoltage Protection
PCB	Printed-Circuit Board
PE	Protective Earth
PFC	Power Factor Correction
SCP	Short Circuit Protection
SMPS	Switched Mode Power Supply
SR	Synchronous Rectification
TIW	Triple Insulated Wire
UEW	polyUrethane Enameled Wire
USTC	polyUrethane Silk Tetrone Covered

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