

CoolMOS™ Power Transistor

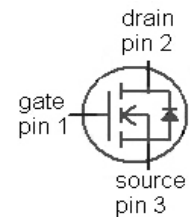
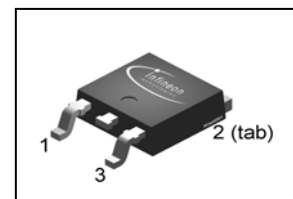
Features

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- High peak current capability
- Ultra low effective capacitances
- Extreme dv/dt rated
- Improved transconductance

Product Summary

$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.75	Ω
I_D	6.2	A

P-TO252-3-1



Type	Package	Ordering Code	Marking
SPD06N60C3	P-TO252-3-1	Q67040-S4630	06N60C3

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	6.2	A
		$T_C=100\text{ °C}$	3.9	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	18.6	
Avalanche energy, single pulse	E_{AS}	$I_D=3.1\text{ A}$, $V_{DD}=50\text{ V}$	200	mJ
Avalanche energy, repetitive t_{AR} ^{1),2)}	E_{AR}	$I_D=6.2\text{ A}$, $V_{DD}=50\text{ V}$	0.5	
Avalanche current, repetitive t_{AR} ¹⁾	I_{AR}		6.2	A
Drain source voltage slope	dv/dt	$I_D=6.2\text{ A}$, $V_{DS}=480\text{ V}$, $T_j=125\text{ °C}$	50	V/ns
Gate source voltage	V_{GS}	static	± 20	V
	V_{GS}	AC ($f > 1\text{ Hz}$)	± 30	
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	74	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1.7	K/W
Thermal resistance, junction - ambient	R_{thJA}	SMD version, device on PCB, minimal footprint	-	-	75	
		SMD version, device on PCB, 6 cm ² cooling area ³⁾	-	50	-	
Soldering temperature	T_{sold}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	600	-	-	V
Avalanche breakdown voltage	$V_{(BR)DS}$	$V_{GS}=0\text{ V}$, $I_D=6.2\text{ A}$	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=0.26\text{ mA}$	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}$, $I_D=3.9\text{ A}$, $T_j=25\text{ °C}$	-	0.68	0.75	Ω
		$V_{GS}=10\text{ V}$, $I_D=3.9\text{ A}$, $T_j=150\text{ °C}$	-	1.82	-	
Gate resistance	R_G	$f=1\text{ MHz}$, open drain	-	1	-	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=3.9\text{ A}$	-	5.6	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	620	-	pF
Output capacitance	C_{oss}		-	200	-	
Reverse transfer capacitance	C_{rss}		-	17	-	
Effective output capacitance, energy related ⁴⁾	$C_{o(er)}$	$V_{GS}=0\text{ V}, V_{DS}=0\text{ V}$ to 480 V	-	28	-	
Effective output capacitance, time related ⁵⁾	$C_{o(tr)}$		-	47	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=480\text{ V},$ $V_{GS}=10\text{ V}, I_D=6.2\text{ A},$ $R_G=12\ \Omega$	-	7	-	ns
Rise time	t_r		-	12	-	
Turn-off delay time	$t_{d(off)}$		-	52	-	
Fall time	t_f		-	10	-	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	$V_{DD}=480\text{ V}, I_D=6.2\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	3.3	-	nC
Gate to drain charge	Q_{gd}		-	12	-	
Gate charge total	Q_g		-	24	31	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

¹⁾ Pulse width limited by maximum temperature $T_{j,max}$ only

²⁾ Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR} \cdot f$.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

⁴⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁵⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

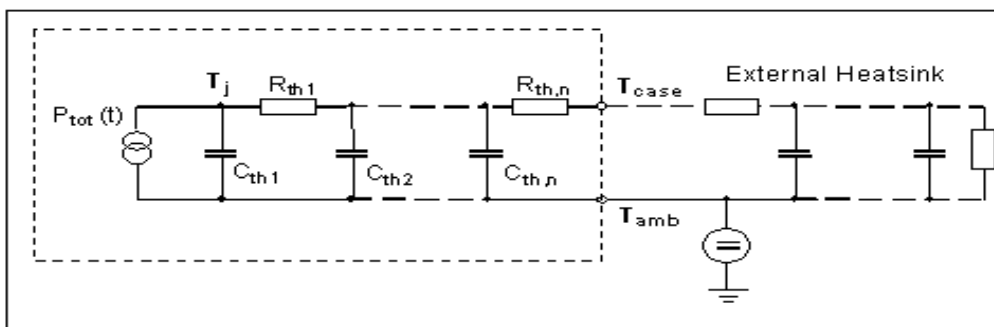
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^{\circ}\text{C}$	-	-	6.2	A
Diode pulse current	$I_{S,pulse}$		-	-	18.6	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=6.2\text{ A}, T_J=25\text{ }^{\circ}\text{C}$	-	0.97	1.2	V
Reverse recovery time	t_{rr}	$V_R=480\text{ V}, I_F=I_S, di_F/dt=100\text{ A}/\mu\text{s}$	-	400	-	ns
Reverse recovery charge	Q_{rr}		-	3.5	-	μC
Peak reverse recovery current	I_{rrm}		-	25	-	A

Typical Transient Thermal Characteristics

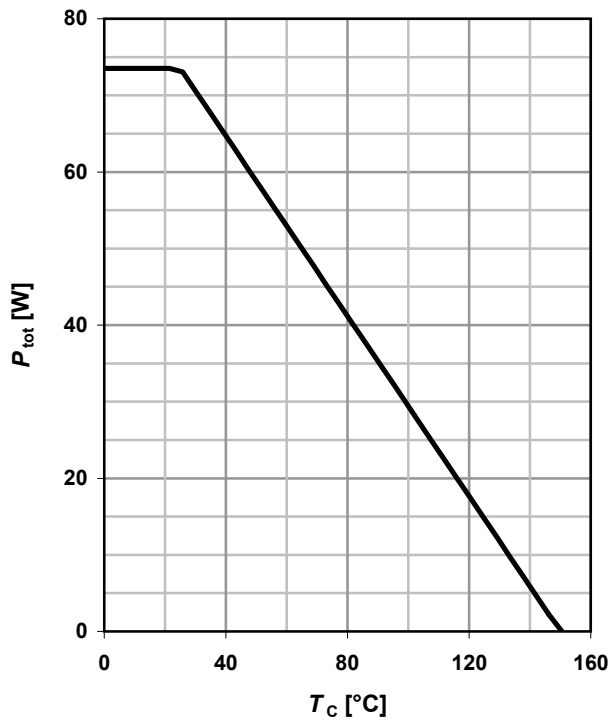
Symbol	Value	Unit	Symbol	Value	Unit
	typ.			typ.	
R_{th1}	0.0325	K/W	C_{th1}	0.0000502	Ws/K
R_{th2}	0.0448		C_{th2}	0.000303	
R_{th3}	0.251		C_{th3}	0.000428	
R_{th4}	0.31		C_{th4}	0.00243	
R_{th5}	0.231		C_{th5}	0.00344	
			C_{th6}	0.198 ⁶⁾	



⁶⁾ C_{th6} models the additional heat capacitance of the package in case of non-ideal cooling. It is not needed if $R_{thCA}=0\text{ K/W}$.

1 Power dissipation

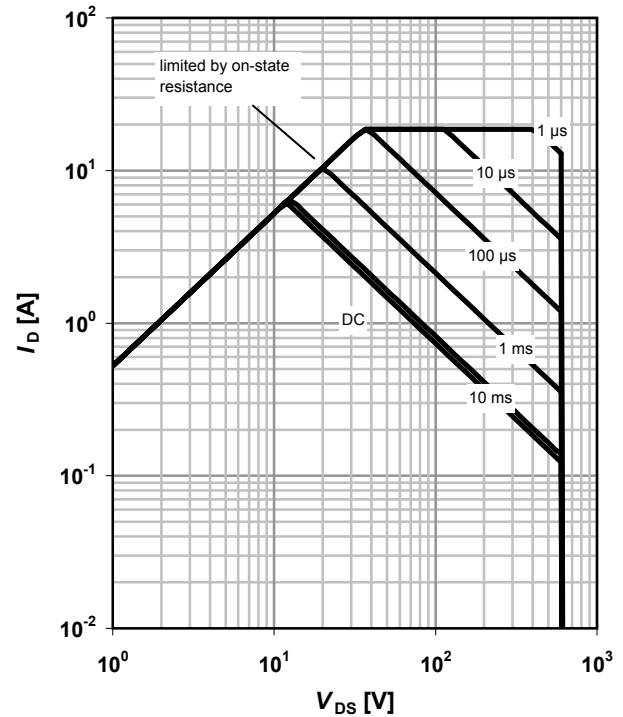
$$P_{\text{tot}} = f(T_C)$$



2 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

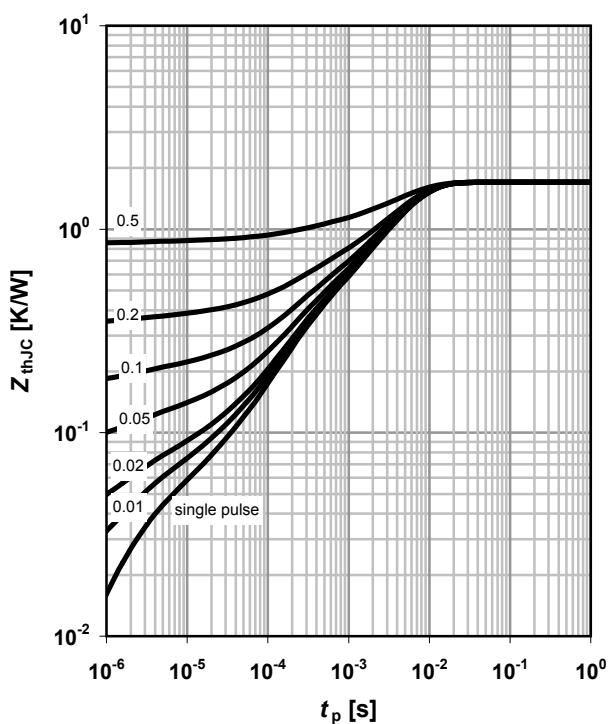
parameter: t_p



3 Max. transient thermal impedance

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

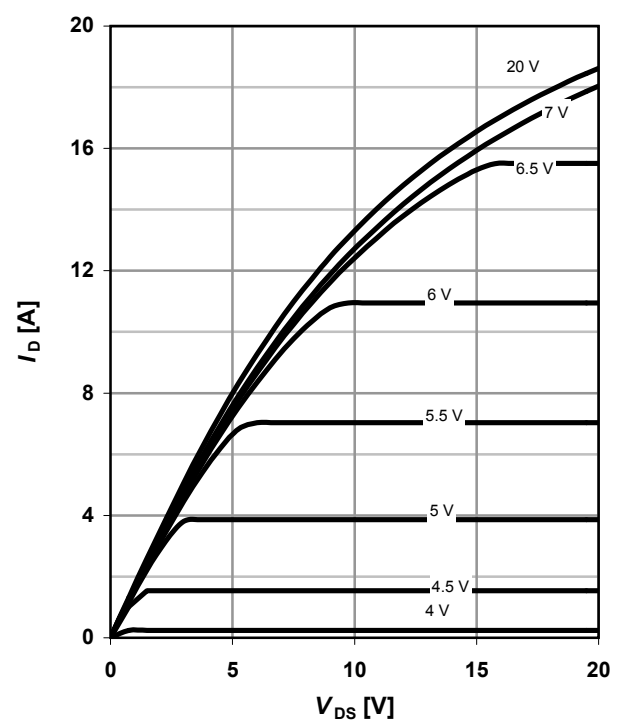
parameter: $D = t_p / T$



4 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

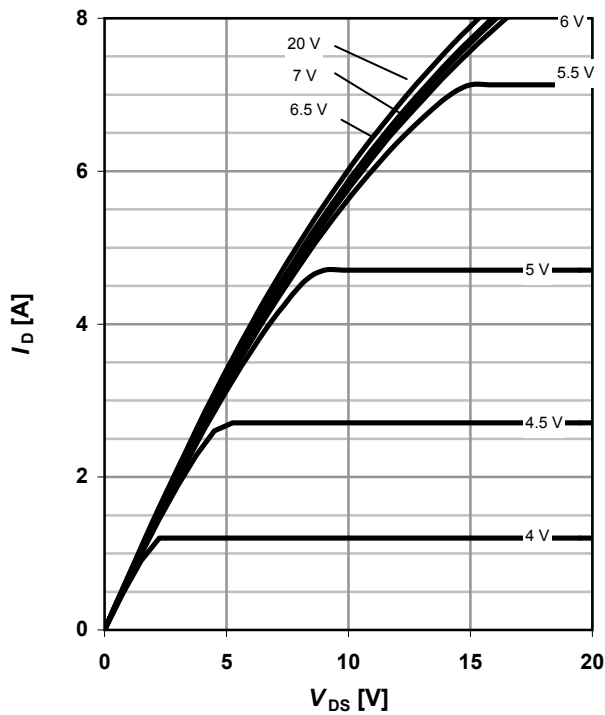
parameter: V_{GS}



5 Typ. output characteristics

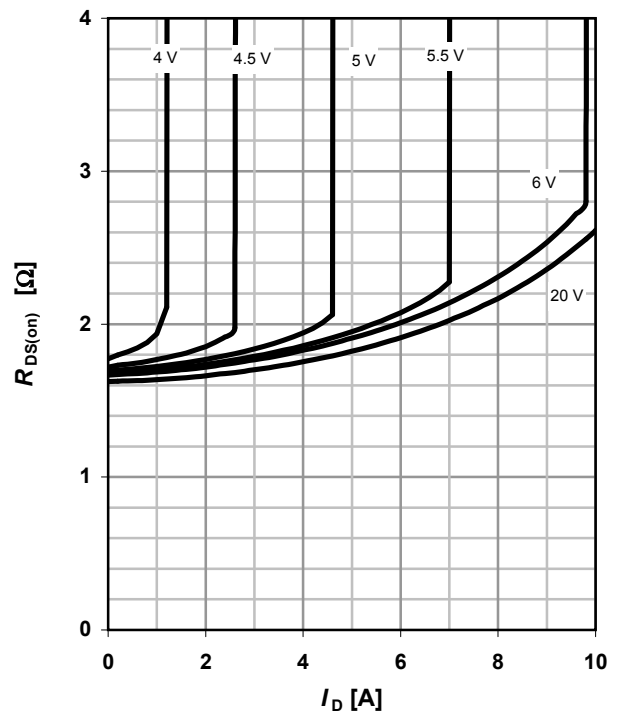
$$I_D = f(V_{DS}); T_j = 150^\circ\text{C}$$

parameter: V_{GS}

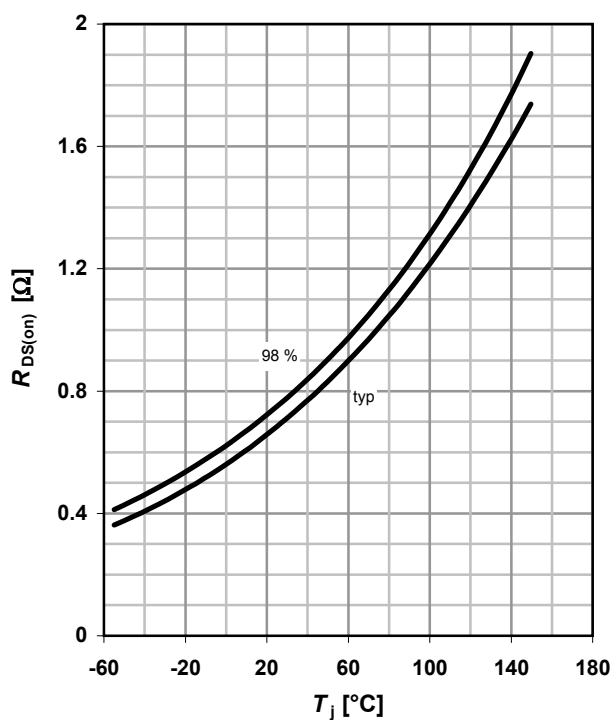

6 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(I_D); T_j = 150^\circ\text{C}$$

parameter: V_{GS}

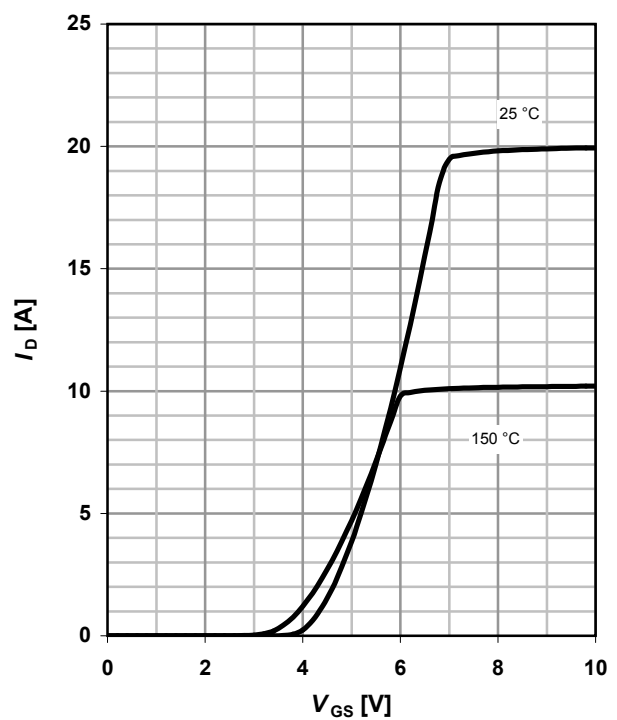

7 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = 3.9\text{ A}; V_{GS} = 10\text{ V}$$

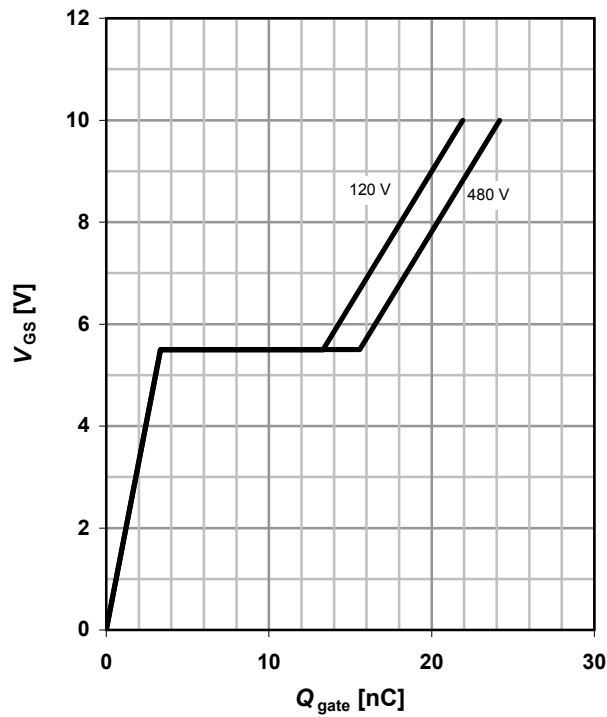

8 Typ. transfer characteristics

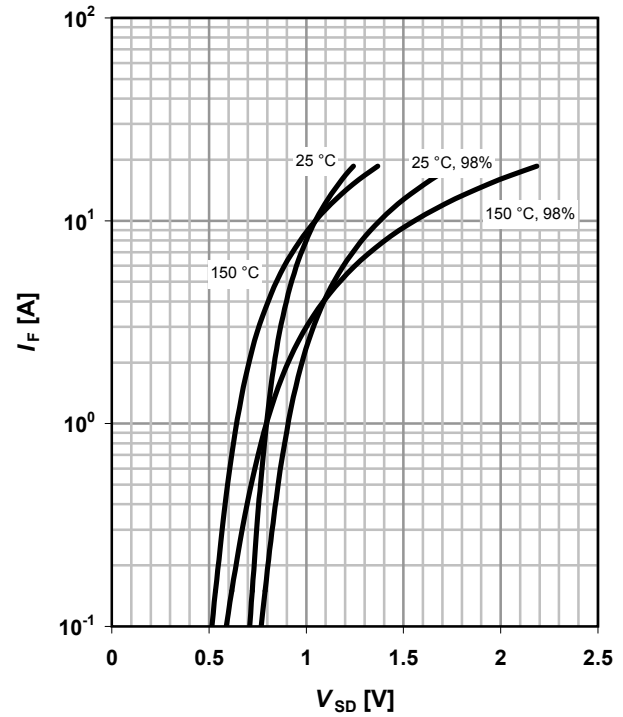
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)\text{max}}$$

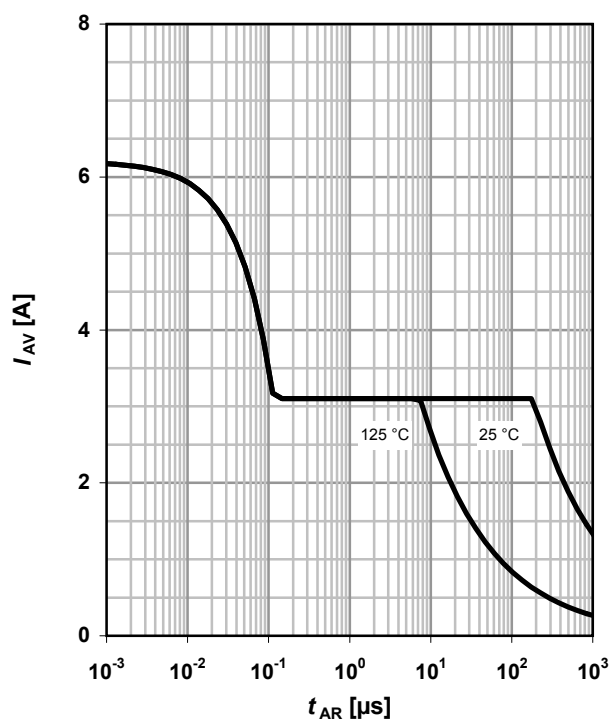
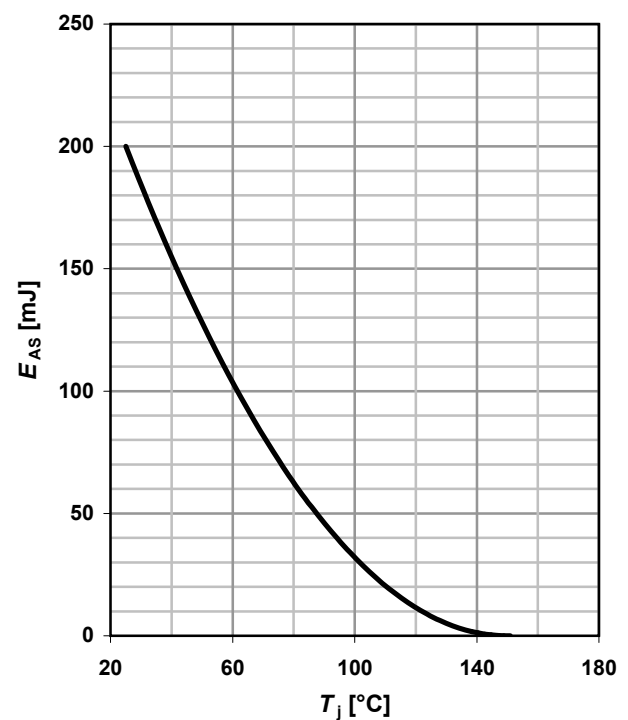
parameter: T_j



9 Typ. gate charge
 $V_{GS}=f(Q_{gate}); I_D=6.2 \text{ A pulsed}$

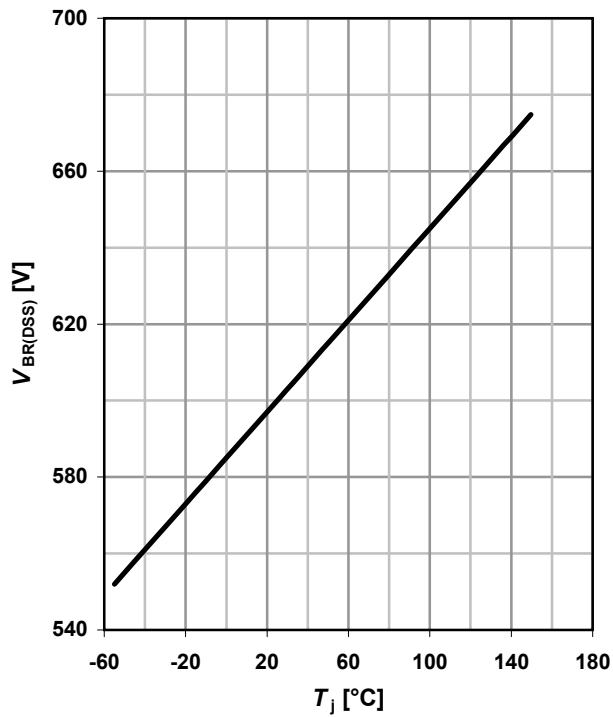
parameter: V_{DD}

10 Forward characteristics of reverse diode
 $I_F=f(V_{SD})$

parameter: T_j

11 Avalanche SOA
 $I_{AR}=f(t_{AR})$

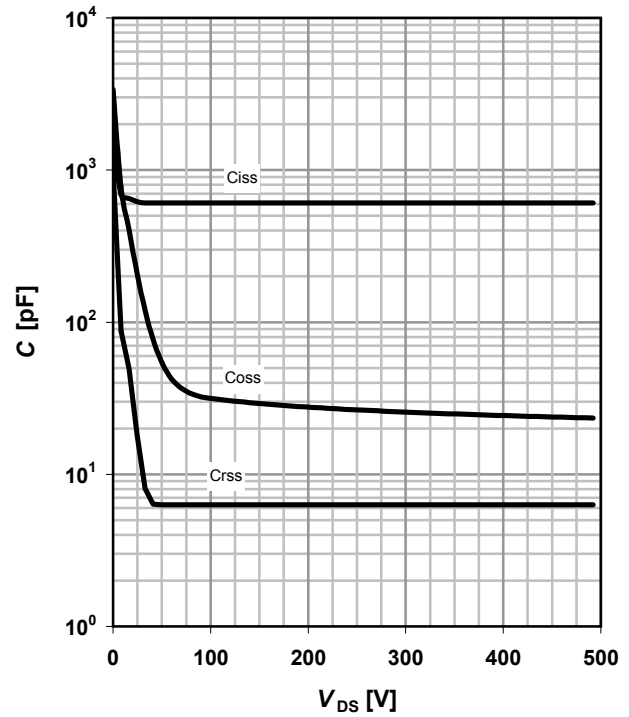
parameter: $T_{j(\text{start})}$

12 Avalanche energy
 $E_{AS}=f(T_j); I_D=3.1 \text{ A}; V_{DD}=50 \text{ V}$


13 Drain-source breakdown voltage

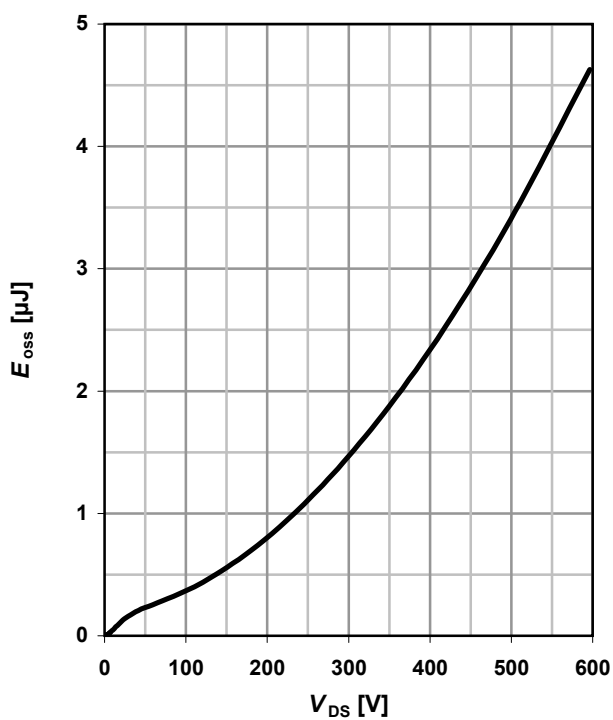
$$V_{BR(DSS)} = f(T_j); I_D = 0.25 \text{ mA}$$


14 Typ. capacitances

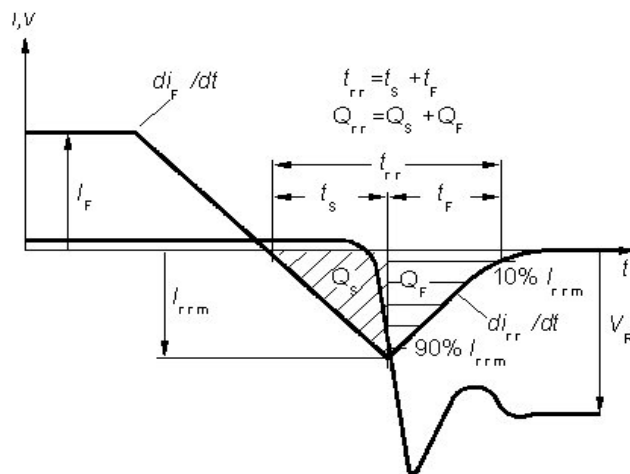
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$


15 Typ. C_{oss} stored energy

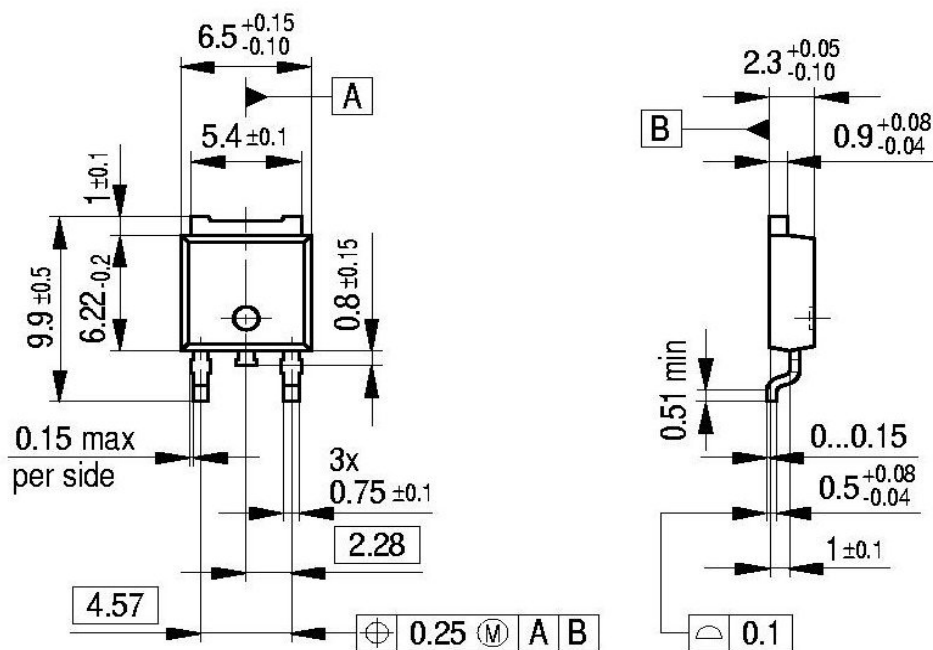
$$E_{oss} = f(V_{DS})$$



Definition of diode switching characteristics



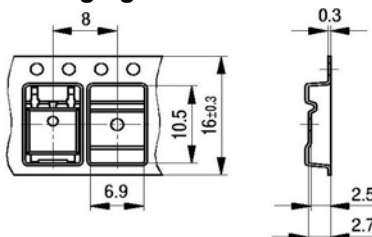
P-TO252-3-1: Outline



GPT09051

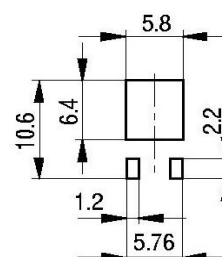
All metal surfaces tin plated, except area of cut.

Packaging



Dimensions in mm

Footprint



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