SHARC Processors

ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

SUMMARY

High performance 32-bit/40-bit floating point processor optimized for high performance audio processing

Single-instruction, multiple-data (SIMD) computational architecture

On-chip memory—3M bits of on-chip SRAM

Code compatible with all other members of the SHARC family

The ADSP-2136x processors are available with a 333 MHz core instruction rate with unique audiocentric peripherals such as the digital applications interface, S/PDIF transceiver, DTCP (digital transmission content protection protocol), serial ports, precision clock generators, and more. For complete ordering information, see Ordering Guide on Page 51.

DEDICATED AUDIO COMPONENTS

S/PDIF-compatible digital audio receiver/transmitter

8 channels of asynchronous sample rate converters (SRC)

16 PWM outputs configured as four groups of four outputs

ROM-based security features include

- **JTAG access to memory permitted with a 64-bit key**
- **Protected memory regions that can be assigned to limit access under program control to sensitive code**

PLL has a wide variety of software and hardware multiplier/divider ratios

Available in 136-ball BGA and 144-lead LQFP_EP packages

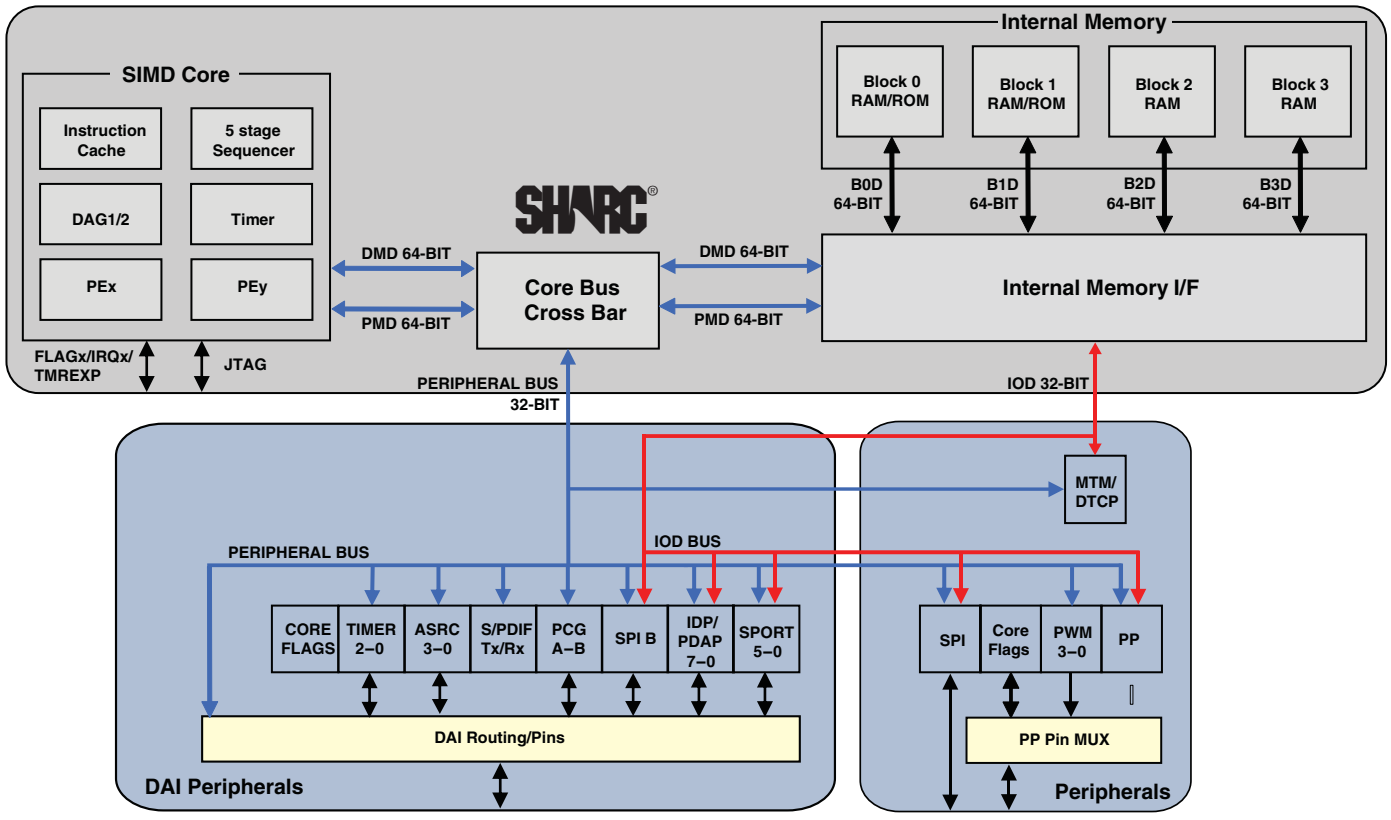

Figure 1. Functional Block Diagram

Rev. E

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REVISION HISTORY

10/09—Rev. D to Rev. E

Corrected all outstanding document errata. Also replaced core clock references (CCLK) in the timing specifications with peripheral clock references (PCLK).

For this revision the following sections have been removed. For information see the *ADSP-2136x SHARC Processor Hardware Reference*: “Address Data Pins as Flags”, “Address/Data Modes”, Core Instruction Rate to CLKIN Ratio Modes.”

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GENERAL DESCRIPTION

The ADSP-2136x SHARC® processor is a member of the SIMD SHARC family of DSPs that feature Analog Devices, Inc., Super Harvard Architecture. The processor is source code-compatible with the ADSP-2126x and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-2136x is a 32-/40-bit floating-point processor optimized for high performance automotive audio applications with a large on-chip SRAM and ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital audio interface (DAI).

As shown in the functional block diagram on Page 1, the ADSP-2136x uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of signal processing algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-2136x processor achieves an instruction cycle time of 3.0 ns at 333 MHz. With its SIMD computational hardware, the ADSP-2136x can perform two GFLOPS running at 333 MHz.

Table 1 shows performance benchmarks for these devices. Table 2 shows the features of the individual product offerings.

Table 1. Benchmarks (at 333 MHz)

Benchmark Algorithm	Speed (at 333 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	27.9 µs
FIR Filter (per tap)[1]	1.5 ns
IIR Filter (per biquad)[1]	6.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	13.5 ns
[4×4] × [4×1]	23.9 ns
Divide (y/x)	10.5 ns
Inverse Square Root	16.3 ns

[1] Assumes two files in multichannel SIMD mode

Table 2. ADSP-2136x Family Features

Feature	ADSP-21362	ADSP-21363	ADSP-21364	ADSP-21365	ADSP-21366
RAM	3M bit	3M bit	3M bit	3M bit	3M bit
ROM	4M bit	4M bit	4M bit	4M bit	4M bit
Audio Decoders in ROM[1]	No	No	No	Yes	Yes
Pulse-Width Modulation	Yes	Yes	Yes	Yes	Yes
S/PDIF	Yes	No	Yes	Yes	Yes
DTCP[2]	Yes	No	No	Yes	No
SRC Performance	128 dB	No SRC	140 dB	128 dB	128 dB

[1] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Prologic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

[2] The ADSP-21362 and ADSP-21365 processors provide the Digital Transmission Content Protection protocol, a proprietary security protocol. Contact your Analog Devices sales office for more information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-2136x processors. The core clock domain contains the following features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (3M bit)
- On-chip mask-programmable ROM (4M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allow flexible exception handling.

The diagram on Page 1 also shows the following architectural features:

- I/O processor which handles 32-bit DMA for the peripherals
- Six full duplex serial ports
- Two SPI-compatible interface ports—primary on dedicated pins, secondary on DAI pins
- 8-bit or 16-bit parallel port that supports interfaces to off-chip memory peripherals
- Digital audio interface that includes two precision clock generators (PCG), an input data port (IDP), an S/PDIF receiver/transmitter, 8-channel asynchronous sample rate converter, DTCP cipher, six serial ports, eight serial inter-

faces, a 20-bit parallel input port, 10 interrupts, six flag outputs, six flag inputs, three timers, and a flexible signal routing unit (SRU).

SHARC FAMILY CORE ARCHITECTURE

The ADSP-2136x is code-compatible at the assembly level with the ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2136x shares architectural features with the ADSP-2126x and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

SIMD Computational Engine

The processor contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY can be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive signal processing algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit, single-precision floating-point, 40-bit extended-precision floating-point, and 32-bit fixed-point data formats.

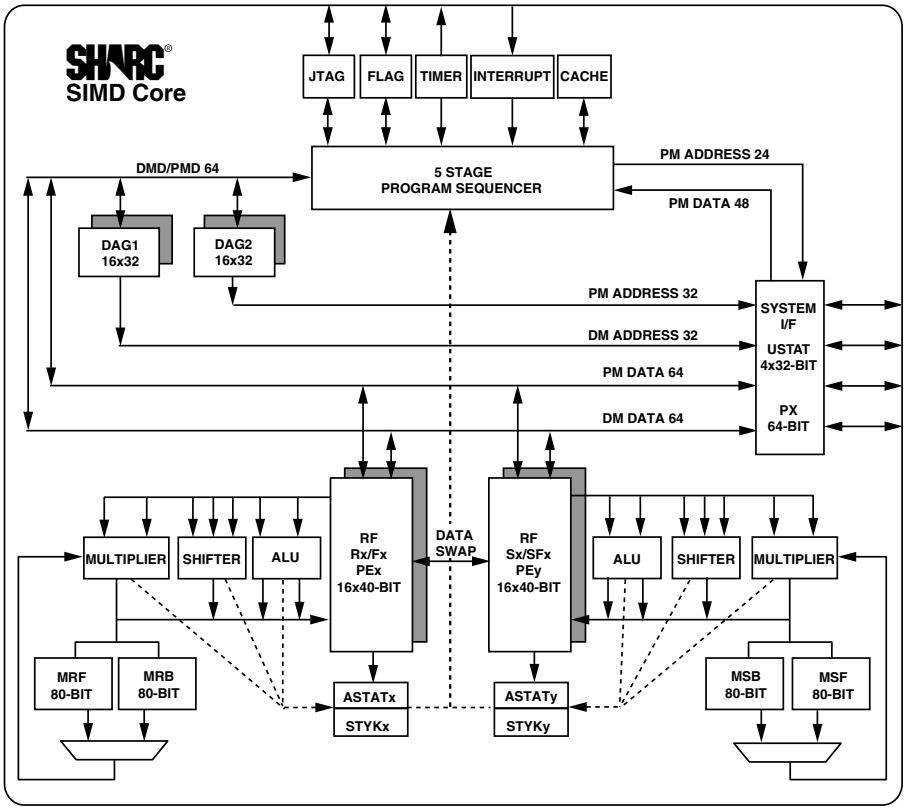


Figure 2. SHARC Core Block Diagram

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2136x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Context switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result register all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

Universal Registers

The universal registers can be used for general purpose. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all system registers (control/status) of the core.

The data bus exchange register PX permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM data bus. These registers contain hardware to handle the data width difference.

Timer

A core timer that can generate periodic software Interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Single-Cycle Fetch of Instruction and Four Operands

The processor features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With the processor's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The processor's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the processor can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

On-Chip Memory

The processor contains 3M bits of internal SRAM and 4M bits of internal ROM. Each block can be configured for different combinations of code and data storage (see Table 3). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The processor's memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

The SRAM can be configured as a maximum of 96K words of 32-bit data, 192K words of 16-bit data, 64K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 3M bits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

On-Chip Memory Bandwidth

The internal memory architecture allows three accesses at the same time to any of the four blocks, assuming no block conflicts. The total bandwidth is gained with DMD and PMD (2 × 64-bits, core CLK) and the IOD bus (32-bit, PCLK)

ROM-Based Security

The processor has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through

Table 3. ADSP-2136x Internal Memory Space

IOP Registers 0x0000 0000–0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM 0x0004 0000–0x0004 7FFF	Block 0 ROM 0x0008 0000–0x0008 AAA9	Block 0 ROM 0x0008 0000–0x0008 FFFF	Block 0 ROM 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 BFFF		Reserved 0x0009 0000–0x0009 7FFF	Reserved 0x0012 0000–0x0012 FFFF
Block 0 SRAM 0x0004 C000–0x0004 FFFF	Block 0 SRAM 0x0009 0000–0x0009 5554	Block 0 SRAM 0x0009 8000–0x0009 FFFF	Block 0 SRAM 0x0013 0000–0x0013 FFFF
Block 1 ROM 0x0005 0000–0x0005 7FFF	Block 1 ROM 0x000A 0000–0x000A AAA9	Block 1 ROM 0x000A 0000–0x000A FFFF	Block 1 ROM 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 BFFF		Reserved 0x000B 0000–0x000B 7FFF	Reserved 0x0016 0000–0x0016 FFFF
Block 1 SRAM 0x0005 C000–0x0005 FFFF	Block 1 SRAM 0x000B 0000–0x000B 5554	Block 1 SRAM 0x000B 8000–0x000B FFFF	Block 1 SRAM 0x0017 0000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 1FFF	Block 2 SRAM 0x000C 0000–0x000C 2AA9	Block 2 SRAM 0x000C 0000–0x000C 3FFF	Block 2 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000–0x0006 FFFF		Reserved 0x000C 4000–0x000D FFFF	Reserved 0x0018 8000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 1FFF	Block 3 SRAM 0x000E 0000–0x000E 2AA9	Block 3 SRAM 0x000E 0000–0x000E 3FFF	Block 3 SRAM 0x001C 0000–0x001C 7FFF
Reserved 0x0007 2000–0x0007 FFFF		Reserved 0x000E 4000–0x000F FFFF	Reserved 0x001C 8000–0x001F FFFF
			Reserved 0x0020 0000–0xFFFF FFFF

the JTAG or test access port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2136x family contains a rich set of peripherals that support a wide variety of applications, including high quality audio, medical imaging, communications, military , test equipment, 3D graphics, speech recognition, monitor control, imaging, and other applications.

Parallel Port

The parallel port provides interfaces to SRAM and peripheral devices. The multiplexed address and data pins (AD15–0) can access 8-bit devices with up to 24 bits of address, or 16-bit devices with up to 16 bits of address. In either mode, 8-bit or 16-bit, the maximum data transfer rate is 55 Mbps.

DMA transfers are used to move data to and from internal memory. Access to the core is also facilitated through the parallel port register read/write functions. The $\overline{RD}$, $\overline{WR}$, and ALE (address latch enable) pins are the control pins for the parallel port.

Serial Peripheral (Compatible) Interface

The processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the processor's SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes and can operate at a maximum baud rate of 41.67 MHz.

The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-2136x SPI-compatible peripheral implementation also features programmable baud rate, clock phase, and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on

two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

Digital Audio Interface (DAI)

The digital audio interface (DAI) provides the ability to connect various peripherals to any of the DSP's DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU, shown in Figure 1).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI- associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes six serial ports, an S/PDIF receiver/transmitter, a DTCP cipher, a precision clock generator (PCG), eight channels of asynchronous sample rate converters, an input data port (IDP), an SPI port, six flag outputs and six flag inputs, and three timers. The IDP provides an additional input path to the ADSP-2136x core, configurable as either eight channels of I^2S serial data or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

For complete information on using the DAI, see the *ADSP-2136x SHARC Processor Hardware Reference*.

Serial Ports

The processor features six synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and a frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTs are enabled, or six full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of 41.67 Mbps. Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I^2S protocols (I^2S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs, such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pairs or I^2S channels (using two stereo devices) per serial port, with a maximum of up to 24 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I^2S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the transmitter can be formatted as left-justified, I^2S, or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

Digital Transmission Content Protection (DTCP)

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) will be protected by this copy protection system. This feature is available on the ADSP-21362 and

ADSP-21365 processors only. Licensing through DTLA is required for these products. Visit www.dtcp.com for more information.

Memory-to-Memory (MTM)

If the DTCP module is not used, the memory-to-memory DMA module allows internal memory copies for a standard DMA.

Synchronous/Asynchronous Sample Rate Converter (SRC)

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 140 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC is used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

The S/PDIF and SRC are not available on the ADSP-21363 models.

Input Data Port (IDP)

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of two units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A and B, C, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Peripheral Timers

Three general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

Each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

I/O PROCESSOR FEATURES

The processor's I/O provides many channels of DMA and controls the extensive set of peripherals described in the previous sections.

DMA Controller

The processor's on-chip DMA controllers allow data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP), or the parallel port (PP). See Table 4.

Table 4. DMA Channels

Peripheral	ADSP-2136x
SPORT	12
PDAP	8
SPI	2
MTM/DTCP	2
PP	1
Total DMA Channels	25

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the processor boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave, or an internal boot. Booting is determined by the boot configuration (BOOT_CFG1–0) pins in Table 5. Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

Table 5. Boot Mode Selection

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Parallel Port Boot via EPROM
11	Reserved

Phase-Locked Loop

The processors use an on-chip phase-locked loop (PLL) to generate the internal clock for the core. On power-up, the CLK_CFG1–0 pins are used to select ratios of 32:1, 16:1, and 6:1. After booting, numerous other ratios can be selected via software control.

The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 1, 2, 4, and 8.

Power Supplies

The processor has a separate power supply connection for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.2 V requirement for K, B, and Y grade models, and the 1.0 V requirement for Y models. (For information on the temperature ranges offered for this product, see Operating Conditions on Page 14, Package Information on Page 15, and Ordering Guide on Page 51.) The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 3. (A recommended ferrite chip is the muRata BLM18AG102SN1D). To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 3 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

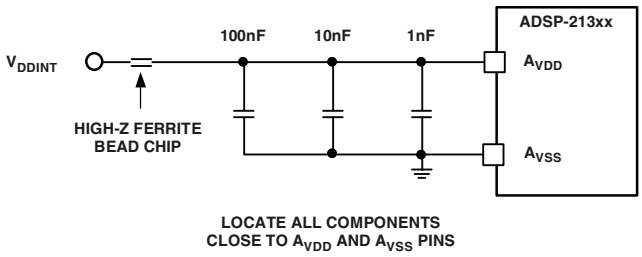


Figure 3. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices' DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processor to monitor and control the target board processor during emulation. Analog Devices' DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate *Emulator Hardware User's Guide*.

DEVELOPMENT TOOLS

The processor is supported with a complete set of CROSSCORE®† software and hardware development tools, including Analog Devices emulators and VisualDSP++®‡ development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-2136x processors.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The SHARC has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the SHARC development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

† CROSSCORE is a registered trademark of Analog Devices, Inc.

‡ VisualDSP++ is a registered trademark of Analog Devices, Inc.

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

Use the expert linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the processor or external memory with a drag of the mouse and examine runtime stack and heap usage. The expert linker is fully compatible with the existing linker definition file (LDF), allowing the developer to move between the graphical and textual environments.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC processor PC plug-in cards. Third party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG test access port (TAP) on each JTAG processor. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *Analog Devices JTAG Emulation Technical Reference (EE-68)* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Evaluation Kit

Analog Devices offers a range of EZ-KIT Lite®† evaluation platforms to use as a cost-effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite platform includes an evaluation board along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board flash device to store user-specific boot code, enabling the board to run as a standalone unit without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom defined system. Connecting one of Analog Devices' JTAG emulators to the EZ-KIT Lite board enables high speed, nonintrusive emulation.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the processor's architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Hardware Reference* and the *ADSP-2136x SHARC Processor Programming Reference*.

† EZ-KIT Lite is a registered trademark of Analog Devices, Inc.

PIN FUNCTION DESCRIPTIONS

The processor's pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS and TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

DAI_Px, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS, $\overline{\text{TRST}}$, TDI, and AD15–0 (NOTE: These pins have pull-up resistors.)

The following symbols appear in the Type column of Table 6: A = asynchronous, G = ground, I = input, O = output, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open drain, and T = three-state, (pd) = pull-down resistor, (pu) = pull-up resistor.

Table 6. Pin Descriptions

Pin	Type	State During and After Reset	Function
AD15–0	I/O/T (pu)	Three-state with pull-up enabled	**Parallel Port Address/Data.** The ADSP-2136x parallel port and its corresponding DMA unit output addresses and data for peripherals on these multiplexed pins. The multiplex state is determined by the ALE pin. The parallel port can operate in either 8-bit or 16-bit mode. Each AD pin has a 22.5 kΩ internal pull-up resistor. See the *ADSP-2136x SHARC Processor Hardware Reference* for details of the AD pin operation. For 8-bit mode: ALE is automatically asserted whenever a change occurs in the upper 16 external address bits, ADDR23–8; ALE is used in conjunction with an external latch to retain the values of the ADDR23–8. For detailed information on I/O operations and pin multiplexing, see the *ADSP-2136x SHARC Processor Hardware Reference*.
$\overline{\text{RD}}$	O (pu)	Three-state, driven high[1]	**Parallel Port Read Enable.** $\overline{\text{RD}}$ is asserted low whenever the processor reads 8-bit or 16-bit data from an external memory device. When AD15–0 are flags, this pin remains deasserted. $\overline{\text{RD}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{WR}}$	O (pu)	Three-state, driven high[1]	**Parallel Port Write Enable.** $\overline{\text{WR}}$ is asserted low whenever the processor writes 8-bit or 16-bit data to an external memory device. When AD15–0 are flags, this pin remains deasserted. $\overline{\text{WR}}$ has a 22.5 kΩ internal pull-up resistor.
ALE	O (pd)	Three-state, driven low[1]	**Parallel Port Address Latch Enable.** ALE is asserted whenever the processor drives a new address on the parallel port address pins. On reset, ALE is active high. However, it can be reconfigured using software to be active low. When AD15–0 are flags, this pin remains deasserted. ALE has a 20 kΩ internal pull-down resistor.
FLAG[0]/$\overline{\text{IRQ0}}$/SPIFLG[0]	I/O	FLAG[0] INPUT	**FLAG0/Interrupt Request0/SPI0 Slave Select.**
FLAG[1]/$\overline{\text{IRQ1}}$/SPIFLG[1]	I/O	FLAG[1] INPUT	**FLAG1/Interrupt Request1/SPI1 Slave Select.**
FLAG[2]/$\overline{\text{IRQ2}}$/$\overline{\text{SPIFLG}}$[2]	I/O	FLAG[2] INPUT	**FLAG2/Interrupt Request 2/SPI2 Slave Select**.
FLAG[3]/TMREXP/SPIFLG[3]	I/O	FLAG[3] INPUT	**FLAG3/Timer Expired/SPI3 Slave Select.**
DAI_P20–1	I/O/T (pu)	Three-state with programmable pull-up	**Digital Audio Interface Pins**. These pins provide the physical interface to the SRU. The SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the SRU can be routed to any of these pins. The SRU provides the connection from the serial ports, input data port, precision clock generators and timers, sample rate converters and SPI to the DAI_P20–1 pins. These pins have internal 22.5 kΩ pull-up resistors which are enabled on reset. These pull-ups can be disabled in the DAI_PIN_PULLUP register.

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
SPICLK	I/O (pu)	Three-state with pull-up enabled, driven high in SPI-master boot mode	**Serial Peripheral Interface Clock Signal.** Driven by the master, this signal controls the rate at which data is transferred. The master can transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock that is active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (high). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{SPIDS}}$	I	Input only	**Serial Peripheral Interface Slave Device Select.** An active low signal used to select the processor as an SPI slave device. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode the processor's $\overline{\text{SPIDS}}$ signal can be driven by a slave device to signal to the processor (as SPI master) that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single-master, multiple-slave configuration where flag pins are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For processor to processor SPI interaction, any of the master processor's flag pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the SPI slave device.
MOSI	I/O (O/D) (pu)	Three-state with pull-up enabled, driven low in SPI-master boot mode	**SPI Master Out Slave In.** If the ADSP-2136x is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the processor is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has a 22.5 kΩ internal pull-up resistor.
MISO	I/O (O/D) (pu)	Three-state with pull-up enabled	**SPI Master In Slave Out.** If the ADSP-2136x is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the processor is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has a 22.5 kΩ internal pull-up resistor. MISO can be configured as O/D by setting the OPD bit in the SPICTL register. **Note:** *Only one slave is allowed to transmit data at any given time.* To enable broadcast transmission to multiple SPI slaves, the processor's MISO pin can be disabled by setting (=1) Bit 5 (DMISO) of the SPICTL register.
BOOT_CFG1–0	I	Input only	**Boot Configuration Select.** This pin is used to select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. See the *ADSP-2136x SHARC Processor Hardware Reference* for a description of the boot modes.
CLKIN	I	Input only	**Local Clock In.** Used in conjunction with XTAL. CLKIN is the ADSP-2136x clock input. It configures the ADSP-2136x to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. The core is clocked either by the PLL output or this clock input depending on the CLK_CFG1–0 pin settings. CLKIN should not be halted, changed, or operated below the specified frequency.
XTAL	O	Output only[2]	**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
CLK_CFG1–0	I	Input only	**Core/CLKIN Ratio Control.** These pins set the start-up clock frequency. See the *ADSP-2136x SHARC Processor Hardware Reference* for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
$\overline{\text{RESETOUT}}$	O	Output only	**Reset Out.** Drives out the core reset signal to an external device.
$\overline{\text{RESET}}$	I/A	Input only	**Processor Reset.** Resets the ADSP-2136x to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Input only[3]	**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the processors.
TMS	I/S (pu)	Three-state with pull-up enabled	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TDI	I/S (pu)	Three-state with pull-up enabled	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 22.5 kΩ internal pull-up resistor.
TDO	O	Three-state[4]	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A (pu)	Three-state with pull-up enabled	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2136x. $\overline{\text{TRST}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D) (pu)	Three-state with pull-up enabled	**Emulation Status.** Must be connected to the processor's JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 22.5 kΩ internal pull-up resistor.
V_{DDINT}	P		**Core Power Supply.** Nominally +1.2 V dc for the K, B grade models, and 1.0 V dc for the Y grade models, and supplies the processor's core (13 pins).
V_{DDEXT}	P		**I/O Power Supply.** Nominally +3.3 V dc (6 pins).
A_{VDD}	P		**Analog Power Supply.** Nominally +1.2 V dc for the K, B grade models, and 1.0 V dc for the Y grade models, and supplies the processor's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 9.
A_{VSS}	G		**Analog Power Supply Return.**
GND	G		**Power Supply Return.** (54 pins)

[1] $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE are three-stated (and not driven) only when $\overline{\text{RESET}}$ is active.
[2] Output only is a three-state driver with its output path always enabled.
[3] Input only is a three-state driver with both output path and pull-up disabled.
[4] Three-state is a three-state driver with pull-up disabled.

SPECIFICATIONS

Specifications subject to change without notice.

OPERATING CONDITIONS

Parameter	Description	K Grade Min	K Grade Max	B Grade Min	B Grade Max	Y Grade Min	Y Grade Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.14	1.26	1.14	1.26	0.95	1.05	V
A_{VDD}	Analog (PLL) Supply Voltage	1.14	1.26	1.14	1.26	0.95	1.05	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	3.13	3.47	V
V_{IH}[1]	High Level Input Voltage @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	V
V_{IL}[1]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V
V_{IH_CLKIN}[2]	High Level Input Voltage @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.19	–0.5	+1.19	–0.5	+1.19	V
T_J[3, 4]	Junction Temperature 136-Ball CSP_BGA	0	+110	–40	+125	–40	+125	°C
T_J[3, 4]	Junction Temperature 144-Lead LQFP_EP	0	+110	–40	+125	–40	+125	°C

[1] Applies to input and bidirectional pins: AD15–0, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[2] Applies to input pin CLKIN.
[3] See Thermal Characteristics on Page 43 for information on thermal specifications.
[4] See *Estimating Power for the ADSP-21362 SHARC Processors (EE-277)* for further information.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1]	High Level Output Voltage	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[2]	2.4		V
V_{OL}[1]	Low Level Output Voltage	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[2]		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU}[5]	Low Level Input Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
I_{OZH}[5, 6]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZLPU}[6]	Three-State Leakage Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
$I_{DD-INTYP}$[7, 8]	Supply Current (Internal)	t_{CCLK} = Min, V_{DDINT} = Nom		800	mA
IA_{VDD}[9]	Supply Current (Analog)	A_{VDD} = Max		10	mA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.2 V		4.7	pF

[1] Applies to output and bidirectional pins: AD15–0, $\overline{RD}$, $\overline{WR}$, ALE, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{EMU}$, TDO, XTAL.
[2] See Output Drive Currents on Page 42 for typical drive current capabilities.
[3] Applies to input pins: $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, CLKIN.
[4] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[5] Applies to three-stateable pins: FLAG3–0.
[6] Applies to three-stateable pins with 22.5 kΩ pull-ups: AD15–0, DAI_Px, SPICLK, $\overline{EMU}$, $\overline{MISO}$, $\overline{MOSI}$.
[7] Typical internal current data reflects nominal operating conditions.
[8] See *Estimating Power for the ADSP-21362 SHARC Processors (EE-277)* for further information.
[9] Characterized, but not tested.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 4 provides details about the package branding for the ADSP-2136x processor. For a complete listing of product availability, see Ordering Guide on Page 51.

Figure 4. Typical Package Brand

Table 7. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See *Estimating Power for the ADSP-21362 SHARC Processors (EE-277)* for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 43.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 8 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	125°C

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 38 on Page 42 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 5). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Voltage Controlled Oscillator

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 11.

- The product of CLKIN and PLLM must never exceed 1/2 f_{VCO} (max) in Table 11 in if the input divider is not enabled (INDIV = 0).

- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 11 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLN)$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLN = 1, 2, 4, 8 based on the PLLD value programmed on the PMCTL register. During reset this value is 1.

f_{INPUT} = Input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 9. All of the timing specifications for the ADSP-2136x peripherals are defined in relation to t_{PCLK}. See the peripheral specific section for each peripheral's timing information. .

Table 9. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}

Figure 5 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the *ADSP-2136x SHARC Processor Hardware Reference*.

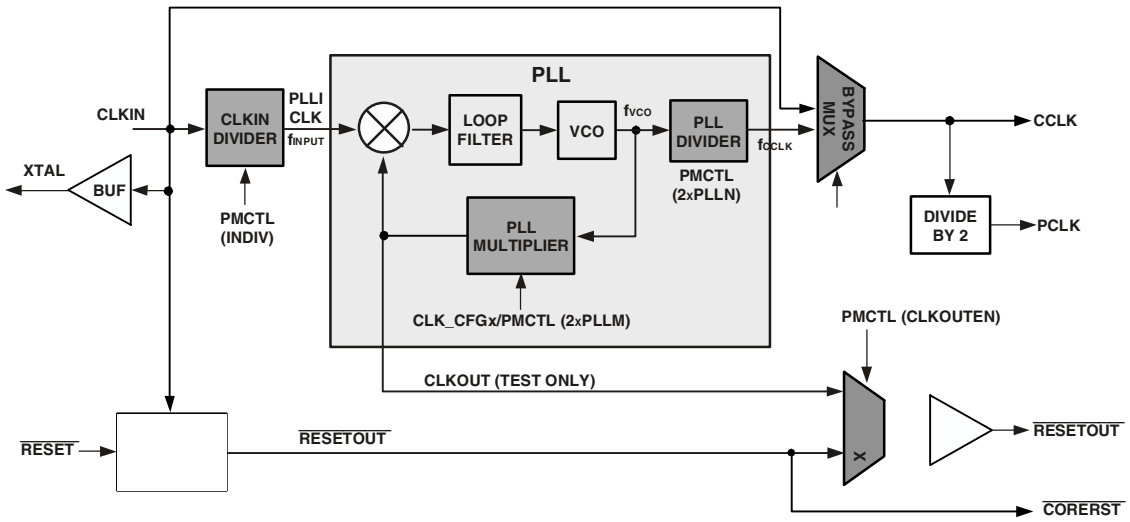


Figure 5. Core Clock and System Clock Relationship to CLKIN

Power-Up Sequencing

The timing requirements for processor startup are given in Table 10.Note that during power-up, a leakage current of approximately 200 µA may be observed on the $\overline{\text{RESET}}$ pin. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 10. Power-Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10 [2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V rails and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[4] The 4096 cycle count depends on t_{SRST} specification in Table 12. If setup time is not met, 1 additional CLKIN cycle can be added to the core reset time, resulting in 4097 cycles maximum.

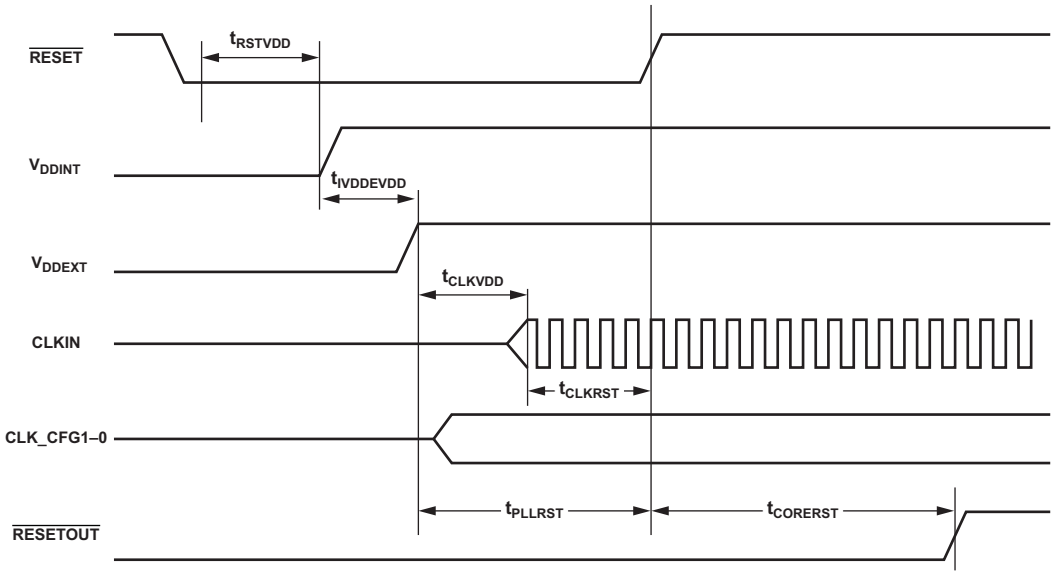


Figure 6. Power-Up Sequencing

Clock Input

Table 11. Clock Input

Parameter		200 MHz[1] Min	200 MHz[1] Max	333 MHz[2] Min	333 MHz[2] Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period	30[3]	100	18[1]	100	ns
t_{CKL}	CLKIN Width Low	12.5[1]		7.5[1]		ns
t_{CKH}	CLKIN Width High	12.5[1]		7.5[1]		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3	ns
t_{CCLK}[4]	CCLK Period	5.0[1]	10	3.0[1]	10	ns
f_{VCO}[5]	VCO Frequency	200	600	200	800	MHz
t_{CKJ}[6,7]	CLKIN Jitter Tolerance	–250	+250	–250	+250	ps

[1] Applies to all 200 MHz models. See Ordering Guide on Page 51.
[2] Applies to all 333 MHz models. See Ordering Guide on Page 51.
[3] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[4] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[5] See Figure 5 on Page 16 for VCO diagram.
[6] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[7] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

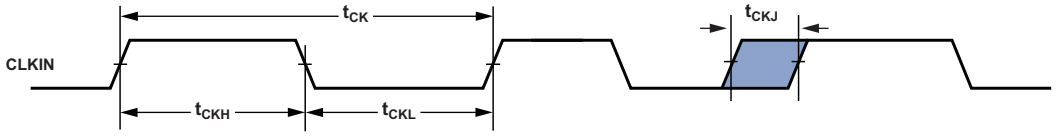


Figure 7. Clock Input

Clock Signals

The processor can use an external clock or a crystal. See the CLKIN pin description in Table 6 on Page 11. The user application program can configure the processor to use its internal clock generator by connecting the necessary components to the CLKIN and XTAL pins. Figure 8 shows the component connections used for a fundamental frequency crystal operating in parallel mode.

Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 266.72 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

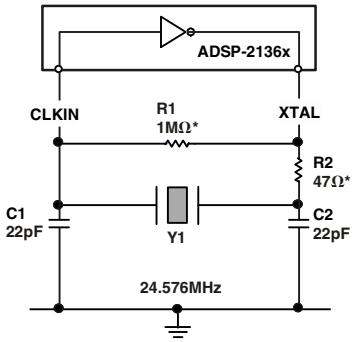


Figure 8. 333 MHz Operation (Fundamental Mode Crystal)

Reset

Table 12. Reset

Parameter		Min	Unit
Timing Requirements			
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4t_{CK}$	ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

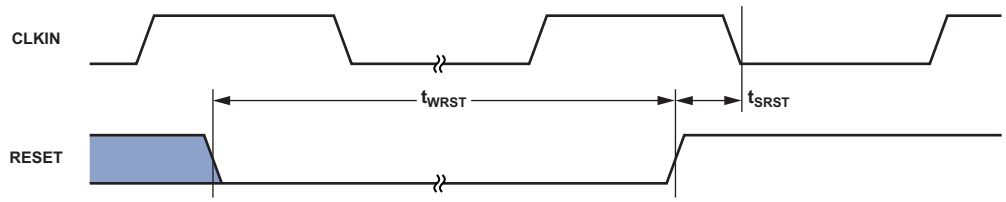


Figure 9. Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts.

Table 13. Interrupts

Parameter		Min	Unit
Timing Requirement			
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$	ns

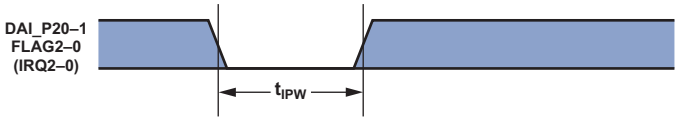


Figure 10. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP pin).

Table 14. Core Timer

Parameter		Min	Unit
Switching Characteristic			
t_{WCTIM}	TMREXP Pulse Width	$2 \times t_{PCLK} - 1$	ns

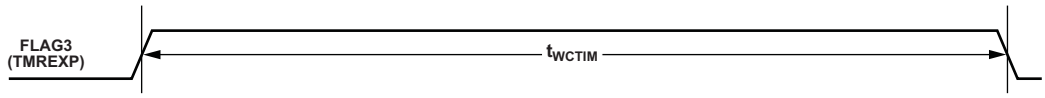


Figure 11. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 15. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2\ t_{PCLK} - 1$	$2(2^{31} - 1)\ t_{PCLK}$	ns

Figure 12. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specification provided below are valid at the DAI_P20–1 pins.

Table 16. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	2 t_{PCLK}	$2(2^{31}-1)$ t_{PCLK}	ns

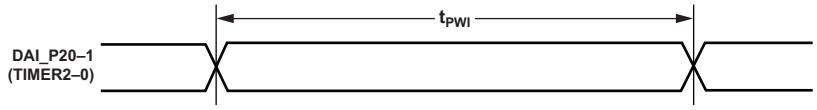


Figure 13. Timer Width Capture Timing

DAI Pin to Pin Direct Routing

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 17. DAI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	10	ns

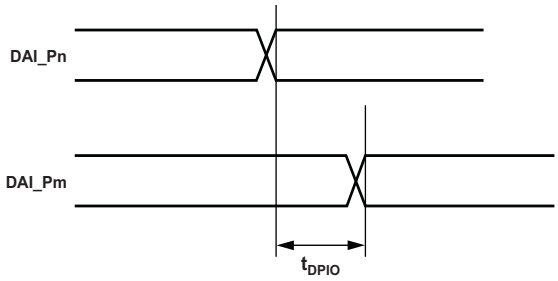


Figure 14. DAI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 through DAI_P20).

Table 18. Precision Clock Generator (Direct Pin Routing)

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$			ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5			ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3			ns
Switching Characteristics					
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	$12 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	$12 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOP}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$			ns

D = FSxDIV, PH = FSxPHASE. For more information, see the *ADSP-2136x SHARC Processor Hardware Reference*, "Precision Clock Generators" chapter.

[1] In normal mode, t_{PCGOP} (min) = $2 \times t_{PCGIP}$.

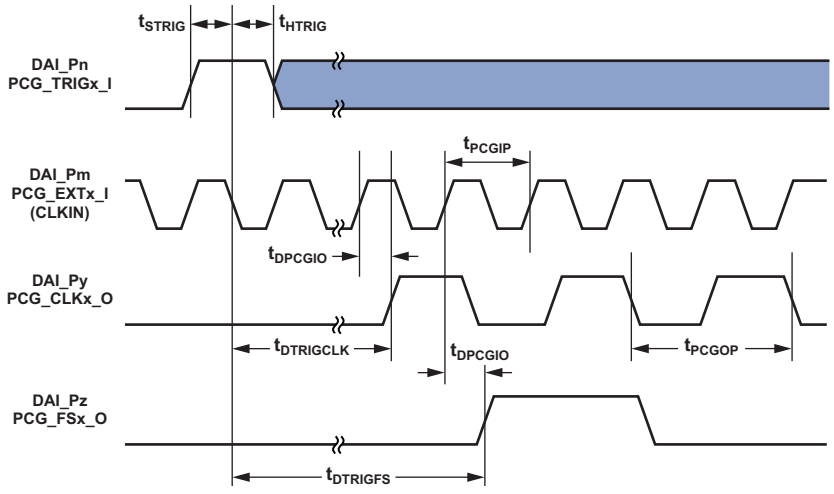


Figure 15. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG3–0 and DAI_P20–1 pins, the parallel port, and the serial peripheral interface (SPI). See Table 6, "Pin Descriptions," on Page 11 for more information on flag use.

Table 19. Flags

Parameter		Min	Unit
Timing Requirement			
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$	ns
Switching Characteristic			
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 1$	ns

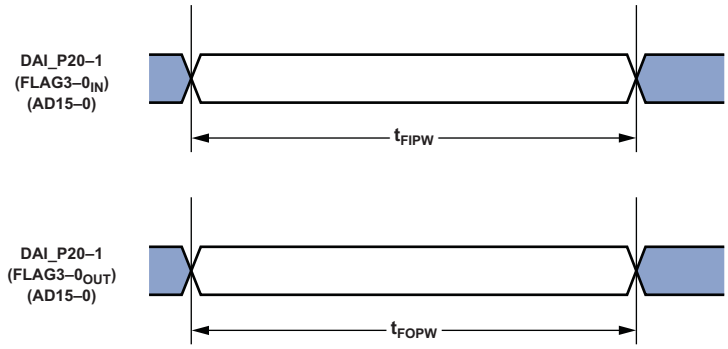


Figure 16. Flags

Memory Read—Parallel Port

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) when the processor is accessing external memory space.

Table 20. 8-Bit Memory Read Cycle

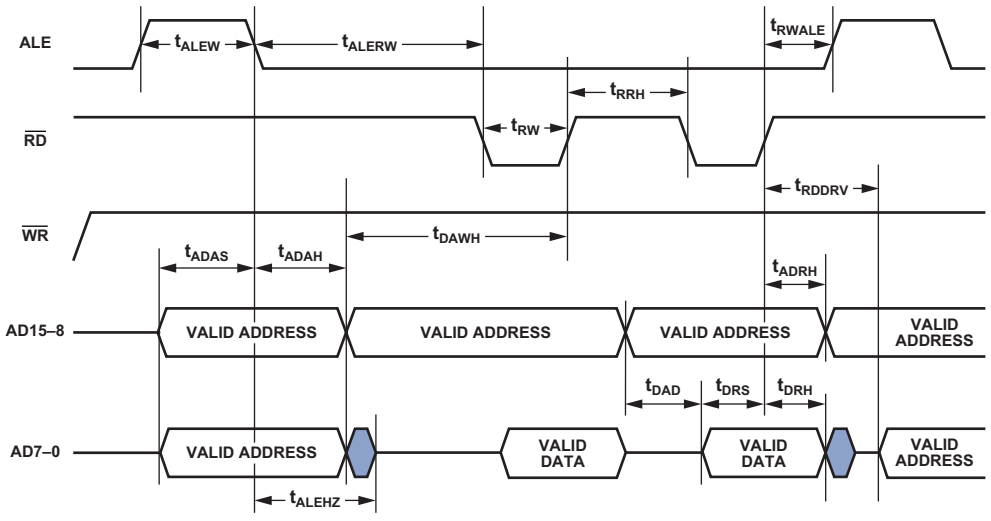
Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{DRS}	AD7–0 Data Setup Before $\overline{RD}$ High	3.3		4.5		ns
t_{DRH}	AD7–0 Data Hold After $\overline{RD}$ High	0		0		ns
t_{DAD}	AD15–8 Address to AD7–0 Data Valid		D + t_{PCLK} – 5.0		D + t_{PCLK} – 5.0	ns
Switching Characteristics						
t_{ALEW}	ALE Pulse Width	2 × t_{PCLK} – 2.0		2 × t_{PCLK} – 2.0		ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	t_{PCLK} – 2.5		t_{PCLK} – 2.5		ns
t_{RRH}	Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge	H + t_{PCLK} – 1.4		H + t_{PCLK} – 1.4		ns
t_{ALERW}	ALE Deasserted to Read Asserted	2 × t_{PCLK} – 3.8		2 × t_{PCLK} – 3.8		ns
t_{RWALE}	Read Deasserted to ALE Asserted	F + H + 0.5		F + H + 0.5		ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	t_{PCLK} – 2.3		t_{PCLK} – 2.3		ns
t_{ALEHZ}[1]	ALE Deasserted to AD7–0 Address in High-Z	t_{PCLK}	t_{PCLK} + 3.0	t_{PCLK}	t_{PCLK} + 3.8	ns
t_{RW}	$\overline{RD}$ Pulse Width	D – 2.0		D – 2.0		ns
t_{RDDRV}	AD7–0 ALE Address Drive After Read High	F + H + t_{PCLK} – 2.3		F + H + t_{PCLK} – 2.3		ns
t_{ADRH}	AD15–8 Address Hold After $\overline{RD}$ High	H		H		ns
t_{DAWH}	AD15–8 Address to $\overline{RD}$ High	D + t_{PCLK} – 4.0		D + t_{PCLK} – 4.0		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{PCLK}

H = t_{PCLK} (if a hold cycle is specified, else H = 0)

F = 7 × t_{PCLK} (if FLASH_MODE is set, else F = 0)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.



NOTES
1. MEMORY READS ALWAYS OCCUR IN GROUPS OF FOUR BETWEEN ALE CYCLES. THIS FIGURE ONLY SHOWS TWO MEMORY READS IN ORDER TO PROVIDE THE NECESSARY TIMING INFORMATION.

Figure 17. Read Cycle for 8-Bit Memory Timing

Table 21. 16-Bit Memory Read Cycle

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{DRS}	AD15–0 Data Setup Before $\overline{RD}$ High	3.3		4.5		ns
t_{DRH}	AD15–0 Data Hold After $\overline{RD}$ High	0		0		ns
Switching Characteristics						
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$		$2 \times t_{PCLK} - 2.0$		ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$		$t_{PCLK} - 2.5$		ns
t_{ALERW}	ALE Deasserted to Read Asserted	$2 \times t_{PCLK} - 3.8$		$2 \times t_{PCLK} - 3.8$		ns
t_{RRH}[2]	Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge	$H + t_{PCLK} - 1.4$		$H + t_{PCLK} - 1.4$		ns
t_{RWALE}	Read Deasserted to ALE Asserted	$F + H + 0.5$		$F + H + 0.5$		ns
t_{RDDRV}	ALE Address Drive After Read High	$F + H + t_{PCLK} - 2.3$		$F + H + t_{PCLK} - 2.3$		ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$		$t_{PCLK} - 2.3$		ns
t_{ALEHZ1}	ALE Deasserted to Address/Data15–0 in High-Z	t_{PCLK}	$t_{PCLK} + 3.0$	t_{PCLK}	$t_{PCLK} + 3.8$	ns
t_{RW}	$\overline{RD}$ Pulse Width	$D - 2.0$		$D - 2.0$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) $\times t_{PCLK}$

$H = t_{PCLK}$ (if a hold cycle is specified, else $H = 0$)

$F = 7 \times t_{PCLK}$ (if FLASH_MODE is set, else $F = 0$)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.

[2] This parameter is only available when in EMPP = 0 mode.

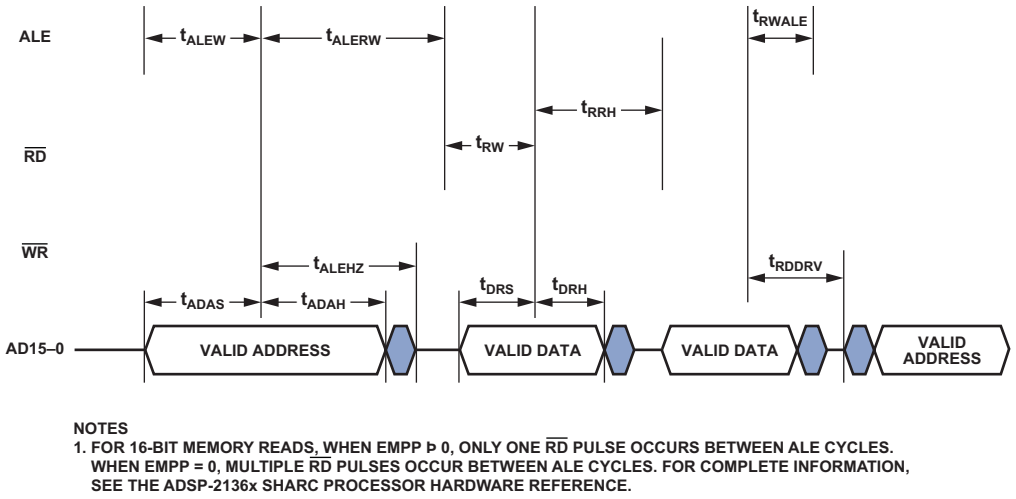


Figure 18. Read Cycle for 16-Bit Memory Timing

Memory Write—Parallel Port

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) when the processor is accessing external memory space.

Table 22. 8-Bit Memory Write Cycle

Parameter		K and B Grade Min	Y Grade Min	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$	$2 \times t_{PCLK} - 2.0$	ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.8$	$t_{PCLK} - 2.8$	ns
t_{ALERW}	ALE Deasserted to Write Asserted	$2 \times t_{PCLK} - 3.8$	$2 \times t_{PCLK} - 3.8$	ns
t_{RWALE}	Write Deasserted to ALE Asserted	H + 0.5	H + 0.5	ns
t_{WRH}	Delay Between $\overline{WR}$ Rising Edge to Next $\overline{WR}$ Falling Edge	$F + H + t_{PCLK} - 2.3$	$F + H + t_{PCLK} - 2.3$	ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 0.5$	$t_{PCLK} - 0.5$	ns
t_{WW}	$\overline{WR}$ Pulse Width	D – F – 2.0	D – F – 2.0	ns
t_{ADWL}	AD15–8 Address to $\overline{WR}$ Low	$t_{PCLK} - 2.8$	$t_{PCLK} - 3.5$	ns
t_{ADWH}	AD15–8 Address Hold After $\overline{WR}$ High	H	H	ns
t_{DWS}	AD7–0 Data Setup Before $\overline{WR}$ High	$D - F + t_{PCLK} - 4.0$	$D - F + t_{PCLK} - 4.0$	ns
t_{DWH}	AD7–0 Data Hold After $\overline{WR}$ High	H	H	ns
t_{DAWH}	AD15–8 Address to $\overline{WR}$ High	$D - F + t_{PCLK} - 4.0$	$D - F + t_{PCLK} - 4.0$	ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{PCLK}.

H = t_{PCLK} (if a hold cycle is specified, else H = 0)

F = 7 × t_{PCLK} (if FLASH_MODE is set, else F = 0). If FLASH_MODE is set, D must be ≥ 9 × t_{PCLK}.

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.

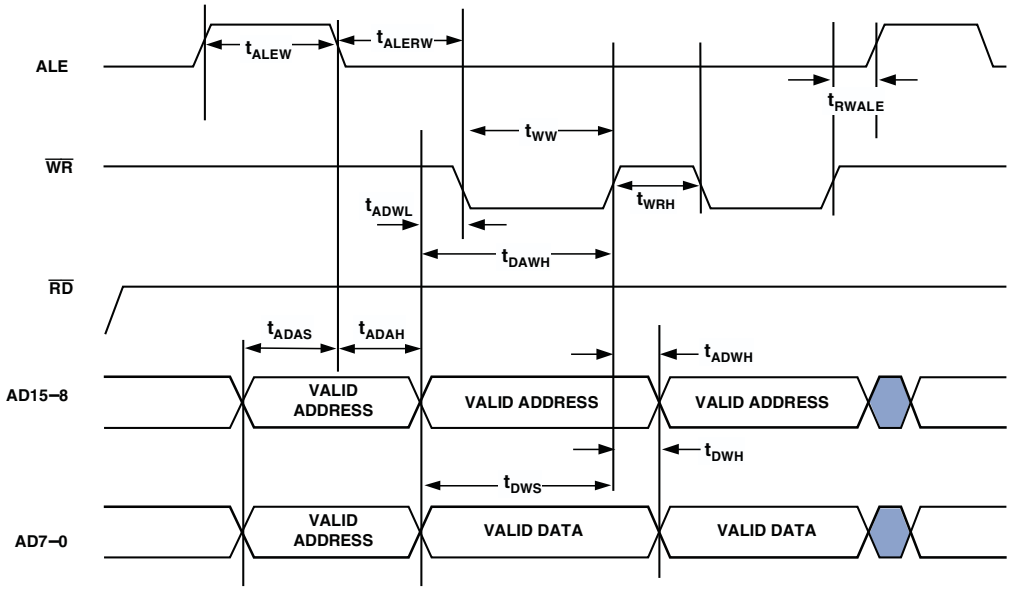


Figure 19. Write Cycle for 8-Bit Memory Timing

Table 23. 16-Bit Memory Write Cycle

Parameter		K and B Grade Min	Y Grade Min	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$	$2 \times t_{PCLK} - 2.0$	ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$	$t_{PCLK} - 2.5$	ns
t_{ALERW}	ALE Deasserted to Write Asserted	$2 \times t_{PCLK} - 3.8$	$2 \times t_{PCLK} - 3.8$	ns
t_{RWALE}	Write Deasserted to ALE Asserted	H + 0.5	H + 0.5	ns
t_{WRH}[2]	Delay Between $\overline{WR}$ Rising Edge to Next $\overline{WR}$ Falling Edge	$F + H + t_{PCLK} - 2.3$	$F + H + t_{PCLK} - 2.3$	ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$	$t_{PCLK} - 2.3$	ns
t_{WW}	$\overline{WR}$ Pulse Width	D – F – 2.0	D – F – 2.0	ns
t_{DWS}	AD15–0 Data Setup Before $\overline{WR}$ High	$D - F + t_{PCLK} - 4.0$	$D - F + t_{PCLK} - 4.0$	ns
t_{DWH}	AD15–0 Data Hold After $\overline{WR}$ High	H	H	ns

D = (the value set by the PPDUR Bits (5–1) in the PPCTL register) $\times t_{PCLK}$.

H = t_{PCLK} (if a hold cycle is specified, else H = 0)

F = $7 \times t_{PCLK}$ (if FLASH_MODE is set, else F = 0). If FLASH_MODE is set, D must be $\geq 9 \times t_{PCLK}$.

t_{PCLK} = (peripheral) clock period = $2 \times t_{CCLK}$

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.
[2] This parameter is only available when in EMPP = 0 mode.

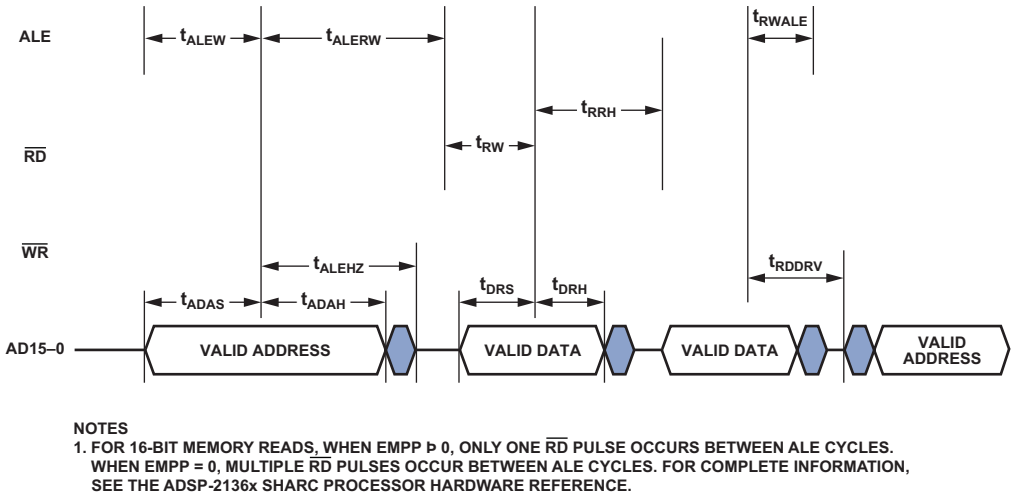


Figure 20. Write Cycle for 16-Bit Memory Timing

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync (FS) delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SCLK) width.

Serial port signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 24. Serial Ports—External Clock

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	2.5			ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5			ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 0.5$			ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$			ns
Switching Characteristics					
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)		9.5	11	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)	2			ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		9.5	11	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2			ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 25. Serial Ports—Internal Clock

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	7			ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7			ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5			ns
Switching Characteristics					
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		3	3.5	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0			ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		8	9.5	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0			ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3	4.0	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0			ns
t_{SCLKIW}	Transmit or Receive SCLK Width	$0.5t_{PCLK} - 2$	$0.5t_{PCLK} + 2$	$0.5t_{PCLK} + 2$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Table 26. Serial Ports—Enable and Three-State

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Switching Characteristics					
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2			ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		7	8.5	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1			ns

[1] Referenced to drive edge.

Table 27. Serial Ports—External Late Frame Sync

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Switching Characteristics					
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive FS with MCE = 1, MFD = 0		9	10.5	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5			ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as DSP serial mode, and MCE = 1, MFD = 0.

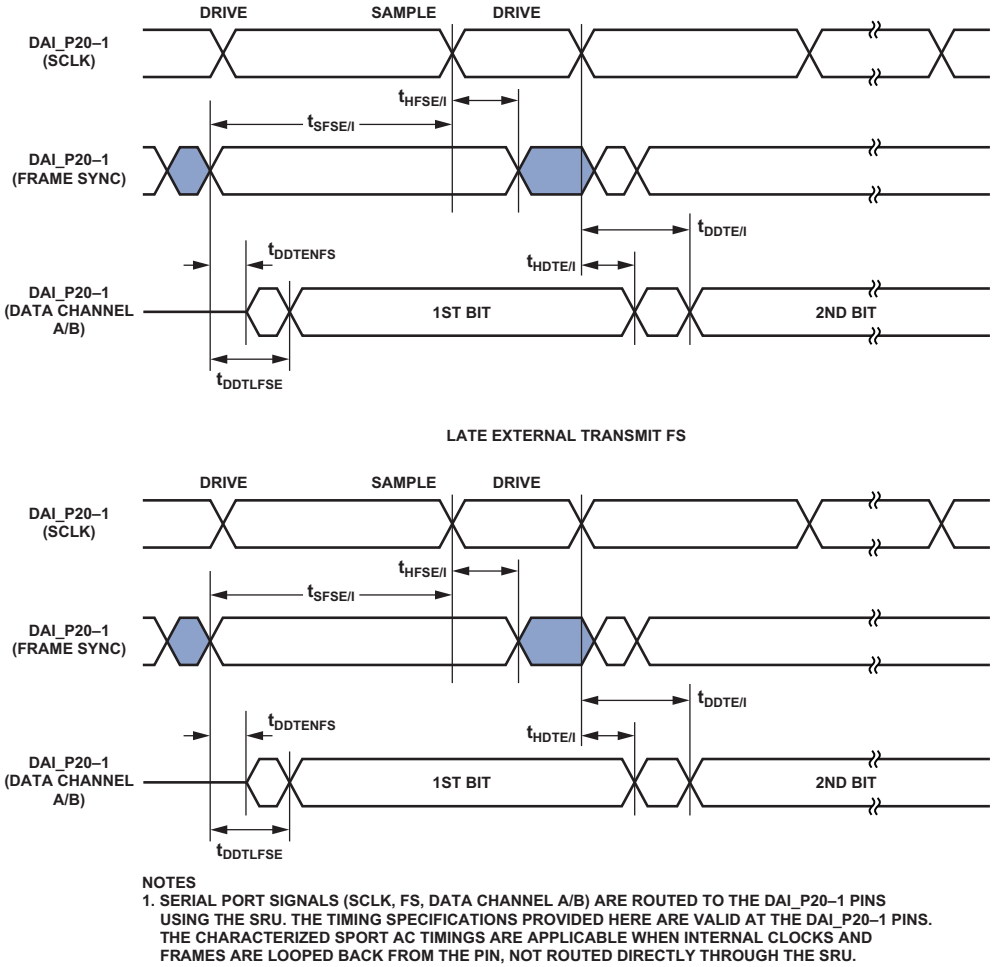


Figure 21. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

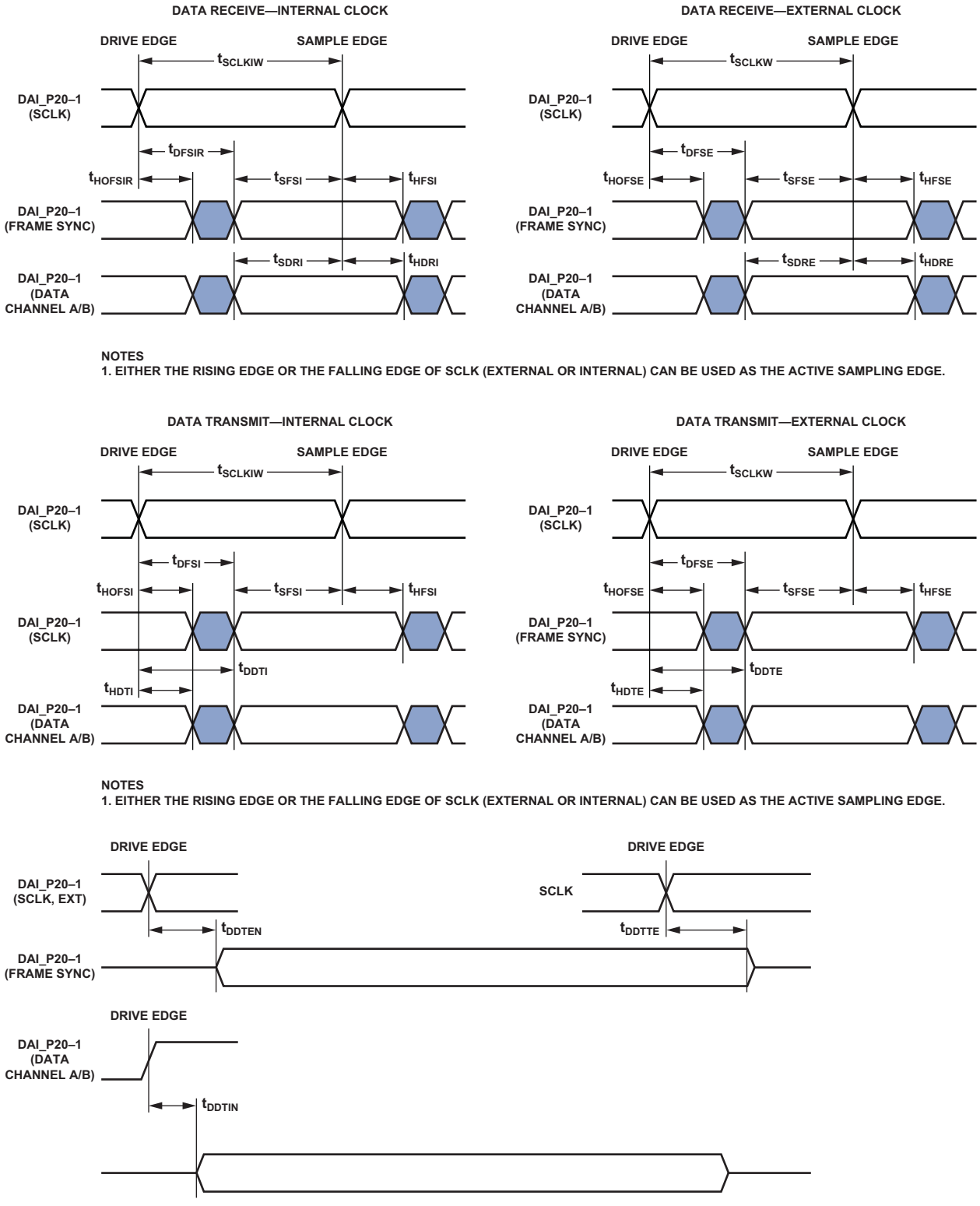


Figure 22. Serial Ports

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 28. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 28. IDP

Parameter		Min	Unit
Timing Requirements			
t_{SISFS}[1]	Frame Sync Setup Before Clock Rising Edge	3	ns
t_{SIHFS}[1]	Frame Sync Hold After Clock Rising Edge	3	ns
t_{SISD}[1]	Data Setup Before Clock Rising Edge	3	ns
t_{SIHD}[1]	Data Hold After Clock Rising Edge	3	ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$	ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$	ns

[1] The data, clock, and frame sync signals can come from any of the DAI pins. Clock and frame sync can also come via the PCGs or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

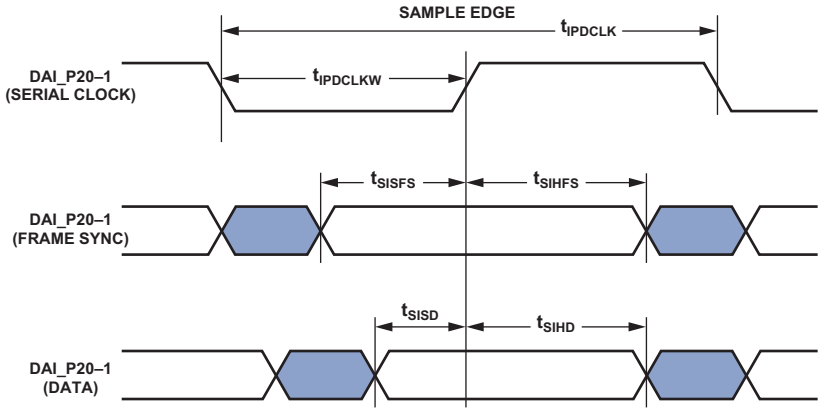


Figure 23. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 29. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the IDP, see the IDP chapter of the *ADSP-2136x SHARC Processor Hardware Reference*.

Note that the most significant 16 bits of external 20-bit PDAP data can be provided through either the parallel port AD15–0 or the DAI_P20–5 pins. The remaining 4 bits can only be sourced through DAI_P4–1. The timing below is valid at the DAI_P20–1 pins or at the AD15–0 pins.

Table 29. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Unit
Timing Requirements			
$t_{SPCLKEN}$[1]	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	2.5	ns
$t_{HPCLKEN}$[1]	PDAP_CLKEN Hold After PDAP_CLK Sample Edge	2.5	ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	3.0	ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	2.5	ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$	ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$	ns
Switching Characteristics			
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} - 1$	ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$	ns

[1] Data source pins are AD15–0 and DAI_P4–1, or DAI pins. Source pins for serial clock and frame sync are DAI pins.

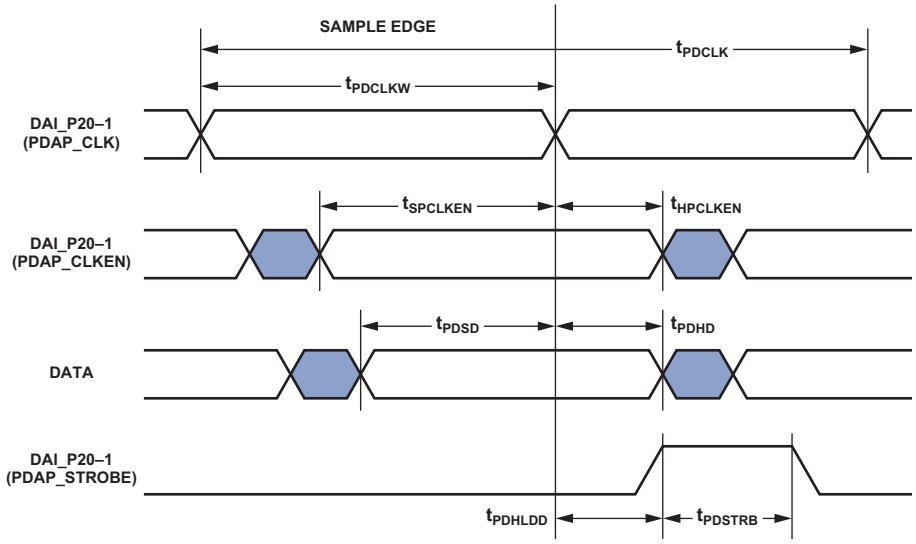


Figure 24. PDAP Timing

Pulse-Width Modulation Generators

Table 30. PWM Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK} - 2$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

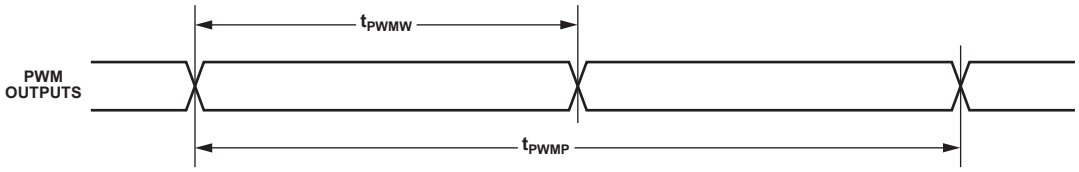


Figure 25. PWM Timing

Sample Rate Converter—Serial Input Port

The SRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 31 are valid at the DAI_P20–1 pins. This feature is not available on the ADSP-21363 models.

Table 31. SRC, Serial Input Port

Parameter		Min	Unit
Timing Requirements			
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3	ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3	ns
t_{SRCSD}[1]	SDATA Setup Before Serial Clock Rising Edge	3	ns
t_{SRCHD}[1]	SDATA Hold After Serial Clock Rising Edge	3	ns
$t_{SRCCLKW}$	Clock Width	36	ns
t_{SRCCLK}	Clock Period	80	ns

[1] The data, serial clock, and frame sync signals can come from any of the DAI pins. The serial clock, and frame sync signals can also come via the PCGs or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

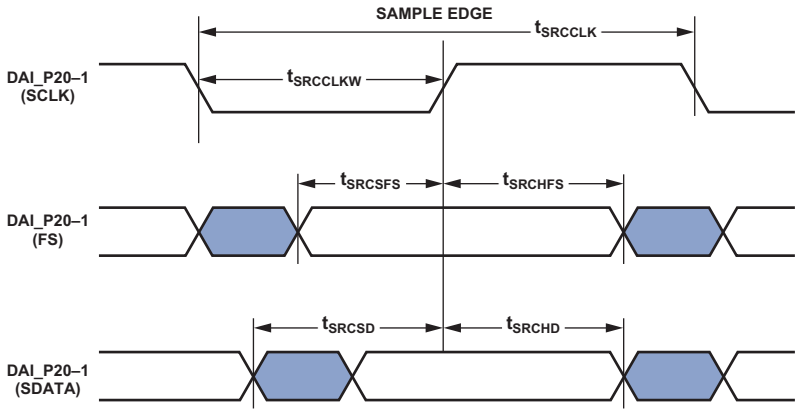


Figure 26. SRC Serial Input Port Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and should meet setup and hold times with regard to the serial clock on the output port. The serial data output has a hold time and delay specification with regard to serial clock. Note that the serial clock rising edge is the sampling edge and the falling edge is the drive edge.

Table 32. SRC, Serial Output Port

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3			ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3			ns
Switching Characteristics					
t_{SRCTDD}[1]	Transmit Data Delay After Serial Clock Falling Edge		10.5	12.5	ns
t_{SRCTDH}[1]	Transmit Data Hold After Serial Clock Falling Edge	2			ns

[1] The data, serial clock, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

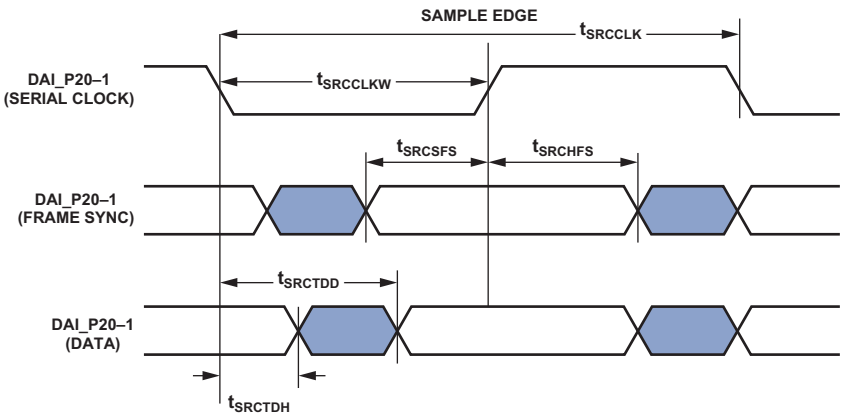


Figure 27. SRC Serial Output Port Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter. This feature is not available on the ADSP-21363 models.

S/PDIF Transmitter—Serial Input Waveforms

Figure 28 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 serial clock periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

Figure 29 shows the default I²S-justified mode. LRCLK is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to an LRCLK transition but with a single serial clock period delay.

Figure 30 shows the left-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to an LRCLK transition with no MSB delay.

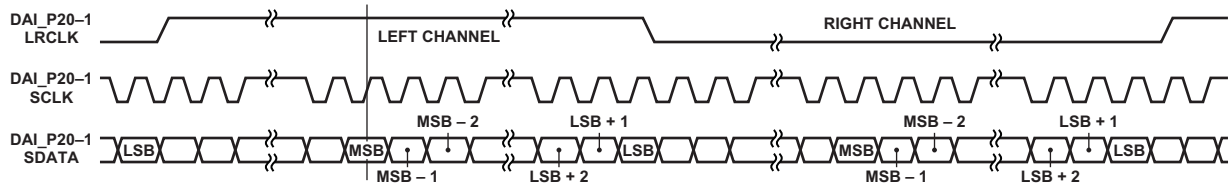


Figure 28. Right -Justified Mode

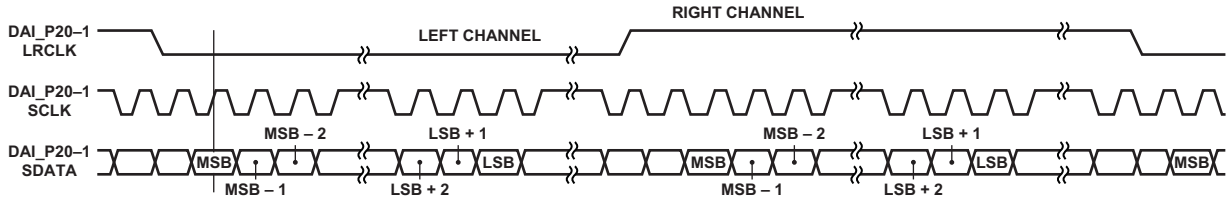


Figure 29. I²S-Justified Mode

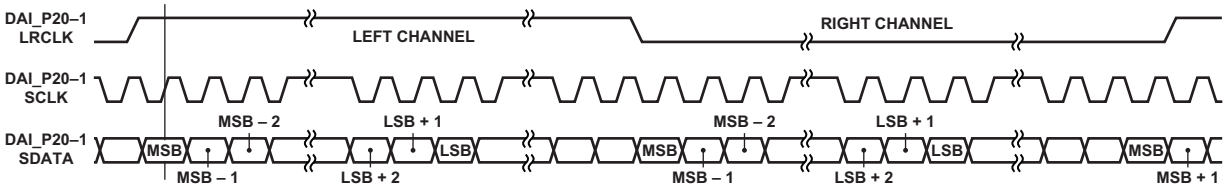


Figure 30. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the input port are given in Table 33. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 33. S/PDIF Transmitter Input Data Timing

Parameter		K and B Grade Min	Y Grade Min	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3	3	ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3	3	ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3	3	ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3	3	ns
$t_{SISCLKW}$	Clock Width	36	36	ns
t_{SISCLK}	Clock Period	80	80	ns
$t_{SITXCLKW}$	Transmit Clock Width	9	9.5	ns
$t_{SITXCLK}$	Transmit Clock Period	20	20	ns

[1] The data, serial clock, and frame sync signals can come from any of the DAI pins. The serial clock, and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

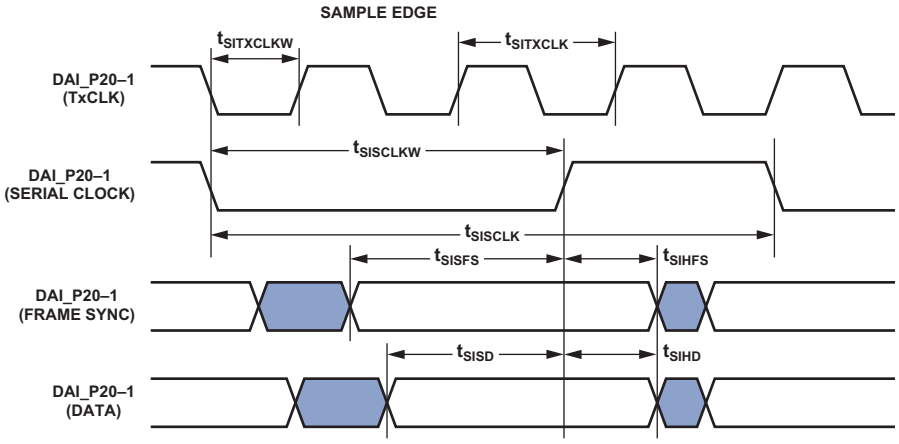


Figure 31. S/PDIF Transmitter Input Timing

Oversampling Clock (TXCLK) Switching Characteristics

S/PDIF transmitter has an oversampling clock. This TXCLK input is divided down to generate the biphase clock.

Table 34. Oversampling Clock (TXCLK) Switching Characteristics

Parameter	Max	Unit
TXCLK Frequency for TXCLK = 384 × FS	Oversampling Ratio × FS <= $1/t_{SITXCLK}$	MHz
TXCLK Frequency for TXCLK = 256 × FS	49.2	MHz
Frame Rate (FS)	192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver. This feature is not available on the ADSP-21363 processors.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 35. S/PDIF Receiver Output Timing (Internal Digital PLL Mode)

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	LRCLK Delay After Serial Clock		5	ns
t_{HOFSI}	LRCLK Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	38		ns

[1] Serial clock frequency is 64 × frame sync where FS = the frequency of LRCLK.

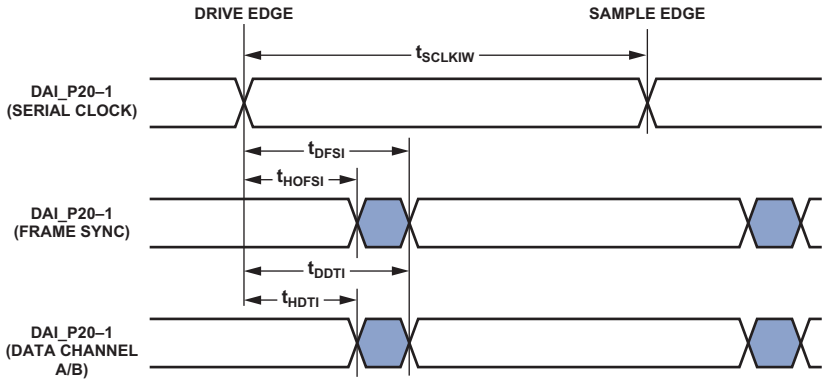


Figure 32. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

The processor contains two SPI ports. The primary has dedicated pins and the secondary is available through the DAI. The timing provided in Table 36 and Table 37 applies to both.

Table 36. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	5.2		6.2		ns
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time) (SPI2)	8.2		9.5		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		2		ns
Switching Characteristics						
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		3.0		3.0	ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time) (SPI2)		8.0		9.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	FLAG3–0IN (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2.5$		$4 \times t_{PCLK} - 3.0$		ns
t_{SDSCIM}	FLAG3–0IN (SPI Device Select) Low to First SPICLK Edge (SPI2)	$4 \times t_{PCLK} - 2.5$		$4 \times t_{PCLK} - 3.0$		ns
t_{HDSM}	Last SPICLK Edge to FLAG3–0IN High	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		$4 \times t_{PCLK} - 1$		ns

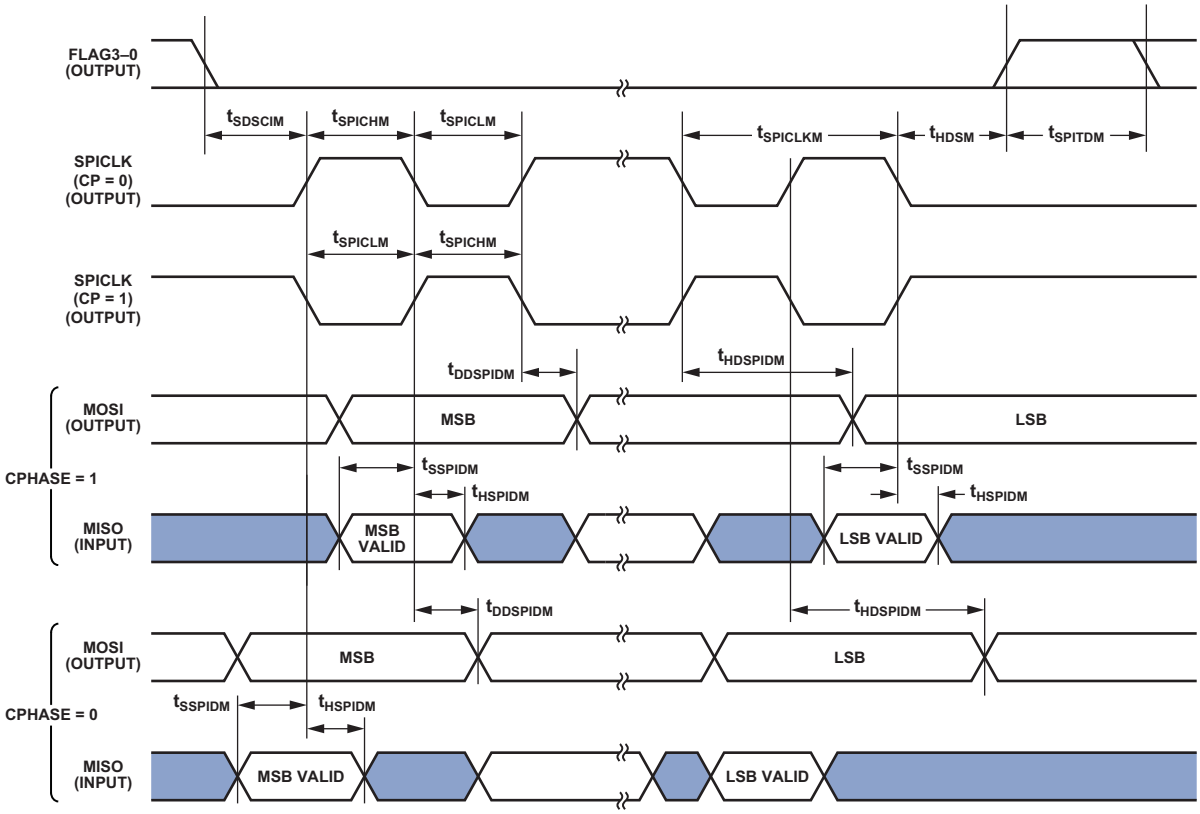


Figure 33. SPI Master Timing

SPI Interface—Slave

Table 37. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$			ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$			ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$			ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge				
	CPHASE = 0	$2 \times t_{PCLK}$			ns
	CPHASE = 1	$2 \times t_{PCLK}$			ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$			ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2			ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2			ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$			ns
Switching Characteristics					
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	5	5	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	8	9	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	5	5.5	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	8.6	10	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	11.0	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$			ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the *ADSP-2136x SHARC Processor Hardware Reference*, "Serial Peripheral Interface Port" chapter.

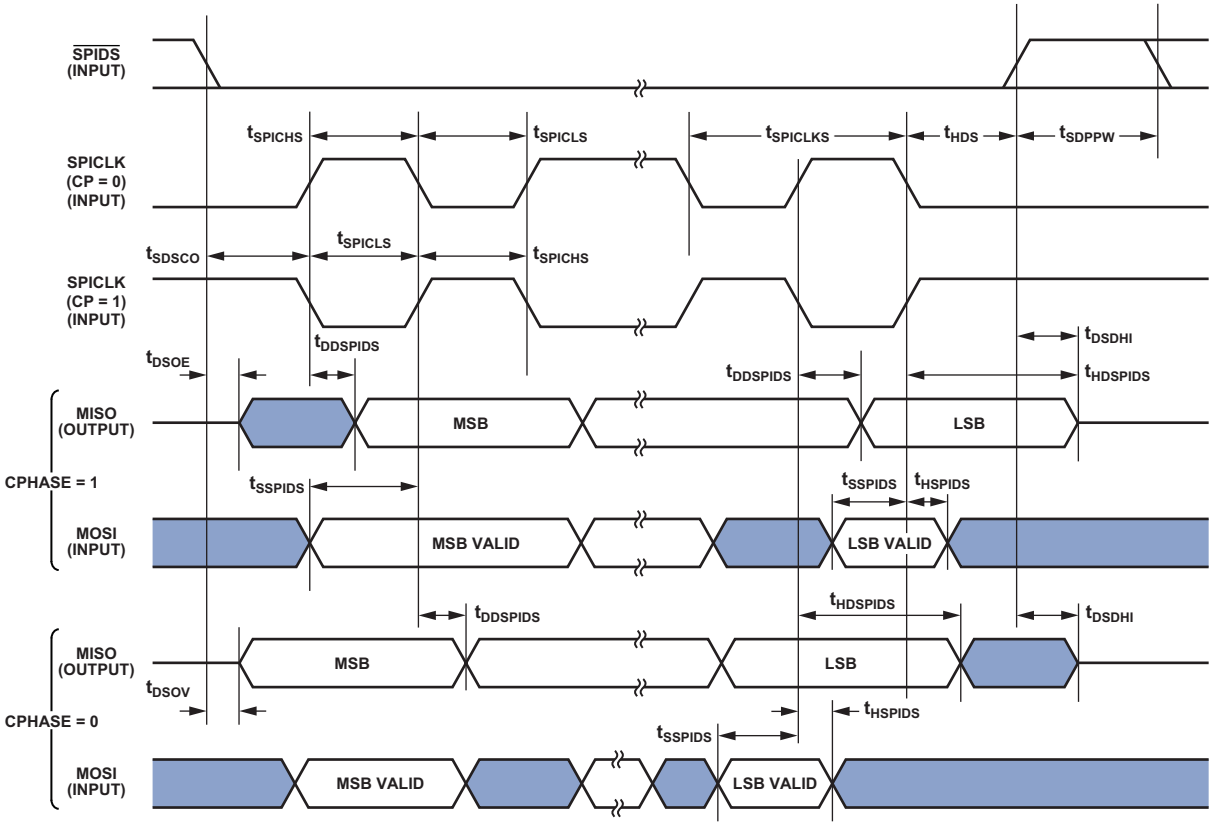


Figure 34. SPI Slave Timing

JTAG Test Access Port and Emulation

Table 38. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = ADDR15–0, $\overline{\text{SPIDS}}$, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, MISO, MOSI, SPICLK, DAI_Px, FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, ADDR15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$, ALE.

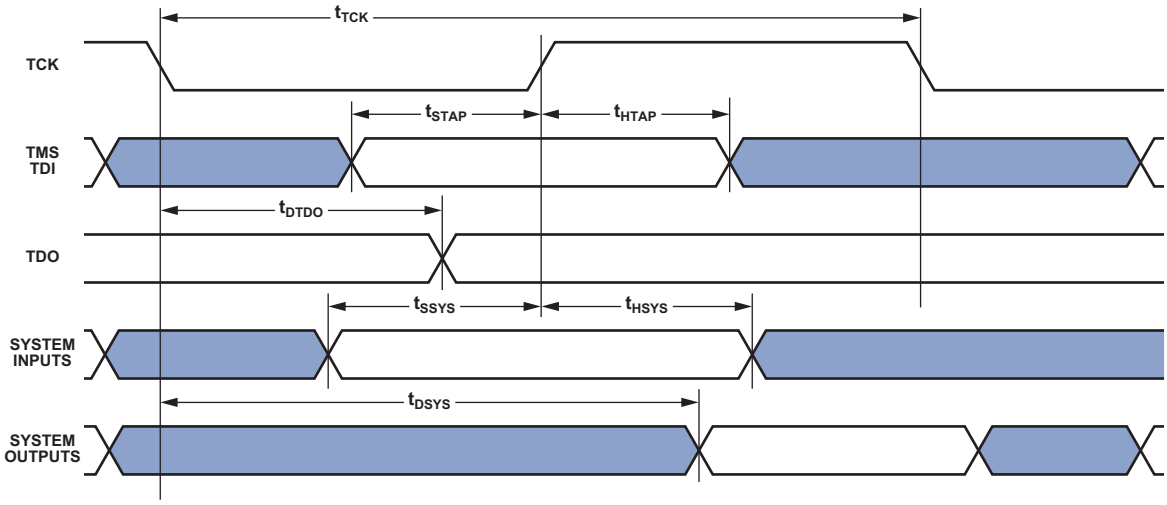


Figure 35. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 36 shows typical I-V characteristics for the output drivers of the processor. The curves represent the current drive capability of the output drivers as a function of output voltage.

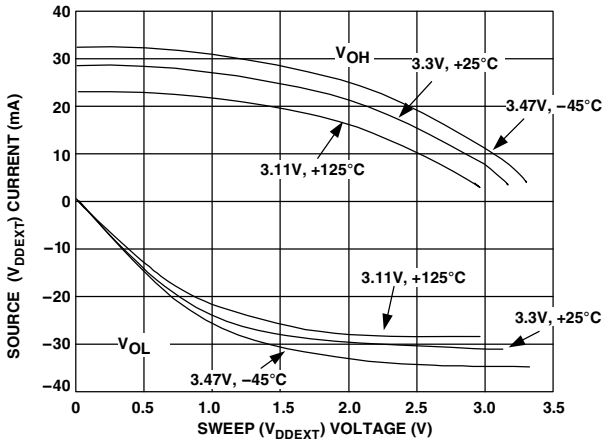


Figure 36. ADSP-2136x Typical Drive

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 12 on Page 19 through Table 38 on Page 41. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 37.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 38. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

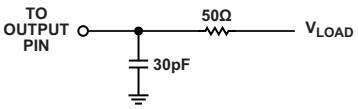


Figure 37. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

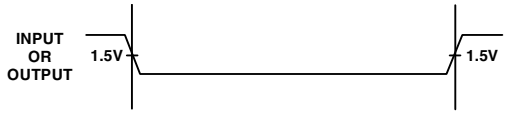


Figure 38. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 37). Figure 41 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 39, Figure 40, and Figure 41 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

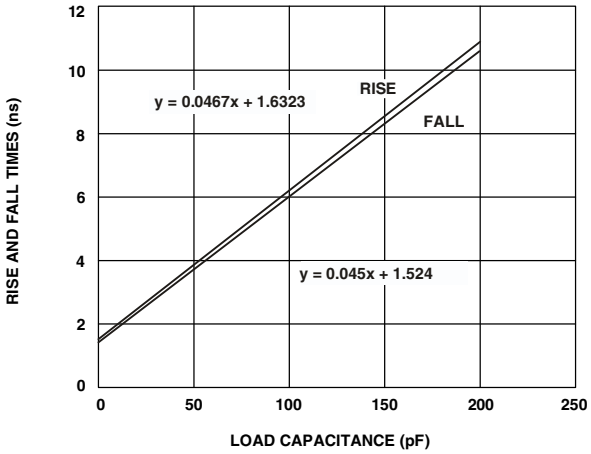


Figure 39. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

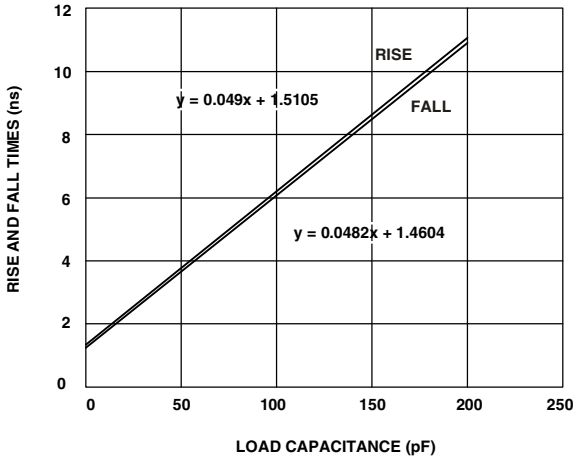


Figure 40. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

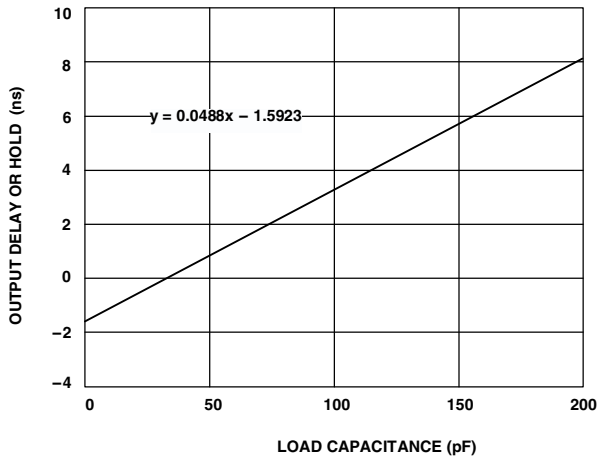


Figure 41. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions on Page 14.

Table 39 through Table 41 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board and thermal via design comply with JEDEC standards JESD51-9 (BGA) and JESD51-5 (LQFP_EP). The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

Industrial applications using the BGA package require thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

Industrial applications using the LQFP_EP package require thermal trace squares and thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-5 for more information.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 39 through Table 41.

P_D = power dissipation. See *Estimating Power for the ADSP-21362 SHARC Processors (EE-277)* for more information.

Values of θ_{JA} are provided for package comparison and PCB design considerations.

Values of θ_{JC} are provided for package comparison and PCB design considerations when an exposed pad is required. Note that the thermal characteristics values provided in Table 39 through Table 41 are modeled values.

Table 39. Thermal Characteristics for BGA (No Thermal vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	25.40	°C/W
θ_{JMA}	Airflow = 1 m/s	21.90	°C/W
θ_{JMA}	Airflow = 2 m/s	20.90	°C/W
θ_{JC}		5.07	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.140	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.330	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.410	°C/W

Table 40. Thermal Characteristics for BGA (Thermal vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	23.40	°C/W
θ_{JMA}	Airflow = 1 m/s	20.00	°C/W
θ_{JMA}	Airflow = 2 m/s	19.20	°C/W
θ_{JC}		5.00	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.130	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.300	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.360	°C/W

Table 41. Thermal Characteristics for LQFP_EP (with Exposed Pad Soldered to PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	16.80	°C/W
θ_{JMA}	Airflow = 1 m/s	14.20	°C/W
θ_{JMA}	Airflow = 2 m/s	13.50	°C/W
θ_{JC}		7.25	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.51	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.72	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.80	°C/W

144-LEAD LQFP PIN CONFIGURATIONS

The following table shows the processor's pin names and their default function after reset (in parentheses).

Table 42. LQFP Pin Assignments

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
V_{DDINT}	1	V_{DDINT}	37	V_{DDEXT}	73	GND	109
CLK_CFG0	2	GND	38	GND	74	V_{DDINT}	110
CLK_CFG1	3	$\overline{RD}$	39	V_{DDINT}	75	GND	111
BOOT_CFG0	4	ALE	40	GND	76	V_{DDINT}	112
BOOT_CFG1	5	AD15	41	DAI_P10 (SD2B)	77	GND	113
GND	6	AD14	42	DAI_P11 (SD3A)	78	V_{DDINT}	114
V_{DDEXT}	7	AD13	43	DAI_P12 (SD3B)	79	GND	115
GND	8	GND	44	DAI_P13 (SCLK3)	80	V_{DDEXT}	116
V_{DDINT}	9	V_{DDEXT}	45	DAI_P14 (SFS3)	81	GND	117
GND	10	AD12	46	DAI_P15 (SD4A)	82	V_{DDINT}	118
V_{DDINT}	11	V_{DDINT}	47	V_{DDINT}	83	GND	119
GND	12	GND	48	GND	84	V_{DDINT}	120
V_{DDINT}	13	AD11	49	GND	85	$\overline{RESET}$	121
GND	14	AD10	50	DAI_P16 (SD4B)	86	$\overline{SPIDS}$	122
FLAG0	15	AD9	51	DAI_P17 (SD5A)	87	GND	123
FLAG1	16	AD8	52	DAI_P18 (SD5B)	88	V_{DDINT}	124
AD7	17	DAI_P1 (SD0A)	53	DAI_P19 (SCLK5)	89	SPICLK	125
GND	18	V_{DDINT}	54	V_{DDINT}	90	MISO	126
V_{DDINT}	19	GND	55	GND	91	MOSI	127
GND	20	DAI_P2 (SD0B)	56	GND	92	GND	128
V_{DDEXT}	21	DAI_P3 (SCLK0)	57	V_{DDEXT}	93	V_{DDINT}	129
GND	22	GND	58	DAI_P20 (SFS5)	94	V_{DDEXT}	130
V_{DDINT}	23	V_{DDEXT}	59	GND	95	A_{VDD}	131
AD6	24	V_{DDINT}	60	V_{DDINT}	96	A_{VSS}	132
AD5	25	GND	61	FLAG2	97	GND	133
AD4	26	DAI_P4 (SFS0)	62	FLAG3	98	$\overline{RESETOUT}$	134
V_{DDINT}	27	DAI_P5 (SD1A)	63	V_{DDINT}	99	$\overline{EMU}$	135
GND	28	DAI_P6 (SD1B)	64	GND	100	TDO	136
AD3	29	DAI_P7 (SCLK1)	65	V_{DDINT}	101	TDI	137
AD2	30	V_{DDINT}	66	GND	102	$\overline{TRST}$	138
V_{DDEXT}	31	GND	67	V_{DDINT}	103	TCK	139
GND	32	V_{DDINT}	68	GND	104	TMS	140
AD1	33	GND	69	V_{DDINT}	105	GND	141
AD0	34	DAI_P8 (SFS1)	70	GND	106	CLKIN	142
$\overline{WR}$	35	DAI_P9 (SD2A)	71	V_{DDINT}	107	XTAL	143
V_{DDINT}	36	V_{DDINT}	72	V_{DDINT}	108	V_{DDEXT}	144

136-BALL BGA PIN CONFIGURATIONS

The following table shows the processor's ball names and their default function after reset (in parentheses).

Table 43. BGA Pin Assignments

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
CLK_CFG0	A01	CLK_CFG1	B01	BOOT_CFG1	C01	V_{DDINT}	D01
XTAL	A02	GND	B02	BOOT_CFG0	C02	GND	D02
TMS	A03	V_{DDEXT}	B03	GND	C03	GND	D04
TCK	A04	CLKIN	B04	GND	C12	GND	D05
TDI	A05	$\overline{TRST}$	B05	GND	C13	GND	D06
$\overline{RESETOUT}$	A06	A_{VSS}	B06	V_{DDINT}	C14	GND	D09
TDO	A07	A_{VDD}	B07			GND	D10
$\overline{EMU}$	A08	V_{DDEXT}	B08			GND	D11
MOSI	A09	SPICLK	B09			GND	D13
MISO	A10	$\overline{RESET}$	B10			V_{DDINT}	D14
$\overline{SPIDS}$	A11	V_{DDINT}	B11				
V_{DDINT}	A12	GND	B12				
GND	A13	GND	B13				
GND	A14	GND	B14				
V_{DDINT}	E01	FLAG1	F01	AD7	G01	AD6	H01
GND	E02	FLAG0	F02	V_{DDINT}	G02	V_{DDEXT}	H02
GND	E04	GND	F04	V_{DDEXT}	G13	DAI_P18 (SD5B)	H13
GND	E05	GND	F05	DAI_P19 (SCLK5)	G14	DAI_P17 (SD5A)	H14
GND	E06	GND	F06				
GND	E09	GND	F09				
GND	E10	GND	F10				
GND	E11	GND	F11				
GND	E13	FLAG2	F13				
FLAG3	E14	DAI_P20 (SFS5)	F14				

Table 43. BGA Pin Assignments (Continued)

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
AD5	J01	AD3	K01	AD2	L01	AD0	M01
AD4	J02	V_{DDINT}	K02	AD1	L02	$\overline{WR}$	M02
GND	J04	GND	K04	GND	L04	GND	M03
GND	J05	GND	K05	GND	L05	GND	M12
GND	J06	GND	K06	GND	L06	DAI_P12 (SD3B)	M13
GND	J09	GND	K09	GND	L09	DAI_P13 (SCLK3)	M14
GND	J10	GND	K10	GND	L10		
GND	J11	GND	K11	GND	L11		
V_{DDINT}	J13	GND	K13	GND	L13		
DAI_P16 (SD4B)	J14	DAI_P15 (SD4A)	K14	DAI_P14 (SFS3)	L14		
AD15	N01	AD14	P01				
ALE	N02	AD13	P02				
$\overline{RD}$	N03	AD12	P03				
V_{DDINT}	N04	AD11	P04				
V_{DDEXT}	N05	AD10	P05				
AD8	N06	AD9	P06				
V_{DDINT}	N07	DAI_P1 (SD0A)	P07				
DAI_P2 (SD0B)	N08	DAI_P3 (SCLK0)	P08				
V_{DDEXT}	N09	DAI_P5 (SD1A)	P09				
DAI_P4 (SFS0)	N10	DAI_P6 (SD1B)	P10				
V_{DDINT}	N11	DAI_P7 (SCLK1)	P11				
V_{DDINT}	N12	DAI_P8 (SFS1)	P12				
GND	N13	DAI_P9 (SD2A)	P13				
DAI_P10 (SD2B)	N14	DAI_P11 (SD3A)	P14				

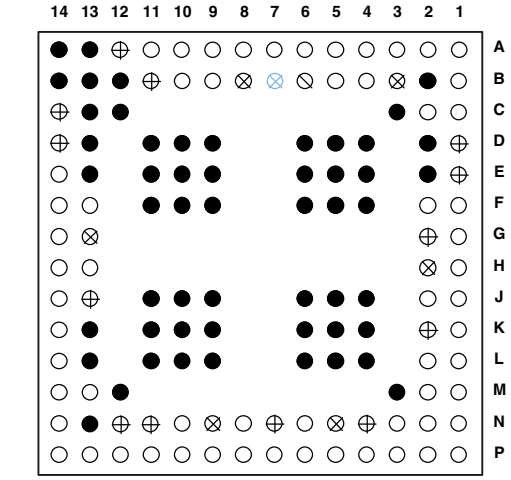


Figure 42. BGA Pin Assignments (Bottom View, Summary)

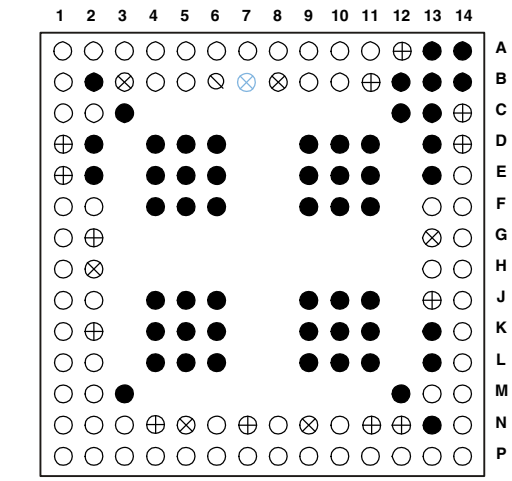


Figure 43. BGA Pin Assignments (Top View, Summary)

PACKAGE DIMENSIONS

The processor is available in 136-ball BGA and 144-lead exposed pad (LQFP_EP) packages.

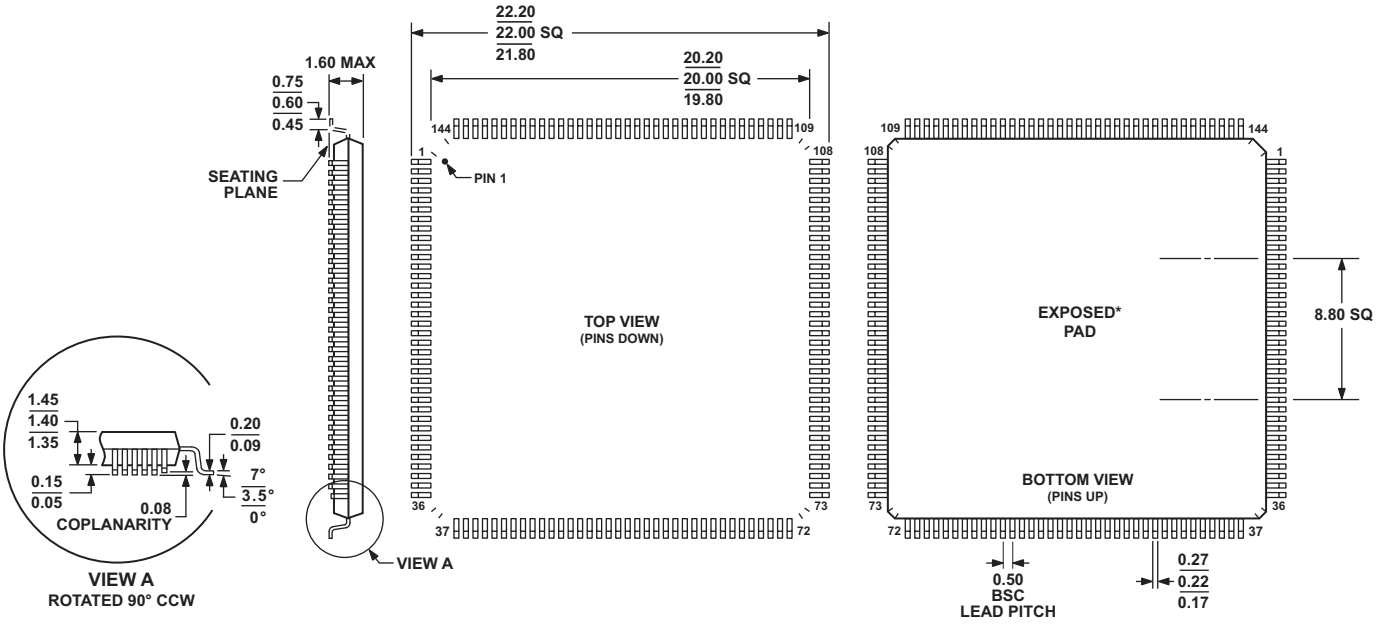


Figure 44. 144-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-144-1)
Dimensions shown in millimeters

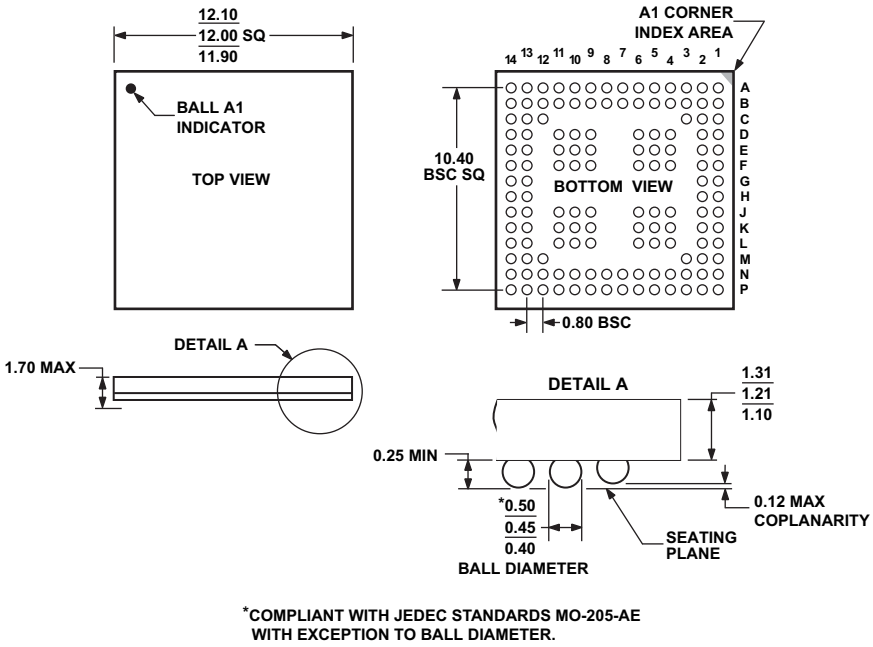


Figure 45. 136-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-136)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 44 is provided as an aid to PCB design. For industry standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 44. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
136-Ball CSP_BGA (BC-136)	Solder Mask Defined	0.40 mm diameter	0.53 mm diameter

AUTOMOTIVE PRODUCTS

An ADSP-2136x model is available for automotive applications with controlled manufacturing. Note that this special model may have specifications that differ from the general release models.

The automotive grade product shown in Table 45 is available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 45. Automotive Products

Model	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
AD21362WBSWZ104	–40°C to 85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
AD21362WYSWZ204	–40°C to 105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21363WBSWZ105	–40°C to 85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
AD21363WYSWZ205	–40°C to 105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21364WBSWZ105	–40°C to 85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
AD21364WYSWZ205	–40°C to 105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WBSWZ104A	–40°C to 85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
AD21365WYSWZ204A	–40°C to 105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21366WBSWZ105A	–40°C to 85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
AD21366WYSWZ205A	–40°C to 105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1

[1] Referenced temperature is ambient temperature.

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
ADSP-21362BBCZ-1AA[2, 3]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21362BSWZ-1AA[2, 3]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21362YSWZ-2AA[2, 3]	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21363KBC-1AA	0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21363KBCZ-1AA[3]	0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21363KSWZ-1AA[3]	0°C to +70°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21363BBC-1AA	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21363BBCZ-1AA[3]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21363BSWZ-1AA[3]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21363YSWZ-2AA[3, 5]	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21364KBC-1AA	0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21364KBCZ-1AA[3]	0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21364KSWZ-1AA[3]	0°C to +70°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21364BBC–1AA	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21364BBCZ-1AA[3]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21364BSWZ-1AA[3]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21364YSWZ-2AA[3]	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ASDP-21365BBCZ-1AA[2, 3, 4, 5]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21365BSWZ-1AA[2, 3, 4, 5]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21365YSWZ-2AA[2, 3, 4, 5]	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21365YSWZ-2CA[2, 3, 4, 5]	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21366KBC-1AA[4, 5]	0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21366KBCZ-1AA[3, 4, 5]	0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21366KSWZ-1AA[3, 4, 5]	0°C to +70°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21366BBC–1AA[4, 5]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21366BBCZ-1AA[3, 4, 5]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136
ADSP-21366BSWZ-1AA[3, 4, 5]	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21366YSWZ-2AA[3, 4, 5]	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1

[1] Referenced temperature is ambient temperature.
[2] License from DTLA required for these products.
[3] Z = RoHS compliant part.
[4] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC.
[5] License from Dolby Laboratories, Inc., and Digital Theater Systems (DTS) required for these products.

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