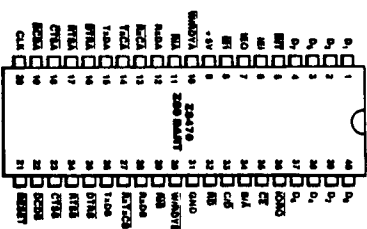
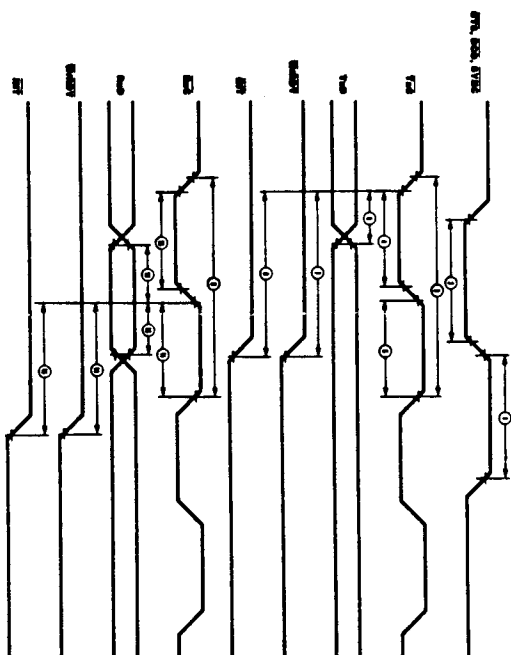


Z08470 Customer  
Procurement Spec (CPS)

The 280 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel, multichannel peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The 280 DART is used as a serial-to-parallel, parallel-to-serial converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.



### 40-Pin Dual-In-Line Package (DIP), Pin Assignments

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characterized or guaranteed by  
design.

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# DC CHARACTERISTICS

| Symbol   | Parameter                          | Min               | Max                | Units | Test Conditions        |
|----------|------------------------------------|-------------------|--------------------|-------|------------------------|
| $V_{IC}$ | Clock Input Low Voltage            | -0.2 <sup>a</sup> | +0.45 <sup>a</sup> | V     |                        |
| $V_{IC}$ | Clock Input High Voltage           | +0.8 <sup>a</sup> | +5.5 <sup>a</sup>  | V     |                        |
| $V_{IL}$ | Input Low Voltage                  | -0.2 <sup>a</sup> | +0.8 <sup>a</sup>  | V     |                        |
| $V_{IH}$ | Input High Voltage                 | +2.0 <sup>a</sup> | +5.5 <sup>a</sup>  | V     |                        |
| $V_{OL}$ | Output Low Voltage                 | +0.4 <sup>a</sup> | V                  |       | $V_{CC} = 2.0$ mA      |
| $V_{OH}$ | Output High Voltage                | +2.4 <sup>a</sup> | V                  |       | $V_{CC} = 2.0$ mA      |
| $I_{OL}$ | Output Slew Output Leakage Current | -10 <sup>a</sup>  | +10 <sup>a</sup>   | µA    | $0.4 < V_{IC} < 2.4$ V |
| $I_{OH}$ | Output Slew Output Leakage Current | -10 <sup>a</sup>  | +10 <sup>a</sup>   | µA    | $0.4 < V_{IC} < 2.4$ V |
| $I_{CC}$ | Power Supply Current               | 100 <sup>a</sup>  |                    | mA    |                        |

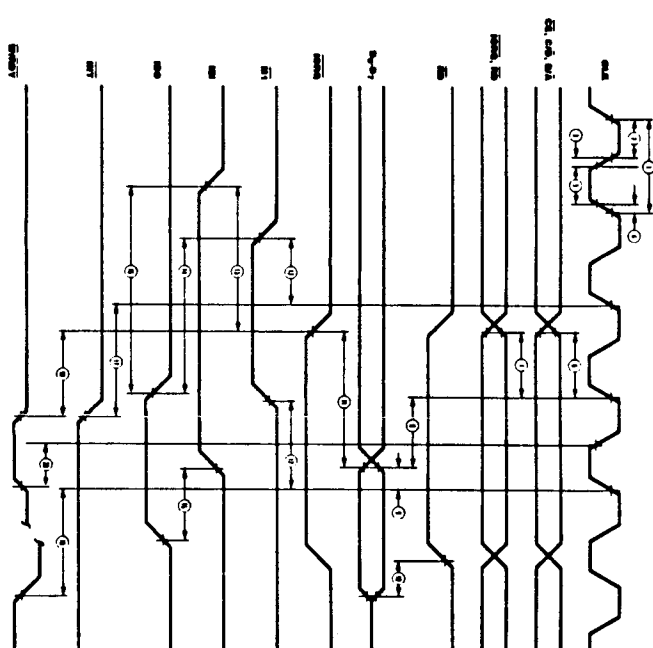
<sup>a</sup>  $V_{CC} = 0$  to  $V_{CC} = 5.5$  V,  $T_A = 25^\circ\text{C}$

<sup>b</sup> Tested  
<sup>c</sup> Guaranteed by Design  
<sup>d</sup> Guaranteed by Characterization

# AC CHARACTERISTICS<sup>a</sup>

| Number | Symbol   | Parameter                                    | Min              | Max               | Units | Test Conditions                    |
|--------|----------|----------------------------------------------|------------------|-------------------|-------|------------------------------------|
| 1      | $T_{DC}$ | Clock Cycle Time                             | 250 <sup>a</sup> | 4000 <sup>a</sup> | ns    | 180 <sup>a</sup> 4000 <sup>a</sup> |
| 2      | $T_{WH}$ | Clock Width (High)                           | 105 <sup>a</sup> | 2000 <sup>a</sup> | ns    | 70 <sup>a</sup> 2000 <sup>a</sup>  |
| 3      | $T_{WC}$ | Clock Fall Time                              | 30 <sup>a</sup>  | 30 <sup>a</sup>   | ns    | 15 <sup>a</sup>                    |
| 4      | $T_{WC}$ | Clock Rise Time                              | 30 <sup>a</sup>  | 30 <sup>a</sup>   | ns    | 15 <sup>a</sup>                    |
| 5      | $T_{WC}$ | Clock Width (Low)                            | 105 <sup>a</sup> | 2000 <sup>a</sup> | ns    | 70 <sup>a</sup> 2000 <sup>a</sup>  |
| 6      | $T_{DQ}$ | CE, C/D, B/A to Clock Setup Time             | 145 <sup>a</sup> |                   | ns    | 80 <sup>a</sup>                    |
| 7      | $T_{DQ}$ | CE, C/D, B/A to Clock Hold Time              | 115 <sup>a</sup> |                   | ns    | 80 <sup>a</sup>                    |
| 8      | $T_{DQ}$ | Clock to Data Out Delay                      | 220 <sup>a</sup> |                   | ns    | 150 <sup>a</sup>                   |
| 9      | $T_{DQ}$ | Data In to Clock Setup (Write or M1 Cycle)   | 50 <sup>a</sup>  |                   | ns    | 30 <sup>a</sup>                    |
| 10     | $T_{DQ}$ | Data In to Data Out Read Delay               | 110 <sup>a</sup> |                   | ns    | 80 <sup>a</sup>                    |
| 11     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (Read Cycle)  | 180 <sup>a</sup> |                   | ns    | 100 <sup>a</sup>                   |
| 12     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (Write Cycle) | 80 <sup>a</sup>  |                   | ns    | 75 <sup>a</sup>                    |
| 13     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (M1 Cycle)    | 140 <sup>a</sup> |                   | ns    | 120 <sup>a</sup>                   |
| 14     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (M1 Cycle)    | 180 <sup>a</sup> |                   | ns    | 180 <sup>a</sup>                   |
| 15     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (M1 Cycle)    | 100 <sup>a</sup> |                   | ns    | 70 <sup>a</sup>                    |
| 16     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (M1 Cycle)    | 100 <sup>a</sup> |                   | ns    | 70 <sup>a</sup>                    |
| 17     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (M1 Cycle)    | 200 <sup>a</sup> |                   | ns    | 150 <sup>a</sup>                   |
| 18     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (M1 Cycle)    | 210 <sup>a</sup> |                   | ns    | 175 <sup>a</sup>                   |
| 19     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (M1 Cycle)    | 120 <sup>a</sup> |                   | ns    | 100 <sup>a</sup>                   |
| 20     | $T_{DQ}$ | CE, C/D, B/A to Data Out Delay (M1 Cycle)    | 130 <sup>a</sup> |                   | ns    | 110 <sup>a</sup>                   |

<sup>a</sup> Units in microseconds (µs)  
<sup>b</sup> Tested  
<sup>c</sup> Guaranteed by Design  
<sup>d</sup> Guaranteed by Characterization



# AC CHARACTERISTICS (Continued)

| Number | Symbol   | Parameter                     | Min              | Max              | Units | Test Conditions |
|--------|----------|-------------------------------|------------------|------------------|-------|-----------------|
| 1      | $T_{WH}$ | Pulse Width (High)            | 200 <sup>a</sup> | 200 <sup>a</sup> | ns    | 2               |
| 2      | $T_{WH}$ | Pulse Width (Low)             | 200 <sup>a</sup> | 200 <sup>a</sup> | ns    | 2               |
| 3      | $T_{WC}$ | CE Cycle Time                 | 400 <sup>a</sup> | 300 <sup>a</sup> | ns    | 2               |
| 4      | $T_{WC}$ | CE Width (Low)                | 180 <sup>a</sup> | 100 <sup>a</sup> | ns    | 2               |
| 5      | $T_{WC}$ | CE Width (High)               | 180 <sup>a</sup> | 100 <sup>a</sup> | ns    | 2               |
| 6      | $T_{DQ}$ | CE to Data Delay              | 300 <sup>a</sup> | 220 <sup>a</sup> | ns    | 2               |
| 7      | $T_{DQ}$ | CE to Data Delay (Ready Mode) | 5 <sup>a</sup>   | 5 <sup>a</sup>   | ns    | 1               |
| 8      | $T_{DQ}$ | CE to Data Delay (Ready Mode) | 5 <sup>a</sup>   | 5 <sup>a</sup>   | ns    | 1               |
| 9      | $T_{DQ}$ | CE Cycle Time                 | 400 <sup>a</sup> | 300 <sup>a</sup> | ns    | 2               |
| 10     | $T_{DQ}$ | CE Width (Low)                | 180 <sup>a</sup> | 100 <sup>a</sup> | ns    | 2               |
| 11     | $T_{DQ}$ | CE Width (High)               | 180 <sup>a</sup> | 100 <sup>a</sup> | ns    | 2               |
| 12     | $T_{DQ}$ | CE to Data Delay (Ready Mode) | 0 <sup>a</sup>   | 0 <sup>a</sup>   | ns    | 2               |
| 13     | $T_{DQ}$ | CE to Data Delay (Ready Mode) | 140 <sup>a</sup> | 100 <sup>a</sup> | ns    | 2               |
| 14     | $T_{DQ}$ | CE to Data Delay (Ready Mode) | 10 <sup>a</sup>  | 13 <sup>a</sup>  | ns    | 1               |
| 15     | $T_{DQ}$ | CE to Data Delay (Ready Mode) | 10 <sup>a</sup>  | 13 <sup>a</sup>  | ns    | 1               |

<sup>a</sup> In all modes, the System Clock rate must be at least five times the maximum data rate. RESET must be active a minimum of one complete clock cycle.  
<sup>1</sup> Units equal to System Clock Period.  
<sup>2</sup> Units in microseconds (µs)  
<sup>b</sup> Tested  
<sup>c</sup> Guaranteed by Design  
<sup>d</sup> Guaranteed by Characterization