

74LVC132A

Quad 2-input NAND Schmitt trigger

Rev. 6 — 12 February 2024

Product data sheet

1. General description

The 74LVC132A provides four 2-input NAND gates with Schmitt trigger inputs. It is capable of transforming slowly-changing input signals into sharply defined, jitter-free output signals.

The inputs switch at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the input hysteresis voltage V_H .

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environment.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- 5 V tolerant inputs for interfacing with 5 V logic
- CMOS low-power consumption
- Direct interface with TTL levels
- Unlimited input rise and fall times
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

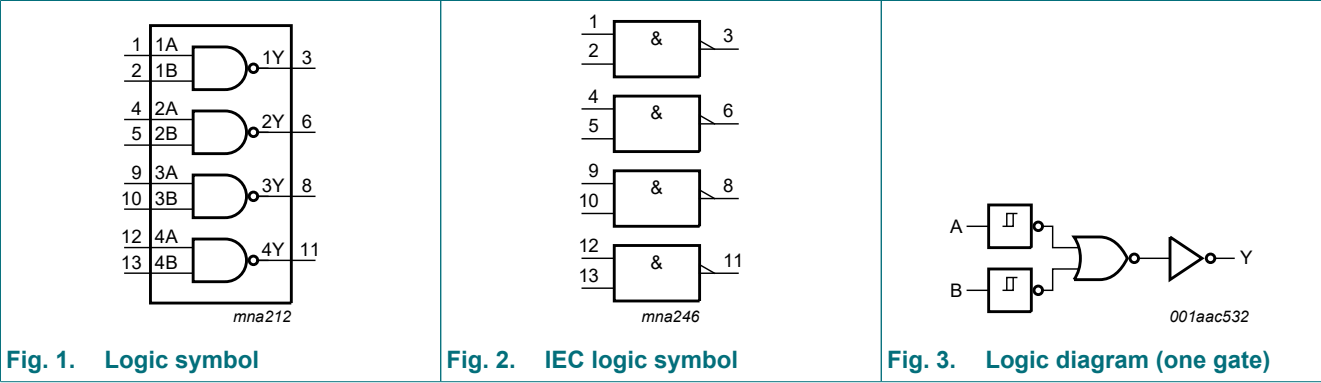
- Wave and pulse shapers for highly noisy environments
- Astable multivibrator
- Monostable multivibrator.

4. Ordering information

Table 1. Ordering information

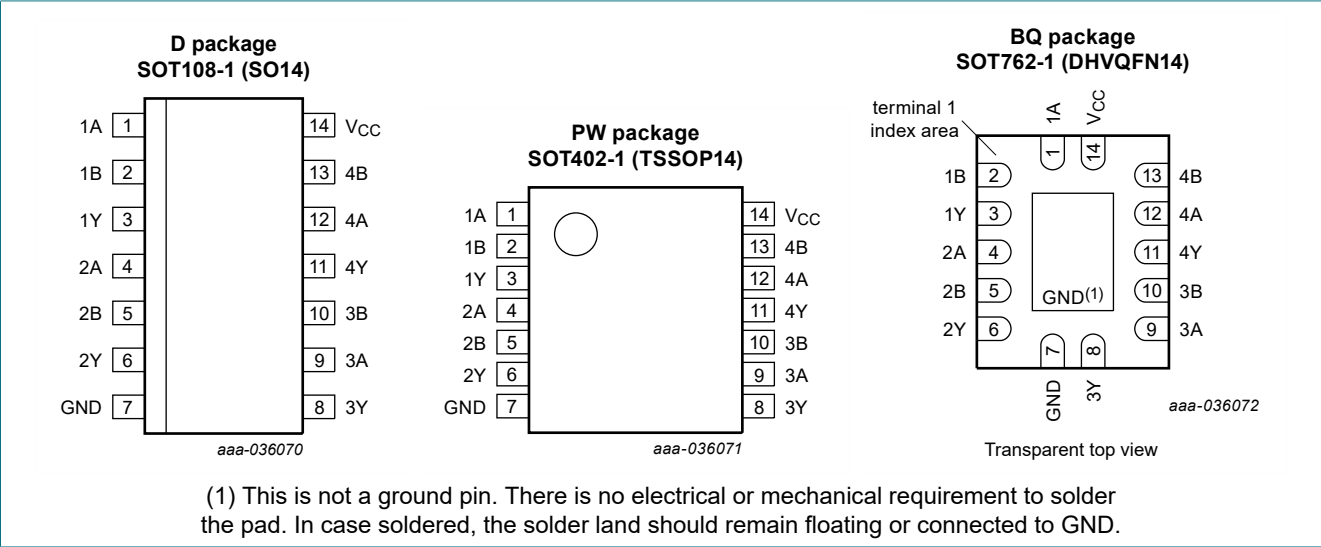
Type number	Package			
	Temperature range	Name	Description	Version
74LVC132AD	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC132APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC132ABQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
V _I	input voltage	[1]	-0.5	+6.5	V
V _O	output voltage	[2]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	V _{CC} - 0.45	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	V _{CC} - 0.5	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	-	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	V _{CC} - 0.6	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	V _{CC} - 0.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	4.0	-	pF
T_{amb} = -40 °C to +125 °C						
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.3	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	V _{CC} - 0.6	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	V _{CC} - 0.65	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.65	-	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	V _{CC} - 0.75	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	V _{CC} - 1	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	-	5	mA

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

11. Dynamic characteristics

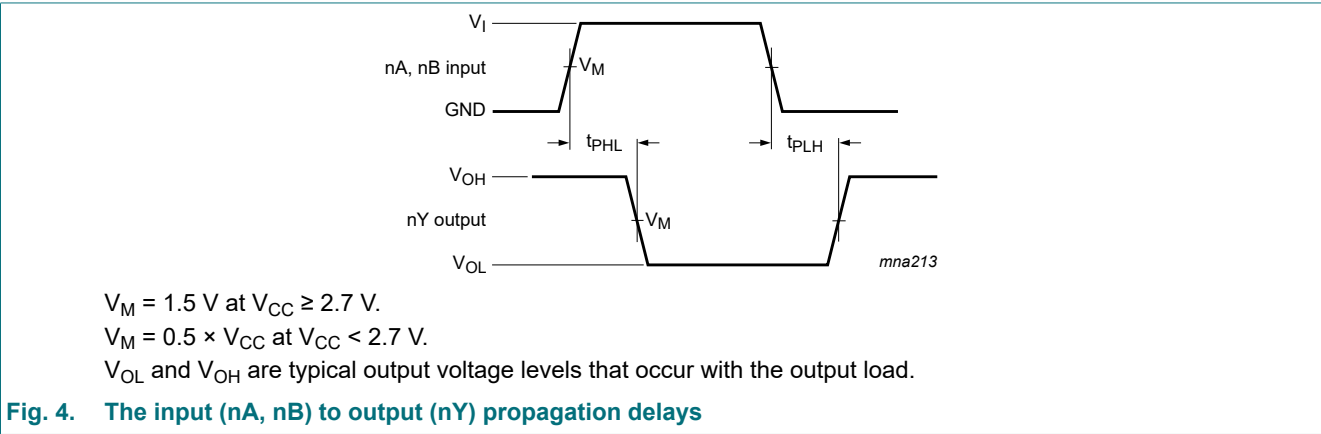
Table 7. Dynamic characteristics

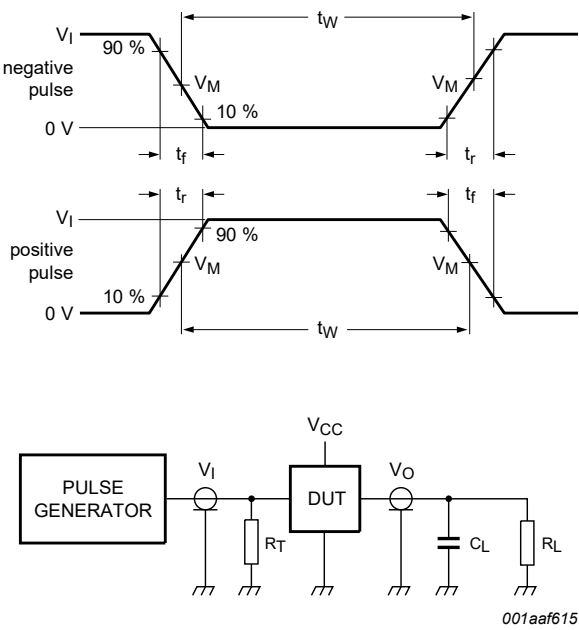
Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	nA, nB to nY; see Fig. 4 [2]						
		V _{CC} = 1.2 V	-	18.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	7.2	12.8	2.0	16.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	4.0	7.6	1.5	9.6	ns
		V _{CC} = 2.7 V	1.5	3.8	7.6	1.5	9.6	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.4	6.4	1.5	8.0	ns
t _{sk(o)}	output skew time	[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} [4]						
		V _{CC} = 1.65 V to 1.95 V	-	10.5	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	10.8	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	11.4	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:
- f_i = input frequency in MHz; f_o = output frequency in MHz;
- N = number of inputs switching;
- C_L = output load capacitance in pF;
- V_{CC} = supply voltage in V;
- Σ(C_L × V_{CC}² × f_o) = sum of outputs.

11.1. Waveforms and test circuit





Test data is given in [Table 8](#). Definitions for test circuit:
 R_L = Load resistance
 C_L = Load capacitance including jig and probe capacitance
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 5. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

12. Transfer characteristics

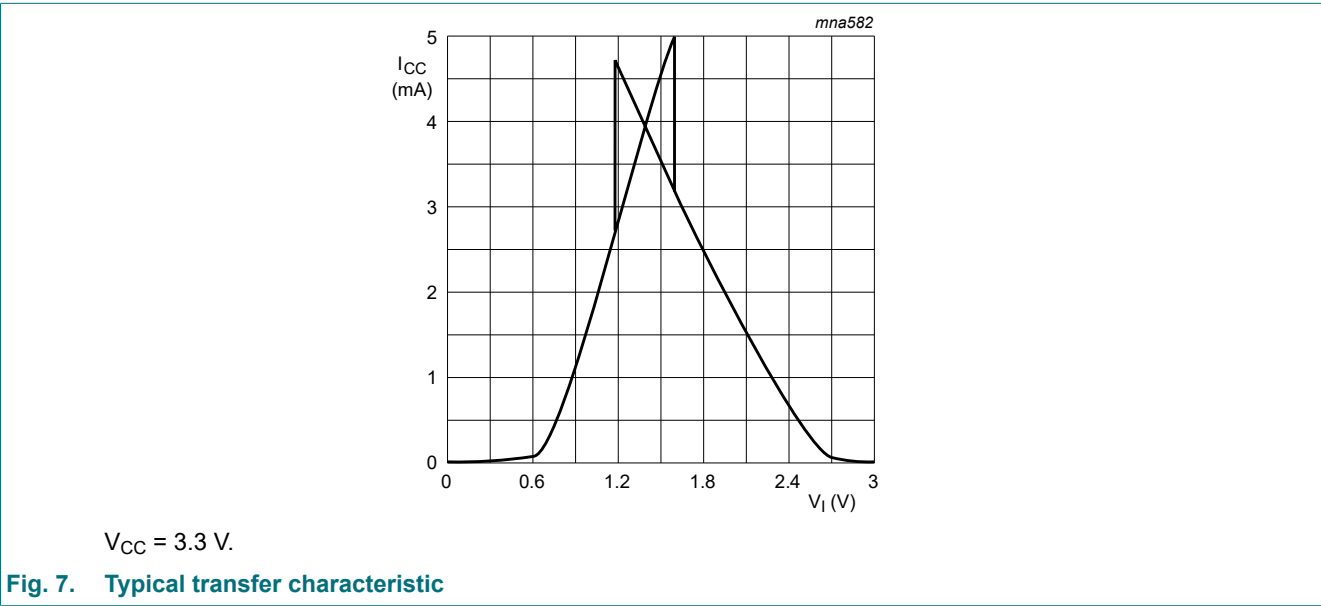
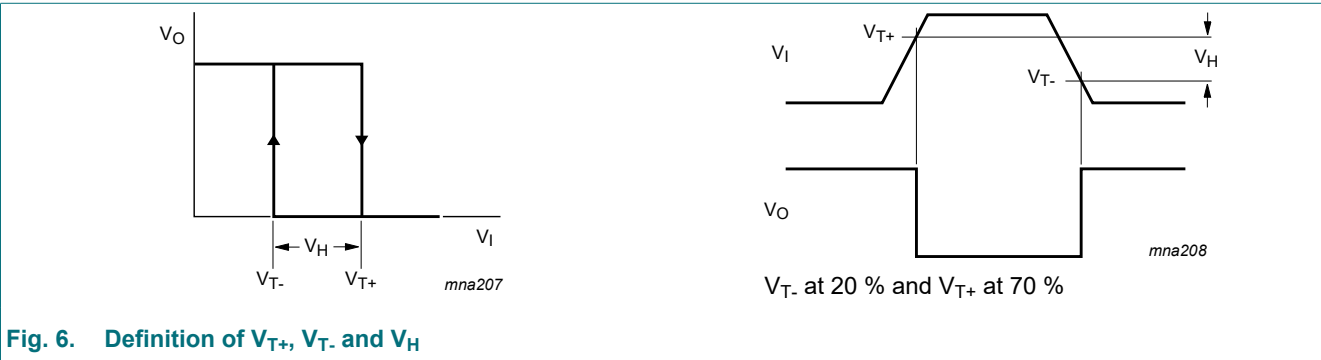
Table 9. Transfer characteristics

Voltages are referenced to GND (ground = 0 V); see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{T+}	positive-going threshold voltage	V _{CC} = 1.2 V	0.2	1.0	0.2	1.0	V
		V _{CC} = 1.65 V	0.4	1.3	0.4	1.3	V
		V _{CC} = 1.95 V	0.6	1.5	0.6	1.5	V
		V _{CC} = 2.3 V	0.8	1.7	0.8	1.7	V
		V _{CC} = 2.5 V	0.9	1.7	0.9	1.7	V
		V _{CC} = 2.7 V	1.1	2	1.1	2	V
		V _{CC} = 3 V	1.2	2	1.2	2	V
		V _{CC} = 3.6 V	1.2	2	1.2	2	V
V _{T-}	negative-going threshold voltage	V _{CC} = 1.2 V	0.12	0.75	0.12	0.75	V
		V _{CC} = 1.65 V	0.15	0.85	0.15	0.85	V
		V _{CC} = 1.95 V	0.25	0.95	0.25	0.95	V
		V _{CC} = 2.3 V	0.4	1.1	0.4	1.1	V
		V _{CC} = 2.5 V	0.4	1.2	0.4	1.2	V
		V _{CC} = 2.7 V	0.8	1.4	0.8	1.4	V
		V _{CC} = 3 V	0.8	1.5	0.8	1.5	V
		V _{CC} = 3.6 V	0.8	1.5	0.8	1.5	V
V _H	hysteresis voltage (V _{T+} - V _{T-})	V _{CC} = 1.2 V	0.1	1.0	0.1	1.0	V
		V _{CC} = 1.65 V	0.2	1.15	0.2	1.15	V
		V _{CC} = 1.95 V	0.2	1.25	0.2	1.25	V
		V _{CC} = 2.3 V	0.3	1.3	0.3	1.3	V
		V _{CC} = 2.5 V	0.3	1.3	0.3	1.3	V
		V _{CC} = 2.7 V	0.3	1.1	0.3	1.1	V
		V _{CC} = 3 V	0.3	1.2	0.3	1.2	V
		V _{CC} = 3.6 V [1]	0.3	1.2	0.3	1.2	V

[1] Typical transfer characteristic is displayed in Fig. 7.

12.1. Waveforms transfer characteristics



13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

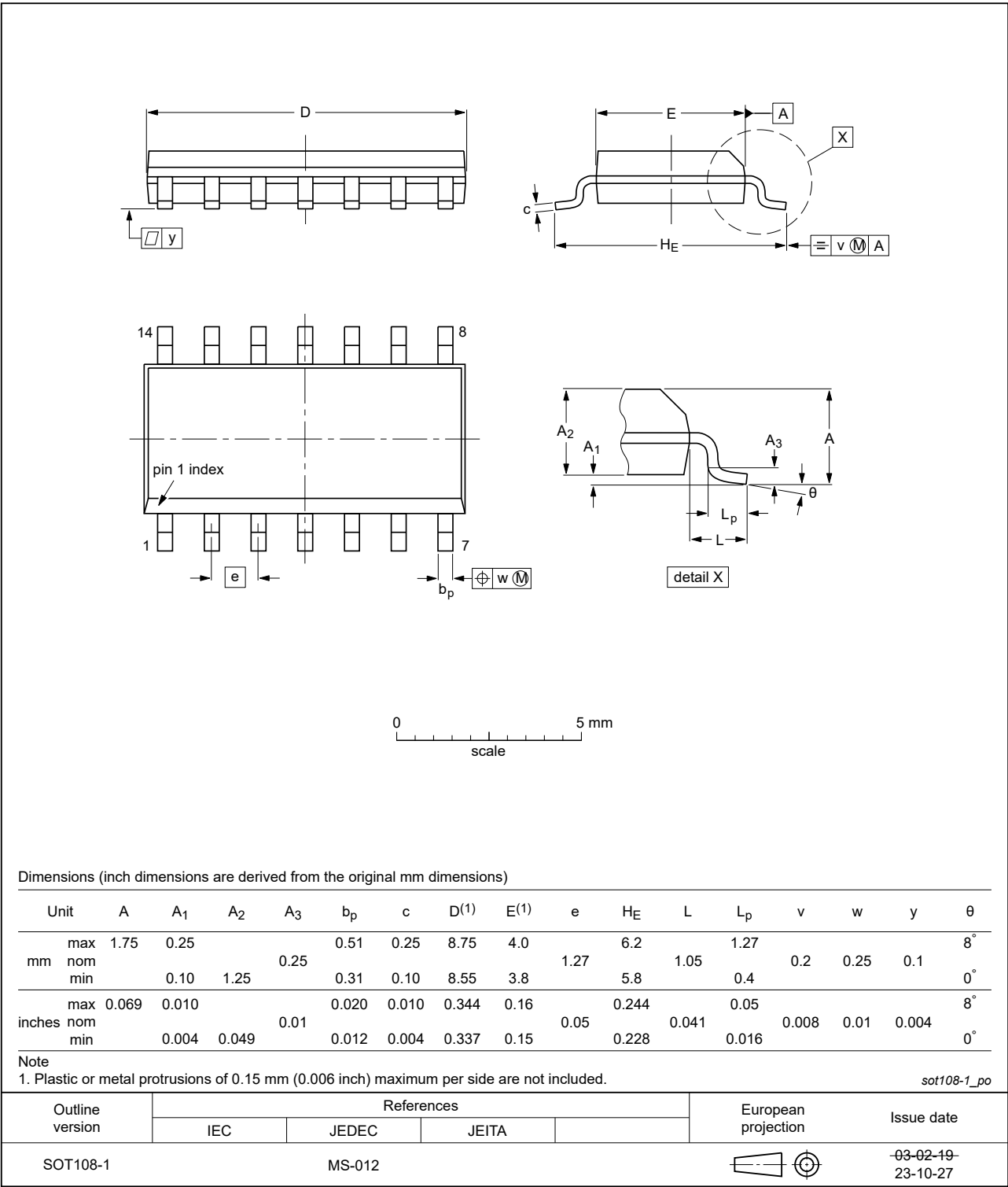


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

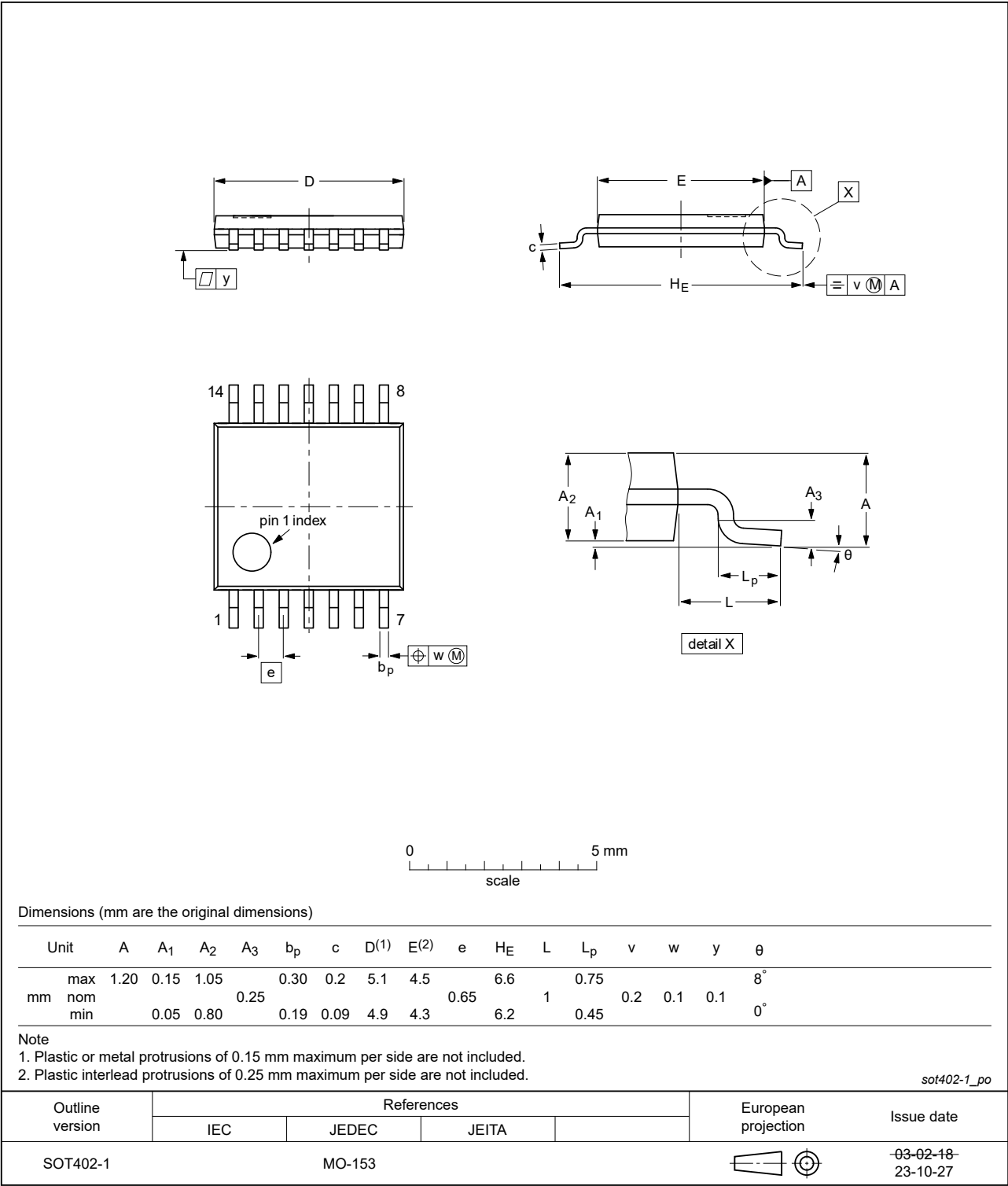


Fig. 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

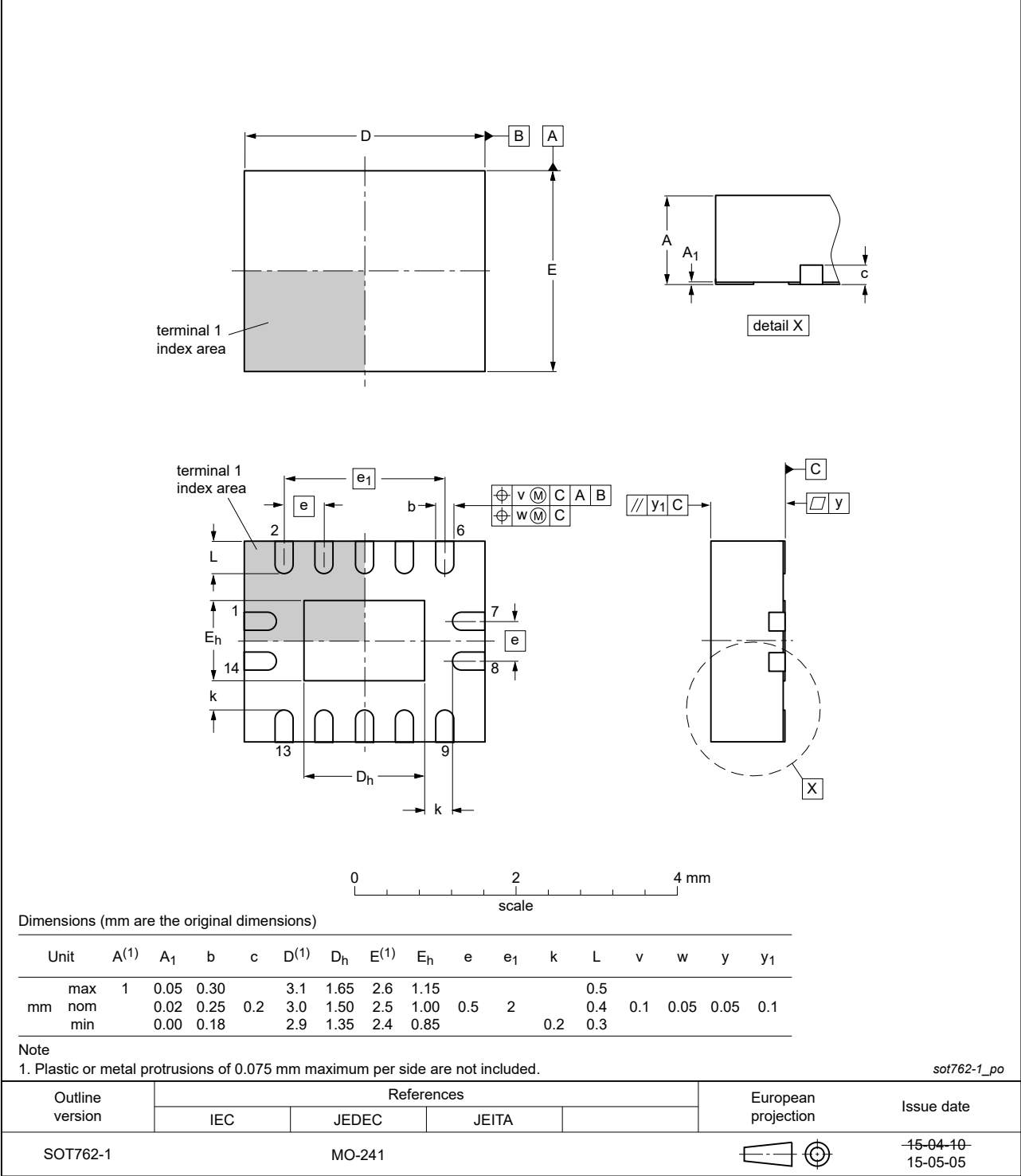


Fig. 10. Package outline SOT762-1 (DHVQFN14)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC132A v.6	20240212	Product data sheet	-	74LVC132A v.5
Modifications:	Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LVC132A v.5	20230803	Product data sheet	-	74LVC132A v.4
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC132A v.4	20200706	Product data sheet	-	74LVC132A v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. Table 4: Derating values for P_{tot} total power dissipation updated. Fig. 10: Package outline drawing SOT762-1 (DHVQFN14) updated.			
74LVC132A v.3	20111207	Product data sheet	-	74LVC132A v.2
Modifications:	Legal pages updated.			
74LVC132A v.2	20110829	Product data sheet	-	74LVC132A v.1
74LVC132A v.1	20061215	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Ordering information..... 1

5. Functional diagram.....2

6. Pinning information.....2

6.1. Pinning.....2

6.2. Pin description..... 2

7. Functional description..... 3

8. Limiting values..... 3

9. Recommended operating conditions.....3

10. Static characteristics.....4

11. Dynamic characteristics.....5

11.1. Waveforms and test circuit..... 5

12. Transfer characteristics..... 7

12.1. Waveforms transfer characteristics.....8

13. Package outline..... 9

14. Abbreviations..... 12

15. Revision history.....12

16. Legal information.....13

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