

74LCXZ16245

Low Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

The LCXZ16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.7V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The T/\bar{R} inputs determine the direction of data flow through the device. The \bar{OE} inputs disable both the A and B ports by placing them in a high impedance state.

When V_{CC} is between 0V and 1.5V, the LCXZ16245 is on the high impedance state during power-up or power-down. This places the outputs in the high impedance (Z) state preventing intermittent low impedance loading or glitching in bus oriented applications.

The LCXZ16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.7V–3.6V V_{CC} specifications provided
- 4.5 ns t_{PD} max ($V_{CC} = 3.3V$), 20 μA I_{CC} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance conforms to the requirements of JESD78
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Note 1: To ensure the high-impedance state during power up or down, \bar{OE} should be tied to V_{CC} through a pull-up resistor: the minimum value of the resistor is determined by the current-sourcing capability of the driver.

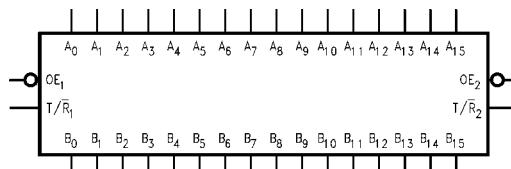
Ordering Code:

Order Number	Package Number	Package Description
74LCXZ16245GX (Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LCXZ16245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 2: BGA package available in Tape and Reel only.

Logic Symbol

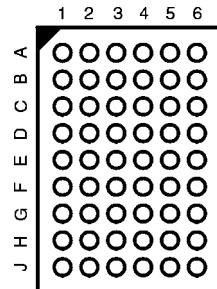


Connection Diagrams

Pin Assignment for SSOP and TSSOP

T/R ₁	1	48	\overline{OE}_1
B ₀	2	47	A ₀
B ₁	3	46	A ₁
GND	4	45	GND
B ₂	5	44	A ₂
B ₃	6	43	A ₃
V _{CC}	7	42	V _{CC}
B ₄	8	41	A ₄
B ₅	9	40	A ₅
GND	10	39	GND
B ₆	11	38	A ₆
B ₇	12	37	A ₇
B ₈	13	36	A ₈
B ₉	14	35	A ₉
GND	15	34	GND
B ₁₀	16	33	A ₁₀
B ₁₁	17	32	A ₁₁
V _{CC}	18	31	V _{CC}
B ₁₂	19	30	A ₁₂
B ₁₃	20	29	A ₁₃
GND	21	28	GND
B ₁₄	22	27	A ₁₄
B ₁₅	23	26	A ₁₅
T/R ₂	24	25	\overline{OE}_2

Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input
T/R _n	Transmit/Receive Input
A ₀ –A ₁₅	Side A Inputs or 3-STATE Outputs
B ₀ –B ₁₅	Side B Inputs or 3-STATE Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	B ₀	NC	T/R ₁	\overline{OE}_1	NC	A ₀
B	B ₂	B ₁	NC	NC	A ₁	A ₂
C	B ₄	B ₃	V _{CC}	V _{CC}	A ₃	A ₄
H	B ₆	B ₅	GND	GND	A ₅	A ₆
E	B ₈	B ₇	GND	GND	A ₇	A ₈
F	B ₁₀	B ₉	GND	GND	A ₉	A ₁₀
G	B ₁₂	B ₁₁	V _{CC}	V _{CC}	A ₁₁	A ₁₂
H	B ₁₄	B ₁₃	NC	NC	A ₁₃	A ₁₄
J	B ₁₅	NC	T/R ₂	\overline{OE}_2	NC	A ₁₅

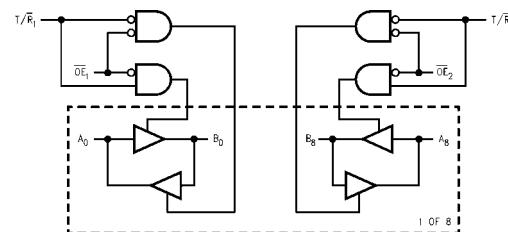
Truth Tables

Inputs		Outputs	
\overline{OE}_1	T/R ₁		
L	L	Bus B ₀ –B ₇ Data to Bus A ₀ –A ₇	
L	H	Bus A ₀ –A ₇ Data to Bus B ₀ –B ₇	
H	X	HIGH Z State on A ₀ –A ₇ , B ₀ –B ₇	

Inputs		Outputs	
\overline{OE}_2	T/R ₂		
L	L	Bus B ₈ –B ₁₅ Data to Bus A ₈ –A ₁₅	
L	H	Bus A ₈ –A ₁₅ Data to Bus B ₈ –B ₁₅	
H	X	HIGH Z State on A ₈ –A ₁₅ , B ₈ –B ₁₅	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Absolute Maximum Ratings (Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	-0.5 to +7.0		V
V_I	DC Input Voltage	-0.5 to +7.0		V
V_O	DC Output Voltage	-0.5 to +7.0 -0.5 to V_{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 4)	V
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50 +50	$V_O < GND$ $V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	± 50		mA
I_{CC}	DC Supply Current per Supply Pin	± 100		mA
I_{GND}	DC Ground Current per Ground Pin	± 100		mA
T_{STG}	Storage Temperature	-65 to +150		$^{\circ}C$

Recommended Operating Conditions (Note 5)

Symbol	Parameter	Operating	Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.7	3.6	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State 3-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$ $V_{CC} = 2.7V - 3.0V$		± 24 ± 12	mA
T_A	Free-Air Operating Temperature		-40	85	$^{\circ}C$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$		0	10	ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Unused inputs or I/O's must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12 mA$	2.7	2.2		
		$I_{OH} = -18 mA$	3.0	2.4		
		$I_{OH} = -24 mA$	3.0	2.2		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7 - 3.6		0.2	V
		$I_{OL} = 12 mA$	2.7		0.4	
		$I_{OL} = 16 mA$	3.0		0.4	
		$I_{OL} = 24 mA$	3.0		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.7 - 3.6		± 5.0	μA
I_{OZ}	3-STATE I/O Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7 - 3.6		± 5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	μA
$I_{PU/PD}$	Power-Up/Power-Down 3-STATE Output Current	$V_O = 0.5V$ to V_{CC} $V_I = V_{CC}$ or GND	0 - 1.5		± 5.0	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		225	μA
		$3.6V \leq V_I, V_O \leq 5.5V$ (Note 6)	2.7-3.6		± 225	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		500	μA

Note 6: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, R_L = 500\Omega$				Units	
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$			
		$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$			
		Min	Max	Min	Max		
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.0	4.5	1.0	5.2	ns	
t_{PLH}		1.0	4.5	1.0	5.2	ns	
t_{PZL}	Output Enable Time	1.0	6.5	1.0	7.2	ns	
t_{PZH}		1.0	6.5	1.0	7.2	ns	
t_{PLZ}	Output Disable Time	1.0	6.4	1.0	6.9	ns	
t_{PHZ}		1.0	6.4	1.0	6.9	ns	
t_{OSHL}	Output to Output Skew (Note 7)		1.0			ns	
t_{OSLH}			1.0			ns	

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	-0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	7	pF
$C_{I/0}$	Input/Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10 \text{ MHz}$	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

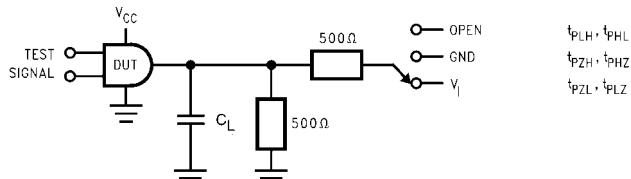
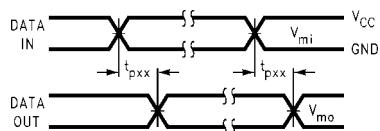
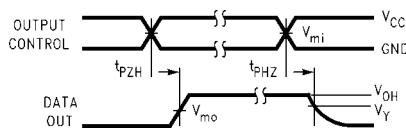


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

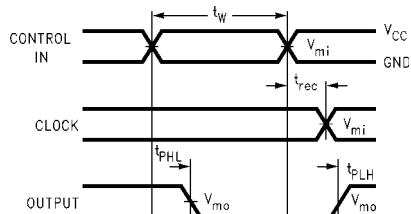
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZH}, t_{PHZ}	6V at $V_{CC} = 3.3 \pm 0.3V$, and 2.7V
t_{PZL}, t_{PLZ}	GND



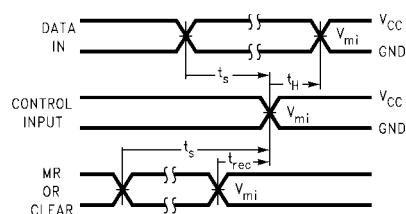
Waveform for Inverting and Non-Inverting Functions



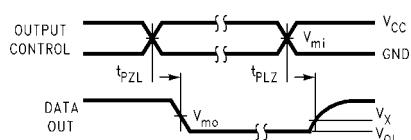
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

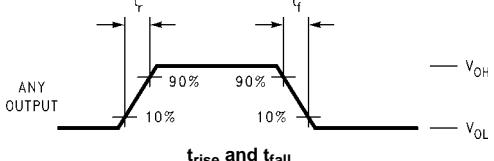
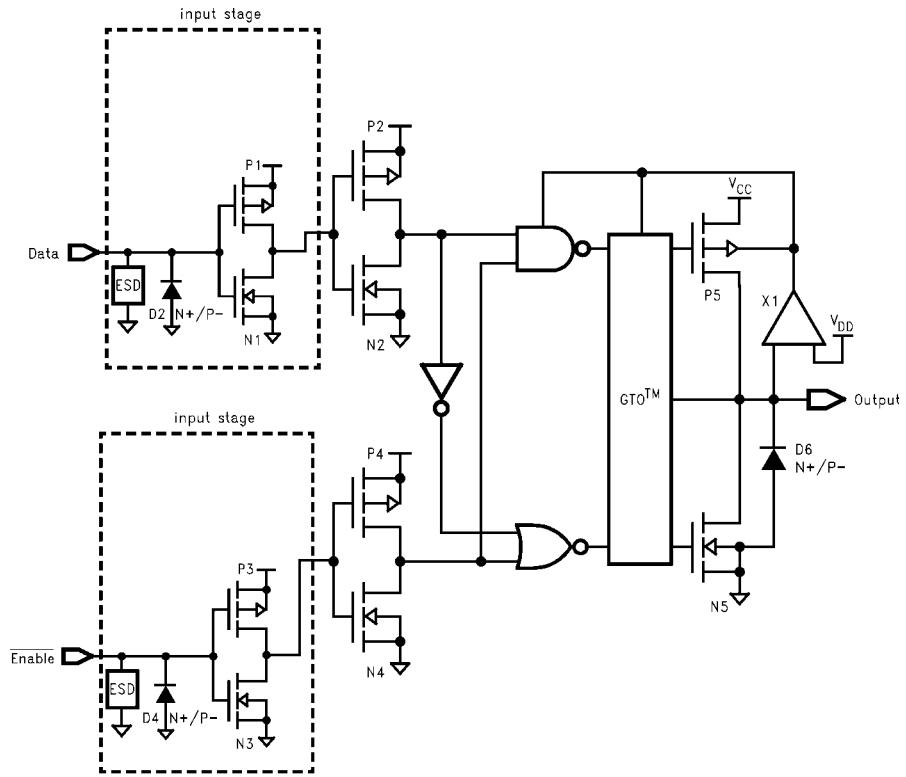


FIGURE 2. Waveforms
(Input Characteristics; $f = 1MHz$, $t_r = t_f = 3ns$)

Symbol	V_{CC}	
	$3.3V \pm 0.3V$	$2.7V$
V_{mi}	1.5V	1.5V
V_{mo}	1.5V	1.5V
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$

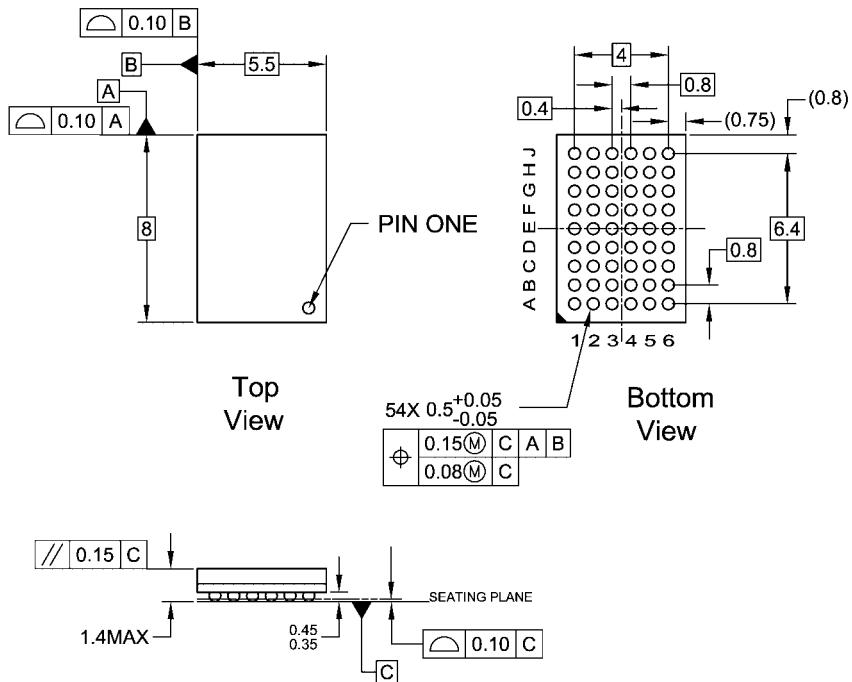
74LCXZ16245

Schematic Diagram Generic for LCX Family



Physical Dimensions

inches (millimeters) unless otherwise noted



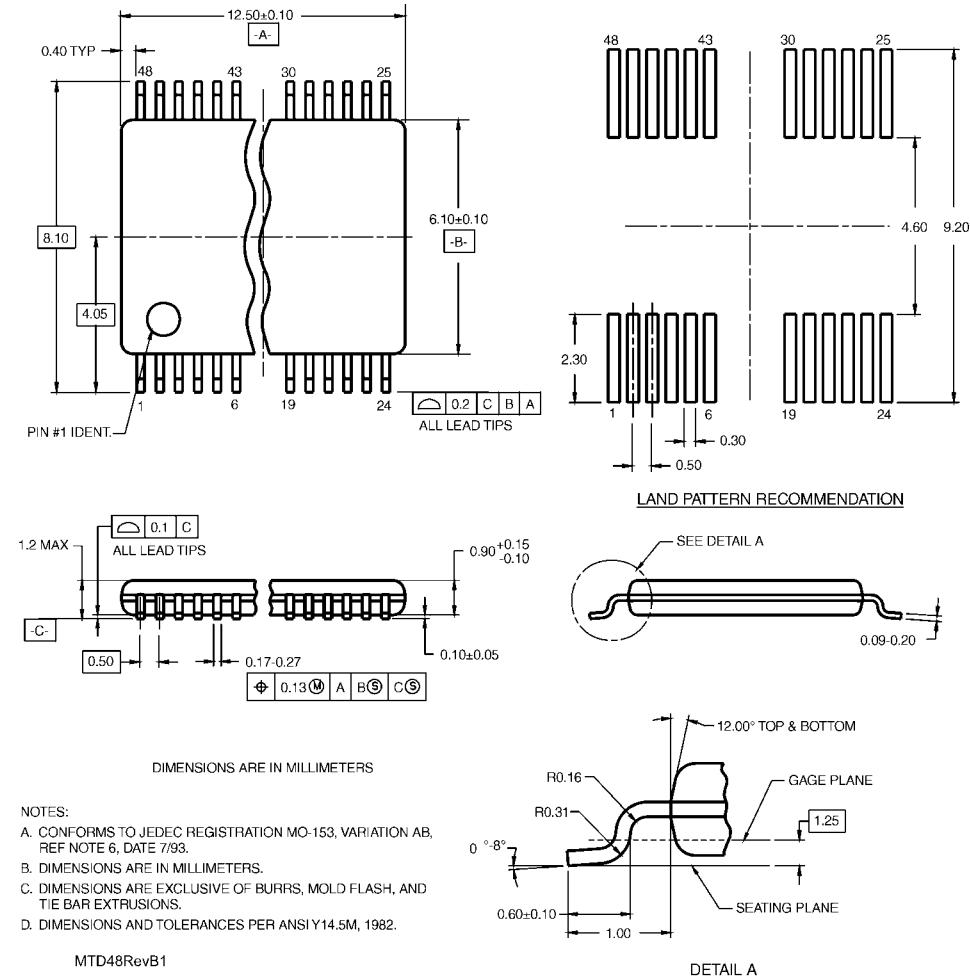
NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54RevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide
Package Number BGA54A
Preliminary

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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