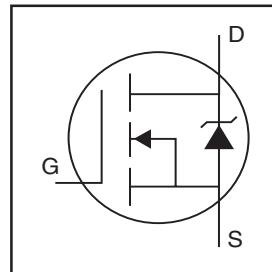


Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

HEXFET® Power MOSFET



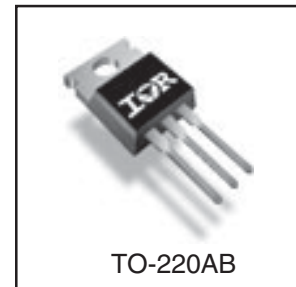
$$V_{DSS} = 20V$$

$$R_{DS(on)} = 4.0m\Omega$$

$$I_D = 180A^{\circ}$$

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



TO-220AB

Absolute Maximum Ratings

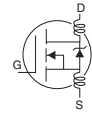
	Parameter	Max.	Units
I_D @ $T_C = 25^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V	180 [Ⓔ]	A
I_D @ $T_C = 100^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V	130 [Ⓔ]	
I_{DM}	Pulsed Drain Current ^①	700	
P_D @ $T_C = 25^{\circ}C$	Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ^②	350	mJ
I_{AR}	Avalanche Current ^①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ^②		mJ
dv/dt	Peak Diode Recovery dv/dt ^③	TBD	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.65	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ^⑧	—	62	

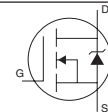
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

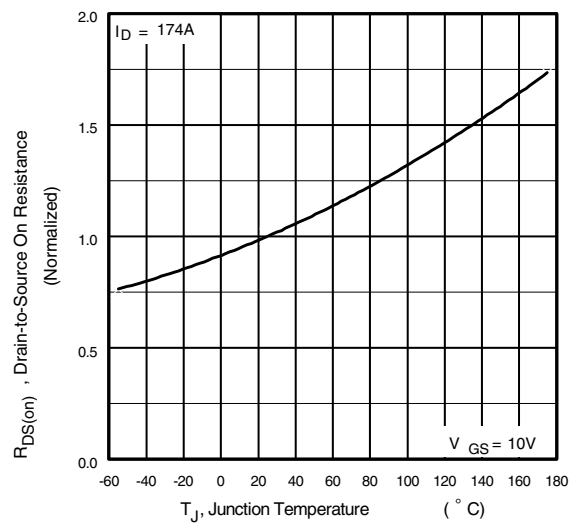
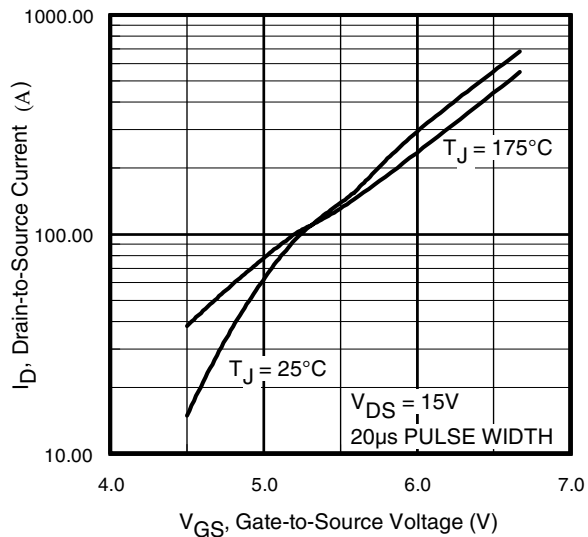
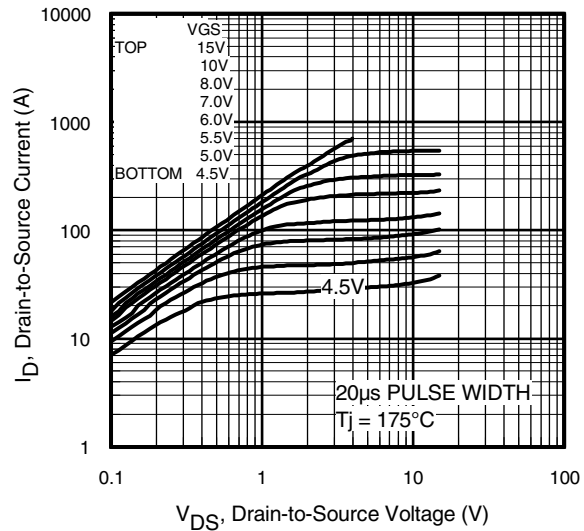
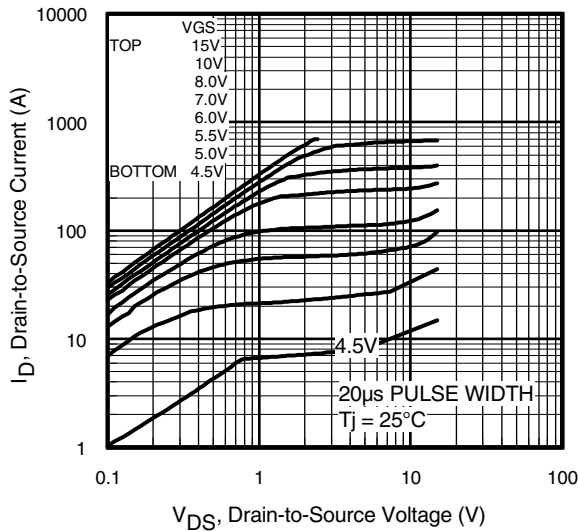
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.021	—	V/°C	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.3	4.0	mΩ	$V_{GS} = 10V, I_D = 104A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
g_{fs}	Forward Transconductance	59	—	—	S	$V_{DS} = 15V, I_D = 104A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 16V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	79	120	nC	$I_D = 104A$
Q_{gs}	Gate-to-Source Charge	—	18	27		$V_{DS} = 16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	31	46		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	$V_{DD} = 11V$
t_r	Rise Time	—	130	—		$I_D = 104A$
$t_{d(off)}$	Turn-Off Delay Time	—	47	—		$R_G = 4.5\Omega$
t_f	Fall Time	—	16	—		$V_{GS} = 10V$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3600	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	2370	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	520	—		$f = 1.0MHz$, See Fig. 5
C_{oss}	Output Capacitance	—	5710	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	2370	—		$V_{GS} = 0V, V_{DS} = 16V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	3540	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 16V$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	180⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	700		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 104A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	66	100	ns	$T_J = 25^\circ\text{C}, I_F = 104A$
Q_{rr}	Reverse Recovery Charge	—	130	200	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				





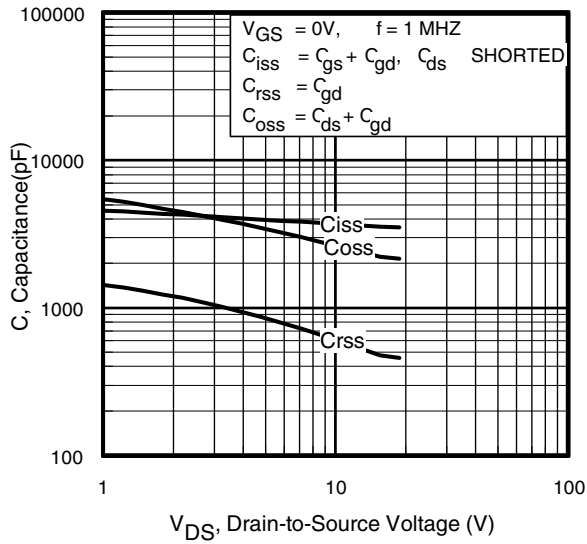


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

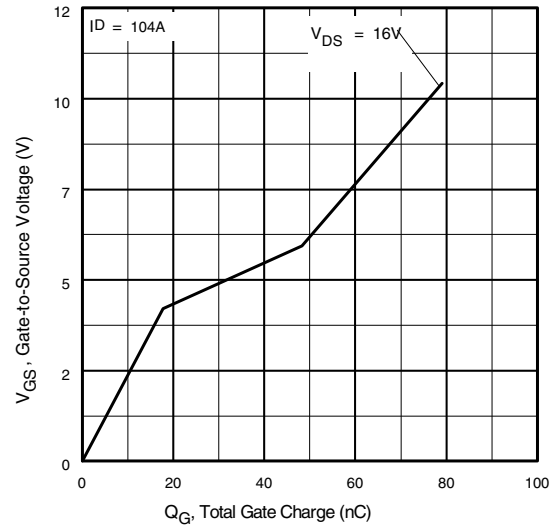


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

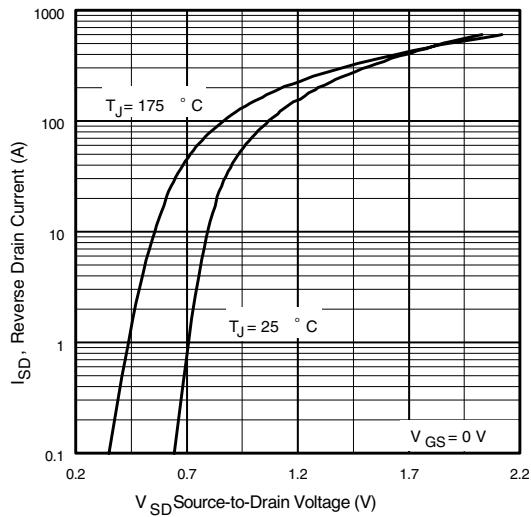


Fig 7. Typical Source-Drain Diode Forward Voltage

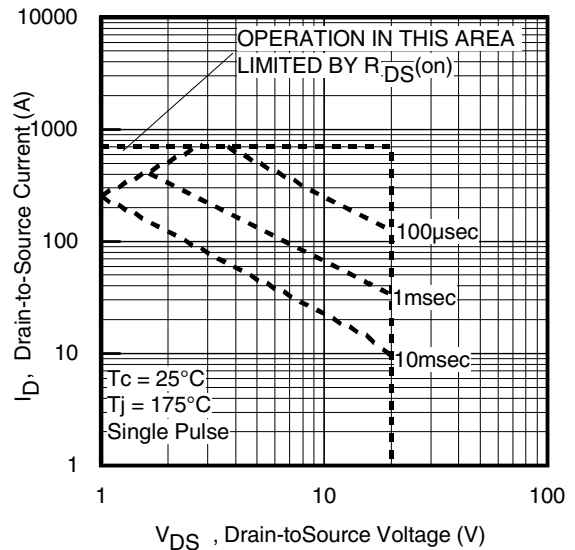


Fig 8. Maximum Safe Operating Area

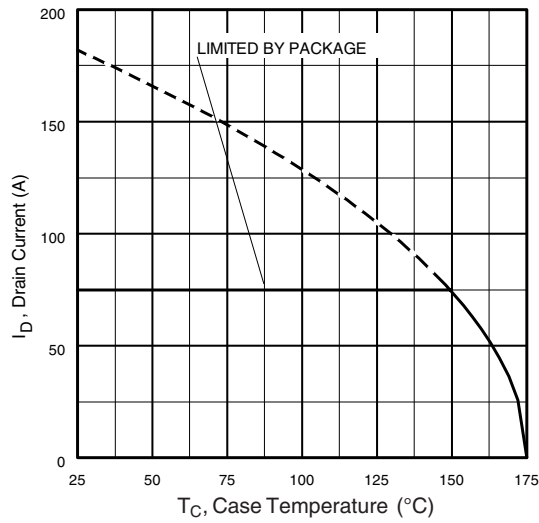


Fig 9. Maximum Drain Current Vs. Case Temperature

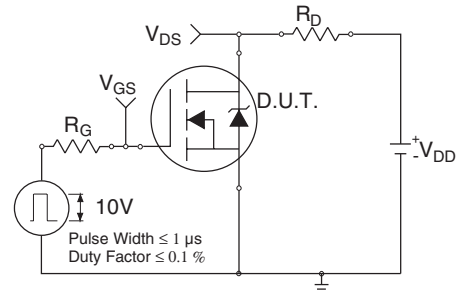


Fig 10a. Switching Time Test Circuit

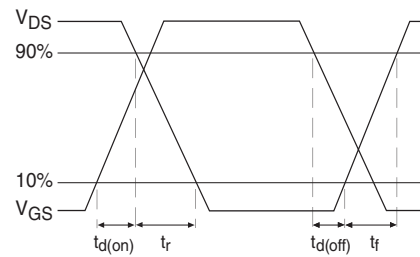


Fig 10b. Switching Time Waveforms

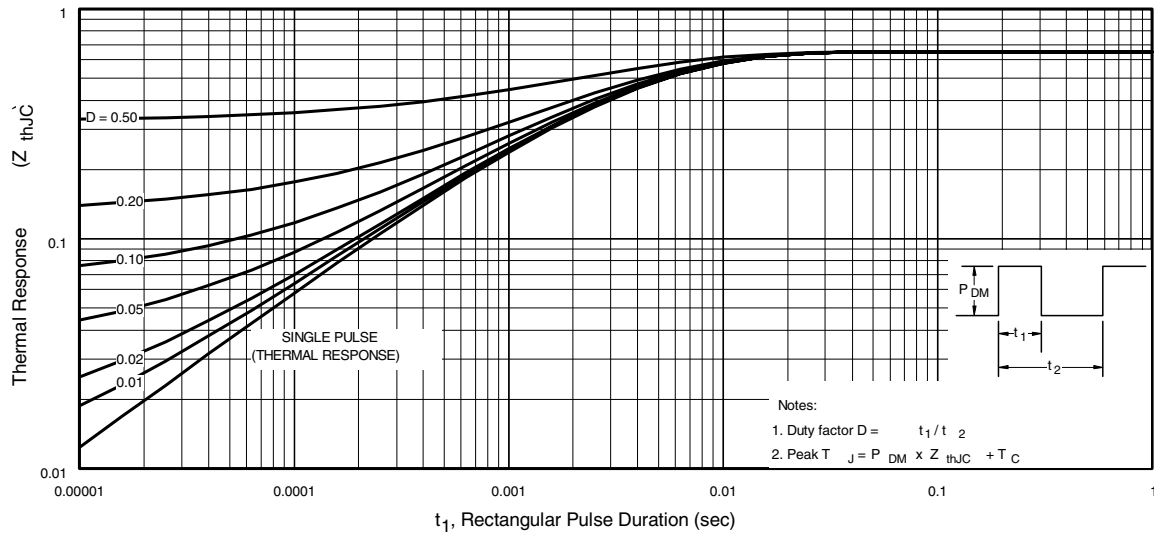


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRF1302

International
IR Rectifier

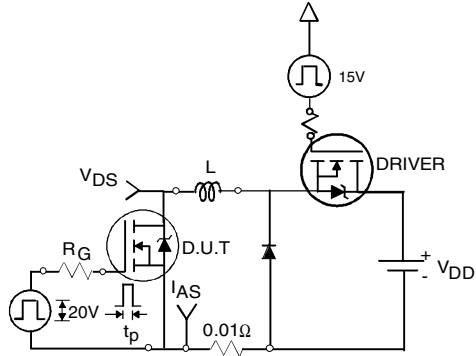


Fig 12a. Unclamped Inductive Test Circuit

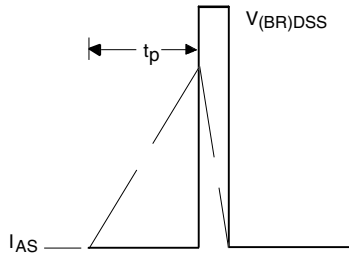


Fig 12b. Unclamped Inductive Waveforms

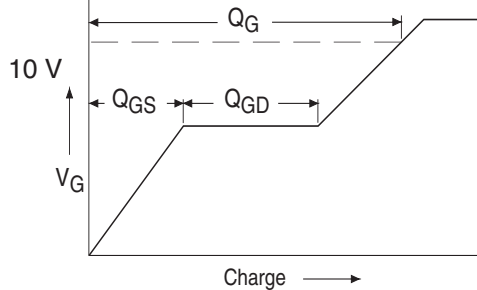


Fig 13a. Basic Gate Charge Waveform

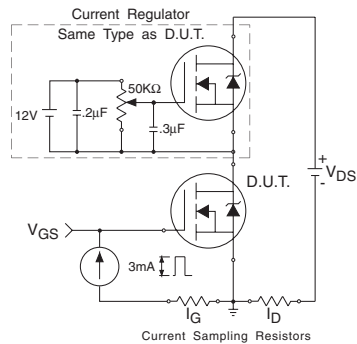


Fig 13b. Gate Charge Test Circuit

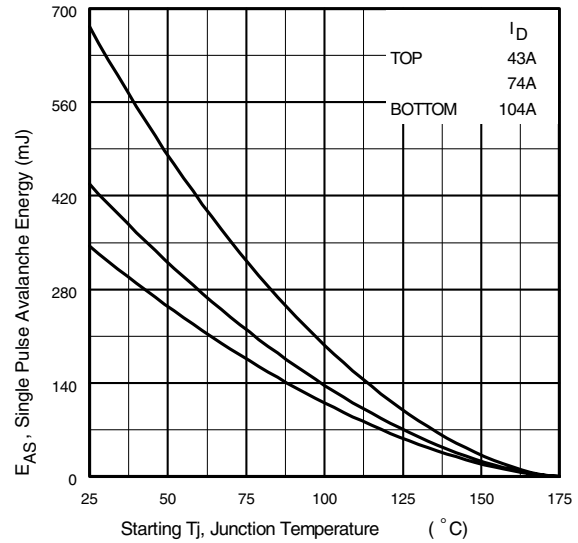


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

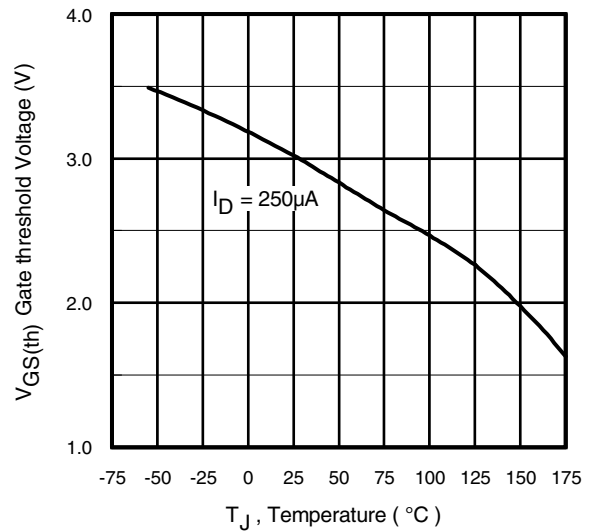


Fig 14. Threshold Voltage Vs. Temperature

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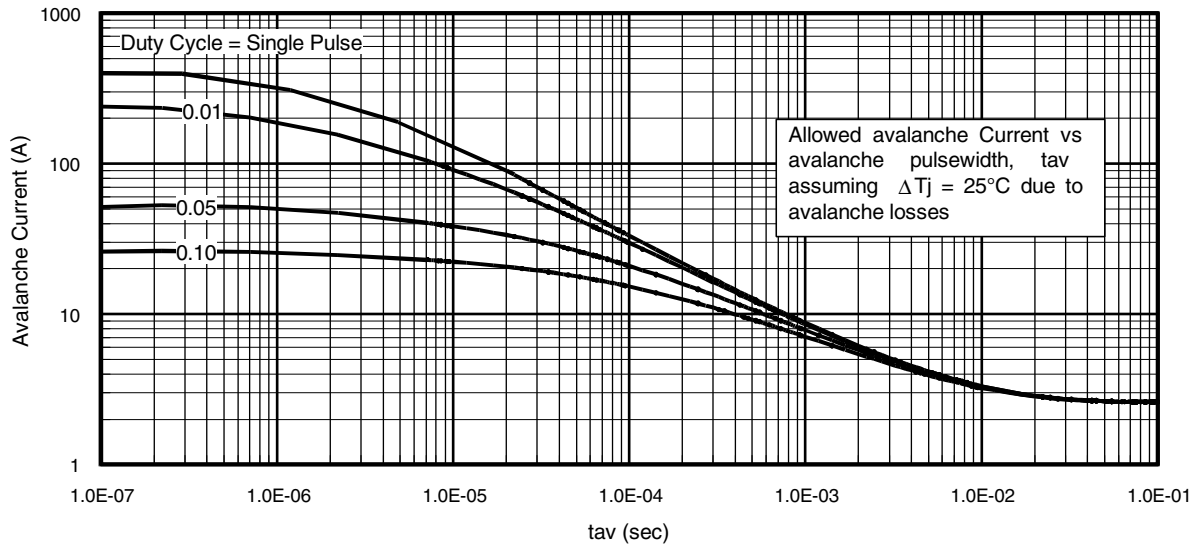


Fig 15. Typical Avalanche Current Vs. Pulsewidth

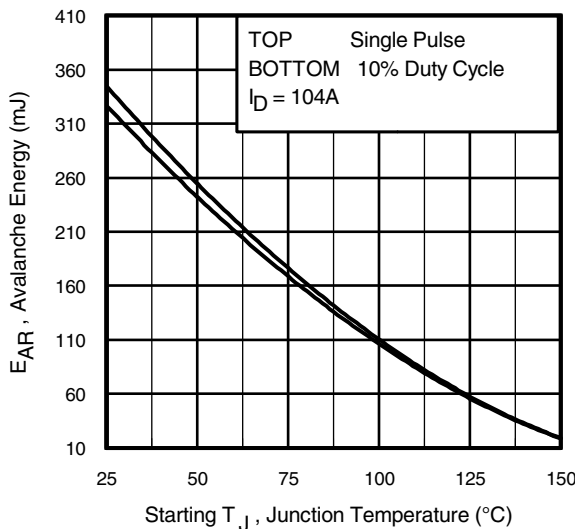


Fig 16. Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)**

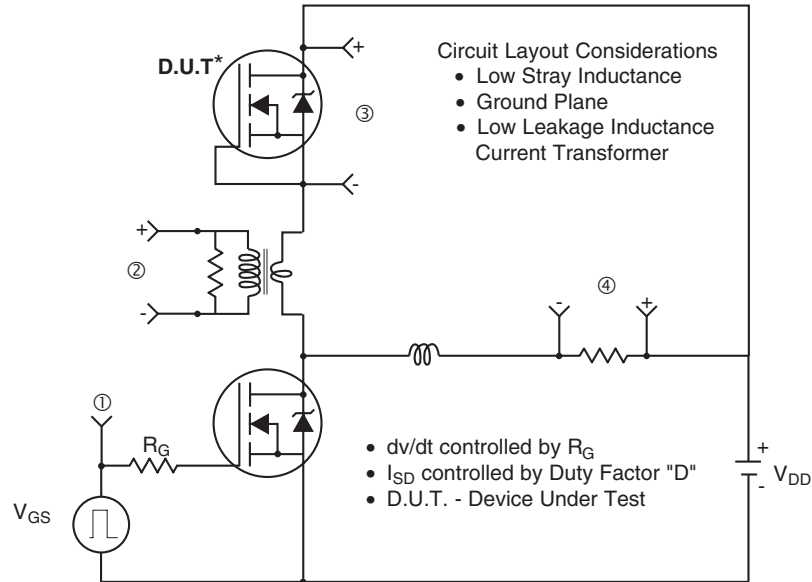
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

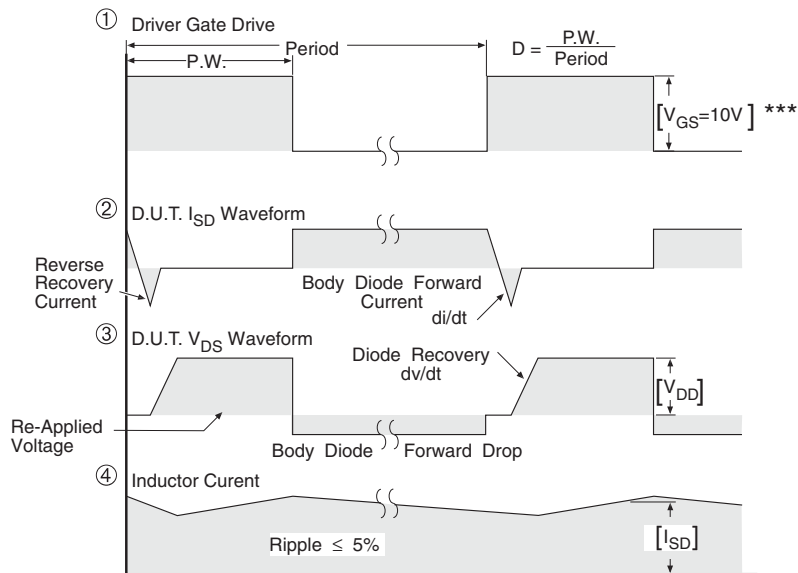
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

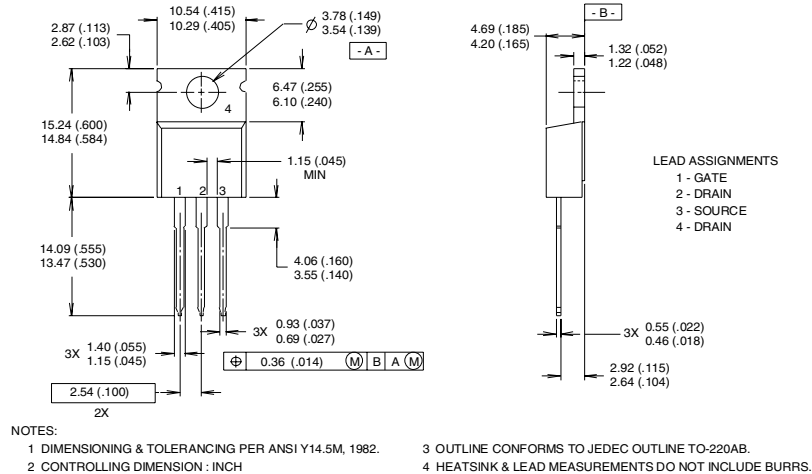


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

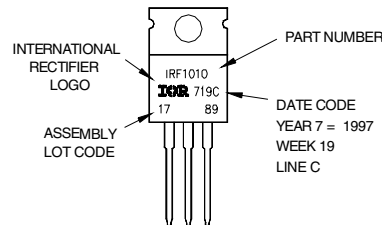
TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.063\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 104\text{A}$. (See Figure 12).
- ③ $I_{SD} \leq 104\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑧ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

TO-220 package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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Visit us at www.irf.com for sales contact information.10/02

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>