

# ***High-Performance 3-A Output Synchronous Buck EVM***

***Using the TPS56100 in Systems With Only 5 V  
Available***

## *User's Guide*

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## Preface

# Read This First

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### **About This Manual**

This user's guide is a reference manual for the *TPS56100EVM-133 5-V to Programmable Output Voltage, 3-A Synchronous Buck Converter Evaluation Module* (Literature Number SLVP133). This document provides information to assist managers and hardware engineers in application development.

### **How to Use This Manual**

This document contains the following chapters:

- ☐ Chapter 1 – Introduction
- ☐ Chapter 2 – Test Results
- ☐ Chapter 3 – Schematic
- ☐ Chapter 4 – Physical Layouts
- ☐ Chapter 5 – Bill of Materials

### **Related Documentation**

*Designing Fast Response Synchronous Buck Converters Using the TPS5210* Application Report, Literature Number SLVA044.

TPS5210 Programmable Synchronous-Buck Regulator Controller Data Sheet, Literature Number SLVS171.

*VRM 8.3 DC-DC Converter Design Guidelines*, Order Number: 243870–001, June 1998, Intel Corporation.

*High-Density Synchronous Buck Converter Design Using the TPS56xx Controllers* User's Guide, Literature Number SLVU013.

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# Introduction

This user's guide describes the TPS56100EVM-133 Synchronous Buck Converter Evaluation Module (SLVP133). The SLVP133 provides a convenient method for evaluating the performance of a synchronous buck converter using the TPS56100 ripple regulator controller. A complete designed and tested power supply is presented. The power supply is a programmable step-down dc/dc EVM that can deliver up to 3 A of continuous output current at a programmable output voltage from 1.3 V to 4.5 V, determined by a 5-bit DAC code and optional feedback divider network with an input voltage of 5 V.

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## 1.1 Background

New high-performance microprocessors may require from 40 to 80 W of power for the CPU alone. Load current must be supplied with up to 30 A/ $\mu$ s slew rate while keeping the output voltage within tight regulation and response time tolerances [3]. Parasitic interconnect impedances between the power supply and the processor must be kept to a minimum. Fast responding synchronous buck dc/dc converters controlled by the Texas Instruments TPS56100 hysteretic controller are ideally suited for microprocessor power applications requiring fast response and precise regulation of rapidly changing loads.

Conventional synchronous regulator control techniques include fixed frequency voltage-mode, fixed frequency current-mode, variable frequency current-mode, variable on-time, or variable off-time. CPU power supplies that are designed using these types of control methods require additional bulk storage capacitors on the output to maintain  $V_O$  within the regulation limits during the high di/dt load transients because of the limited bandwidth of the controller. Some controllers add a fast loop around the slower main control loop to improve the response time, but  $V_O$  must deviate outside a fixed tolerance band before the fast loop becomes active. The hysteretic control method employed by the TPS56100 offers superior performance with no requirements for additional output capacitance or difficult loop compensation design.

The TPS56100 controller was optimized for tight  $V_{out}$  regulation under static and dynamic load conditions, for improved system efficiency, and can operate in systems that derive main power from 5 V.



## 1.2 Performance Specification Summary

This section summarizes the performance specifications of the SLVP133 converter. Table 1–1 gives the performance specifications of the converters.

Table 1–1. Performance Specification Summary

| SPECIFICATION                              |                      | TEST CONDITIONS | MIN  | TYP    | MAX   | UNITS |
|--|----------------------|-----------------|------|--------|-------|-------|
| Input voltage range                        |                      |                 | 4.5  |        | 6     | V     |
| Output voltage range (no feedback divider) |                      | See Note 1      | 1.3  | 2.0    | 2.6   | V     |
| Static voltage tolerance                   |                      | See Note 2      | 1.98 | 2.0    | 2.02  | V     |
| Line regulation                            |                      | See Notes 1, 3  |      | ±0.05% | ±0.1% |       |
| Load regulation                            |                      | See Notes 4, 5  |      | ±0.1%  | ±0.4% |       |
| Transient response                         |                      | See Note 6      |      | ±55    |       | mV pk |
|  |                      |                 |      | 50     |       | μs    |
| Output current range                       |                      | See Note 3      | 0    |        | 3     | A     |
| Current limit                              |                      | See Note 3      | 3.5  |        |       | A     |
| Output ripple                              |                      | See Note 3      |      | 20     |       | mV    |
| Soft-Start risetime                        |                      | See Note 4      |      | 10     |       | ms    |
| Operating frequency                        | $V_O = 3.3\text{ V}$ | See Notes 1, 4  |      | 197    |       | kHz   |
|  | $V_O = 1.8\text{ V}$ | See Notes 1, 4  |      | 520    |       | kHz   |
| Efficiency 3 A load                        | $V_O = 3.3\text{ V}$ | See Note 4      |      | 88%    |       |       |
|  | $V_O = 1.8\text{ V}$ | See Note 4      |      | 80%    |       |       |

- Notes:**
- 1)  $I_O = 3\text{ A}$
  - 2) VID inputs set for  $V_{REF} = 2\text{ V}$ .
  - 3) Input voltage can be at any point over entire range.
  - 4) Input voltage adjusted to 5 VDC.
  - 5)  $I_O$  varied can be at any point over entire range.
  - 6)  $I_O$  pulsed from 0 A to 3 A,  $di/dt = 30\text{ A}/\mu\text{s}$ .

## 1.3 Voltage Programming Code

A voltage programming network (VP) consisting of a 5-bit DAC programs the reference voltage within a range from 1.3 V to 2.6 V. The reference voltage for a given VP Code is shown in Table 1–2. When no feedback divider network is used, the output voltage will equal the reference voltage. Using the feedback divider network (R5 and R10), allows the user to set the output voltage higher than the reference voltage.

Table 1–2. Voltage Programming Code

| VP Terminals<br>(0 = GND, 1 = floating or pull-up to 5 V) |     |     |     |     | VREF<br>(Vdc) |
|---|-----|-----|-----|-----|---------------|
| VP4   | VP3 | VP2 | VP1 | VP0 |               |
| 0   | 1   | 1   | 1   | 1   | 1.30          |
| 0   | 1   | 1   | 1   | 0   | 1.35          |
| 0   | 1   | 1   | 0   | 1   | 1.40          |
| 0   | 1   | 1   | 0   | 0   | 1.45          |
| 0   | 1   | 0   | 1   | 1   | 1.50          |
| 0   | 1   | 0   | 1   | 0   | 1.55          |
| 0   | 1   | 0   | 0   | 1   | 1.60          |
| 0   | 1   | 0   | 0   | 0   | 1.65          |
| 0   | 0   | 1   | 1   | 1   | 1.70          |
| 0   | 0   | 1   | 1   | 0   | 1.75          |
| 0   | 0   | 1   | 0   | 1   | 1.80          |
| 0   | 0   | 1   | 0   | 0   | 1.85          |
| 0   | 0   | 0   | 1   | 1   | 1.90          |
| 0   | 0   | 0   | 1   | 0   | 1.95          |
| 0   | 0   | 0   | 0   | 1   | 2.00          |
| 0   | 0   | 0   | 0   | 0   | 2.05          |
| 1   | 1   | 1   | 1   | 1   | No CPU        |
| 1   | 1   | 1   | 1   | 0   | 2.10          |
| 1   | 1   | 1   | 0   | 1   | 2.20          |
| 1   | 1   | 1   | 0   | 0   | 2.30          |
| 1   | 1   | 0   | 1   | 1   | 2.40          |
| 1   | 1   | 0   | 1   | 0   | 2.50          |
| 1   | 1   | 0   | 0   | 1   | 2.60          |
| 1   | 1   | 0   | 0   | 0   | 2.60          |
| 1   | 0   | 1   | 1   | 1   | 2.60          |
| 1   | 0   | 1   | 1   | 0   | 2.60          |
| 1   | 0   | 1   | 0   | 1   | 2.60          |
| 1   | 0   | 1   | 0   | 0   | 2.60          |
| 1   | 0   | 0   | 1   | 1   | 2.60          |
| 1   | 0   | 0   | 1   | 0   | 2.60          |
| 1   | 0   | 0   | 1   | 1   | 2.60          |
| 1   | 0   | 0   | 0   | 1   | 2.60          |
| 1   | 0   | 0   | 0   | 0   | 2.60          |

**Note:** If the VP bits are set to 11111, then the high-side and low-side driver outputs will be set low.

# Test Results

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This chapter shows the test setups used and the test results obtained in designing the SLVP133 EVM.

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## 2.1 Test Summary

The detailed test results are presented in Figures 2–2 to 2–5 for the SLVP133. The following are summarized results.

### 2.1.1 Static Line and Load Regulation

The precise reference voltage regulator implemented in the TPS56100 controller using a positive remote sense pin provides excellent regulation characteristics. The load regulation from no load to 3 A load current does not exceed 0.2%. The line regulation is less than 0.03% for the input voltage range from 4.5 V to 6 V. Line and load regulation curves are shown in Figure 2–1. The set point tolerance is approximately 1.0%.

### 2.1.2 Output Voltage Ripple

The output voltage peak-to-peak ripple is approximately 20 mV. This is a typical value but it can be optimized for lower ripple applications. The output filter for this EVM design is optimized for fast transient response due to the high slew-rate load current transitions. Therefore, the output filter is not optimized for low ripple and has a moderate amount of output ripple.

### 2.1.3 Efficiency and Power Losses

Efficiency and power losses for 5-V input voltage and maximum output current of 3 A are presented in the following table:

Table 2–1. Evaluation Board Efficiency and Power Losses

| Evaluation Board      | Efficiency, % | Power Losses, W |
|-----------------------|---------------|-----------------|
| SLVP133 $V_o = 1.8$ V | 80            | 1.3             |
| SLVP133 $V_o = 3.3$ V | 88            | 1.4             |

Low power loss in each component decreases their temperature rise and improves long term reliability. The EVM does not require forced air cooling over a temperature range of 0°C to 50°C.

### 2.1.4 Output Start-Up and Overshoot

Output voltage rise time does not depend on the load current and ramps up in a linear fashion. There is no discernable overshoot in the waveform. In this application, output voltage rise time is set to approximately 10 mS with an external capacitor.

### 2.1.5 Frequency Variation

The switching frequency for a hysteretic controller depends on the input and output voltages and the output filter characteristics. It has approximately the same frequency variation as constant OFF time controllers. The precise equation for switching frequency, confirmed by experiment, is presented in the

TPS56100 datasheet. A more detailed analysis of the switching frequency variation for a hysteretic converter can be found in TI's application report *Designing Fast Response Synchronous Buck Converters Using the TPS5210*, Literature Number SLVA044 and in the paper presented at HFPC-98: *A Fast, Efficient Synchronous-Buck Controller for Microprocessor Power Supplies*. This paper can also be downloaded from the URL:  
<http://www.ti.com/sc/docs/msp/papers/index.htm>

### 2.1.6 Conclusion

The test results of the SLVP133 EVM demonstrate the advantages of the TPS56100 controller to meet stringent supply requirements to power supplies, especially for powering DSPs and microprocessors. The power system designer has a good solution to optimize the system for his particular application. Detailed information on how to design a dc-dc converter by using the TPS56100 hysteretic controller is presented in the TPS56100 datasheet. Other sources of information on designing hysteretic controlled power supplies can be found in TI's User's Guide *High-Density Synchronous Buck Converter Design Using TPS56xx Controllers in SLVP10x EVMs*, Literature Number SLVU007 or the application report *Designing Fast Response Synchronous Buck Regulators Using the TPS5210*, Literature Number SLVA044.

## 2.2 Test Setup

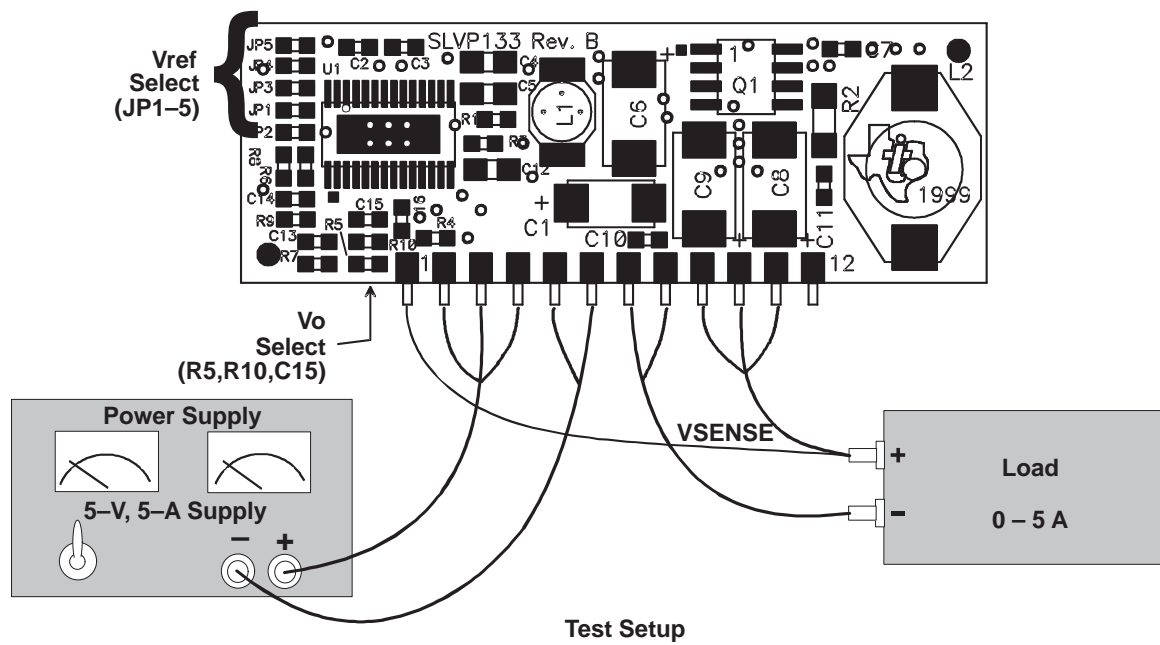
This test procedure assumes that the output voltage is set to 1.8 V (JP2, JP4, JP5 installed). If this is not the case, the user should make appropriate adjustments in the load and measurements.

Follow these steps for initial power up of the SLVP133:

- 1) Connect an electronic load from Vout to PwrGND (J9, J10, J11 and J7, J8) adjusted to draw approximately 1 A at 1.8 V. The exact current is not critical; any nominal current is sufficient. A fixed resistor can also be used in place of the electronic load. The output current drawn by the resistor is  $I_L = 1.8 \text{ V}/R$ , where R is the value of the load resistor. The resistor power rating,  $P_R$  should be at least  $2 \times 1.8^2/R$  watts.  
 Connect the sense line from the load to Vsense+(J1).
- 2) Connect a 5-V lab power supply to the 5-V input and PWRGND (J2, J3, J4 and J5, J6) of the SLVP133. Adjust the current limit to approximately 1 A.
- 3) Turn on the 5-V power supply and ramp the input voltage up to 5 V.
- 4) Verify that the SLVP133 output voltage (measured at the module output pins) is  $1.8 \text{ V} \pm 0.020 \text{ V}$ .
- 5) For subsequent testing, ensure the lab supply output current capacity and current limit are at least 3 A so that the SLVP133 can be operated at maximum load of 3 A.
- 6) Refer to the Test Results for selected typical waveforms and operating conditions for verification of proper module operation.

Figure 2–1 shows the SLVP133 test setup.

Figure 2–1. SLVP133 Test Setup



NOTE: All wire pairs should be twisted.

## 2.3 Test Results

Figures 2–2 to 2–5 show test results for the SLVP133.

Figure 2–2. SLVP133 Measured Load Regulation 3.3-V Output

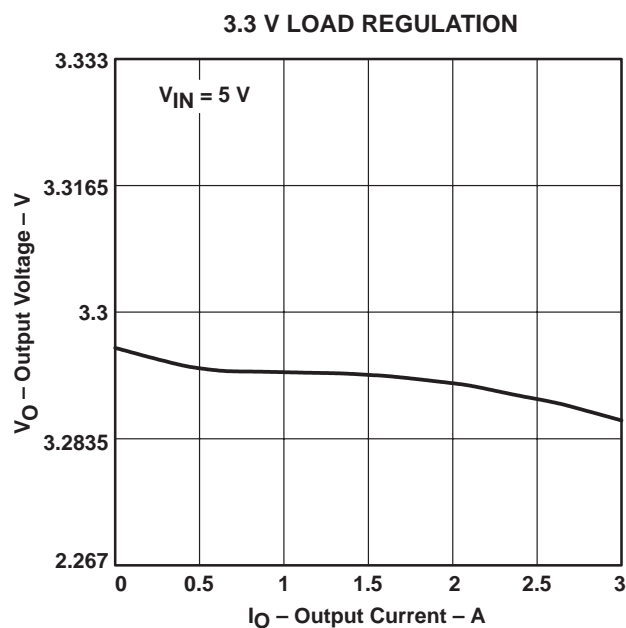


Figure 2–3. SLVP133 Measured Line Regulation 1.8-V Output

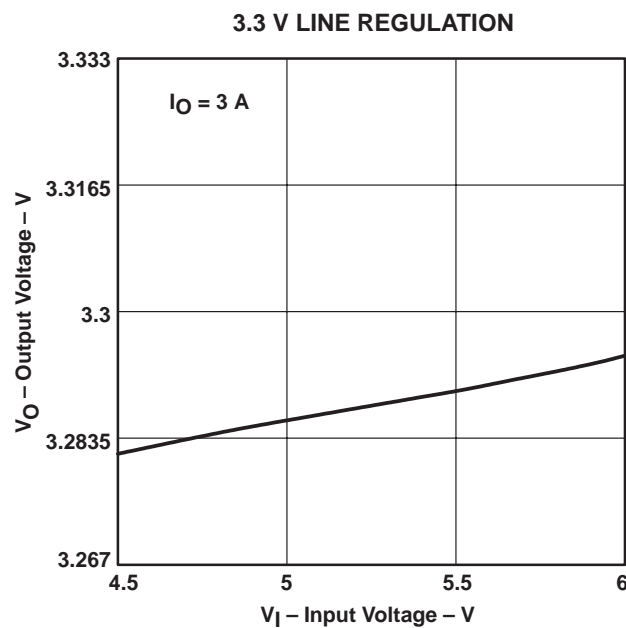


Figure 2–4. SLVP133 Measured Load Regulation 1.8-V Output

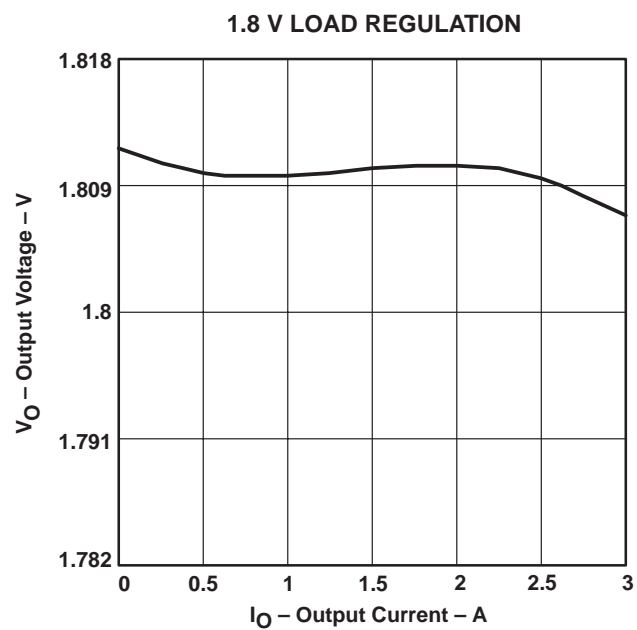
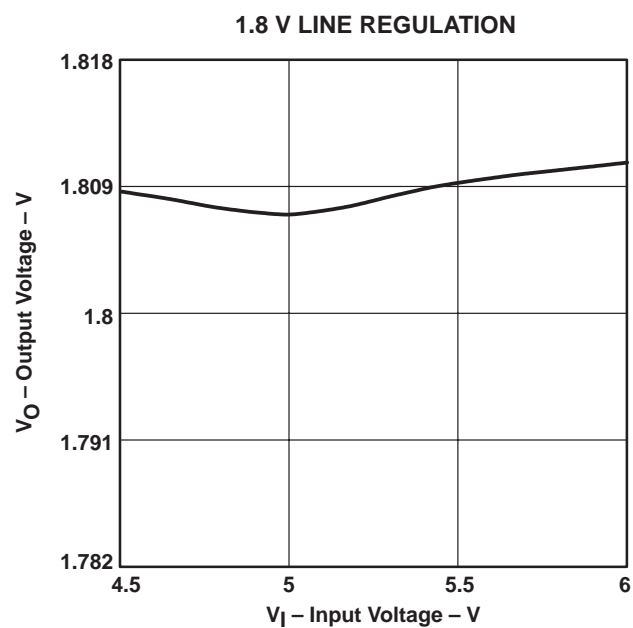


Figure 2–5. SLVP133 Line Regulation 1.8-V Output





# Schematic



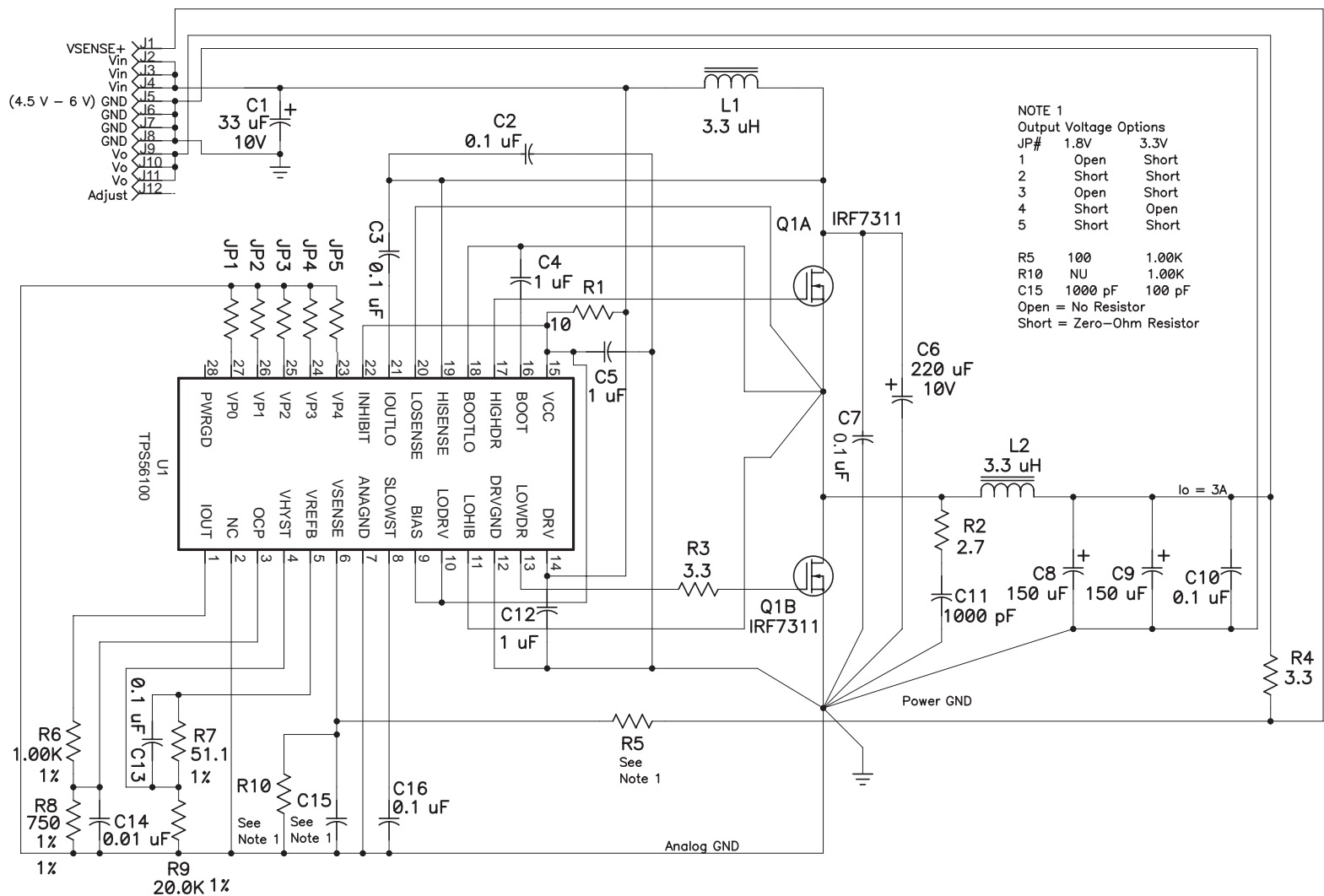
This chapter contains the schematic diagram for the SLVP133 EVM.

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### **3.1 Schematic**

Figure 3–1 shows the SLVP133 EVM schematic diagram.

Figure 3–1. SLVP133 Schematic Diagram



Notes: 1) R4 can be replaced with a short when circuit is integrated onto motherboard.

2) R10 can be deleted for voltage options below 2.6 V.

3) Jumpers JP1–5 can be replaced with shorts to ground or opens as specified in data sheet (or Note 1 on schematic) when voltage-programming option is not needed.



# Physical Layouts

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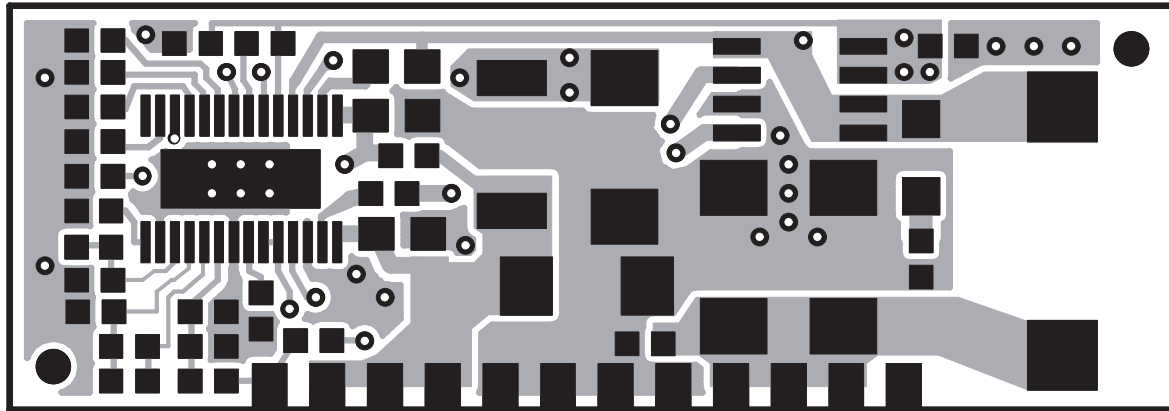
This chapter contains the board layout, and assembly drawings for the SLVP133 EVM.

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## 4.1 Board Layout

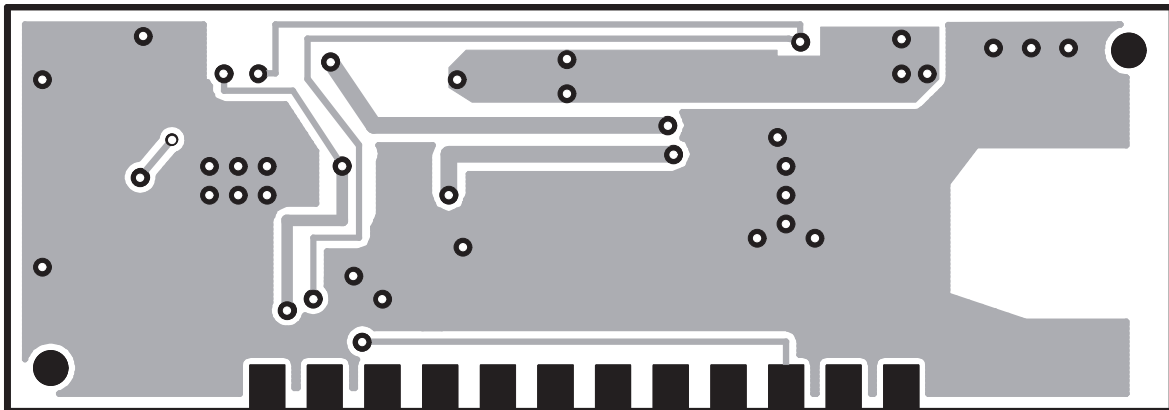
The power supply module consists of one PWB. Figure 4–1 shows the top layer of the SLVP133 PWB. Figure 4–2 shows the bottom layer (top view) of the SLVP133 PWB.

*Figure 4–1. SLVP133 Board Layout Top Layer*



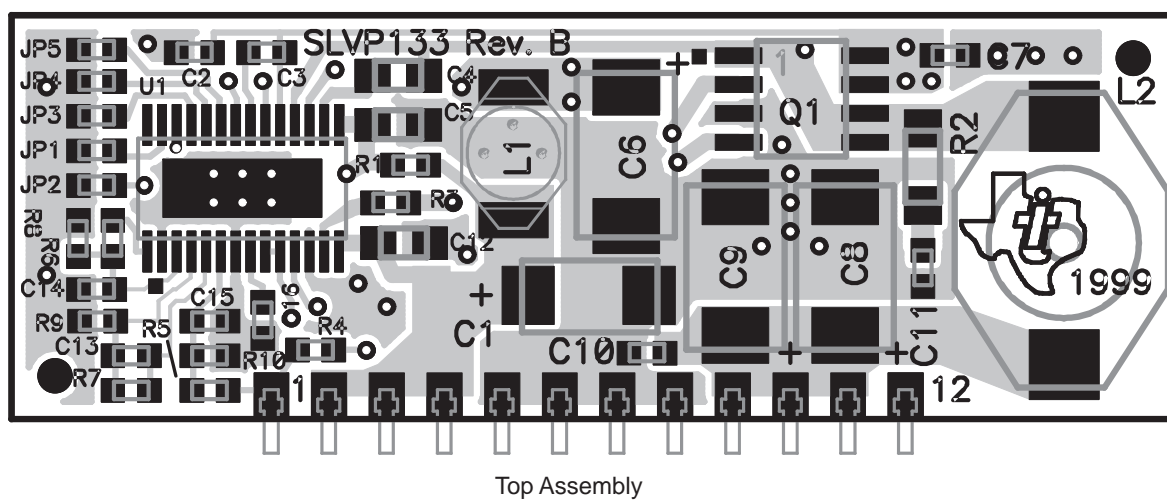
Top Layer

*Figure 4–2. SLVP133 Board Layout Bottom Layer*



Bottom Layer (Top View)

Figure 4–3. SLVP133 Top Assembly View







# Bill of Materials



This chapter contains the bill of materials required for the SLVP133 EVM.

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## 5.1 Bill of Materials

EVM. Table 5–1 lists materials required for the SLVP133 EVM.

Table 5–1. SLVP133 Bill of Materials

| Ref Des | Qty | Part Number      | Description   | MFG           | Size     |
|---------|-----|------------------|---|---------------|----------|
| C1      | 1   | 10TPA33M         | Capacitor, POSCAP, 33 $\mu$ F, 10 V, 20%            | Sanyo         | C        |
| C2      | 6   | GRM39X7R104K016A | Capacitor, ceramic, 0.1 $\mu$ F, 16 V, 10%, X7R     | MuRata        | 603      |
| C3      |     | GRM39X7R104K016A | Capacitor, ceramic, 0.1 $\mu$ F, 16 V, 10%, X7R     | MuRata        | 603      |
| C4      | 4   | ECJ-2VF1C105Z    | Capacitor, ceramic, 1 $\mu$ F, 16 V, 80%–20%, Y5V   | Panasonic     | 805      |
| C5      |     | ECJ-2VF1C105Z    | Capacitor, ceramic, 1 $\mu$ F, 16 V, 80%–20%, Y5V   | MuRata        | 805      |
| C6      | 1   | 10TPB220M        | Capacitor, POSCAP, 220 $\mu$ F, 10 V, 20%           | Sanyo         | D        |
| C7      |     | GRM39X7R104K016A | Capacitor, ceramic, 0.1 $\mu$ F, 16 V, 10%, X7R     | MuRata        | 603      |
| C8      | 2   | 6TPB150M         | Capacitor, POSCAP, 150 $\mu$ F, 6.3 V, 20%          | Sanyo         | D        |
| C9      |     | 6TPB150M         | Capacitor, POSCAP, 150 $\mu$ F, 6.3 V, 20%          | Sanyo         | D        |
| C10     |     | GRM39X7R104K016A | Capacitor, ceramic, 0.1 $\mu$ F, 16 V, 10%, X7R     | MuRata        | 603      |
| C11     | 1   | GRM39X7R102K050A | Capacitor, ceramic, 1000 pF, 50 V, 10%, X7R         | MuRata        | 603      |
| C12     |     | ECJ-2VF1C105Z    | Capacitor, ceramic, 1 $\mu$ F, 16 V, +80%–20%, Y5V  | Panasonic     | 805      |
| C13     |     | GRM39X7R104K016A | Capacitor, ceramic, 0.1 $\mu$ F, 16 V, 10%, X7R     | MuRata        | 603      |
| C14     | 1   | GRM39X7R103K025A | Capacitor, ceramic, 0.01 $\mu$ F, 25 V, 10%, X7R    | MuRata        | 603      |
| C15     |     |                  | See below   |               | 603      |
| C16     |     | GRM39X7R104K016A | Capacitor, ceramic, 0.1 $\mu$ F, 16 V, 10%, X7R     | MuRata        | 603      |
| J1–J12  | 12  | CA26DA-D36W-0FC  | Clip, surface-mount, 0.040" board, 0.090" stand-off | NAS Interplex | 0.1 Ctrs |
| JP1     |     |                  | See voltage options at end of bill of materials     |               | 603      |
| JP2     | 2   | Std              | Resistor, chip, 0 $\Omega$ , 1/16W, 5%              | Sanyo         | 603      |
| JP3     |     |                  | See voltage options at end of bill of materials     |               | 603      |
| JP4     |     |                  | See voltage options at end of bill of materials     |               | 603      |
| JP5     |     | Std              | Resistor, Chip, 0 $\Omega$ , 1/16W, 5%              |               | 603      |
| L1      | 1   | DO1608P-332      | Inductor, 3.3 $\mu$ H, 2 A                          | Coilcraft     | DO1608P  |
| L2      | 1   | DO3316P-332      | Inductor, 3.3 $\mu$ H, 6.1 A                        | Coilcraft     | DO3316P  |
| Q1      | 1   | IRF7311          | FET, Dual N-ch, 20 V, 6.6 A, 29 m $\Omega$          | IR            | SO–8     |
| Q1 Alt  |     | Si4966DY         | FET, Dual N-ch, 20 V, 7.1 A, 25 m $\Omega$          | Siliconix     | SO–8     |
| R1      | 1   | Std              | Resistor, Chip, 10 $\Omega$ , 1/16W, 5%             |               | 603      |
| R2      | 1   | Std              | Resistor, Chip, 2.7 $\Omega$ , 1/10W, 5%            |               | 1206     |
| R3      | 2   | Std              | Resistor, Chip, 3.3 $\Omega$ , 1/16W, 5%            |               | 603      |
| R4      |     | Std              | Resistor, Chip, 3.3 $\Omega$ , 1/16W, 5%            |               | 603      |
| R5      |     |                  | See voltage options at end of bill of materials     |               | 603      |
| R6      | 1   | Std              | Resistor, Chip, 1.00 k $\Omega$ , 1/16W, 1%         |               | 603      |
| R7      | 1   | Std              | Resistor, Chip, 51.1 $\Omega$ , 1/16W, 1%           |               | 603      |

Table 5–1. SLVP128 Bill of Materials (Continued)

| Ref Des             | Qty | Part Number      | Description   | MFG    | Size   |
|---------------------|-----|------------------|---|--------|--------|
| R8                  | 1   | Std              | Resistor, chip, 750 $\Omega$ , 1/16W, 1%            |        | 603    |
| R9                  | 1   | Std              | Resistor, chip, 20.0 k $\Omega$ , 1/16W, 1%         |        | 603    |
| R10                 |     |                  | See voltage options below                           |        | 603    |
| U1                  | 1   | TPS56100PWP      | IC, PWM ripple controller, programmable             | TI     | PWP–28 |
|                     | 1   | SLVP133, Rev. A  | PCB, 2-layer, 2-oz, 2.02"(L) x 0.70"(W) x 0.040"(T) |        |        |
| <b>1.8–V option</b> |     |                  |   |        |        |
| JP1                 |     |                  | Not used  |        | 603    |
| JP3                 |     |                  | Not used  |        | 603    |
| JP4                 | 1   | Std              | Resistor, chip, 0 $\Omega$ , 1/16W, 5%              |        | 603    |
| R5                  | 1   | Std              | Resistor, chip, 100 $\Omega$ , 1/16W, 5%            |        | 603    |
| R10                 |     |                  | Not used  |        | 603    |
| C15                 | 1   | GRM39X7R102K050A | Capacitor, ceramic, 1000 pF, 50 V, 10%, X7R         | MuRata | 603    |
| <b>3.3–V option</b> |     |                  |   |        |        |
| JP1                 | 2   | Std              | Resistor, chip, 0 $\Omega$ , 1/16W, 5%              |        | 603    |
| JP3                 |     | Std              | Resistor, chip, 0 $\Omega$ , 1/16W, 5%              |        | 603    |
| JP4                 |     |                  | Not used  |        | 603    |
| R5                  | 2   | Std              | Resistor, chip, 1 K $\Omega$ , 1/16W, 1%            |        | 603    |
| R10                 |     | Std              | Resistor, chip, 1 K $\Omega$ , 1/16W, 1%            |        | 603    |
| C15                 | 1   | GRM39COG101J050A | Capacitor, ceramic, 100 pF, 50 V, 5%, COG           | MuRata | 603    |

