

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.)

Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003



DESCRIPTION

The M65857FP is a Surround Processor IC for AV Amplifier ,Mini-component stereo and Car audio built-in QSurround™5.1.

The QSurround™5.1 system generates 5.1ch from 2ch input and produce 3D sound.

(Note) QSurround™5.1 is a trademark of QSound Labs, Inc., and is used under license from QSound Labs, Inc.

FEATURES

- Built-in QSurround™5.1 system
- 6 Output (5.1ch) available
- Built-in SRAM for digital delay
- Digital delay
 - Delay time; 20,30,40,50msec
 - Frequency response; 3KHz/7KHz
- Built-in 3wire MCU interface
- Bypass mode



36P2R-A

0.8mm pitch 450mil SSOP
(8.4mm×15.0mm×2.0mm)

APPLICATIONS

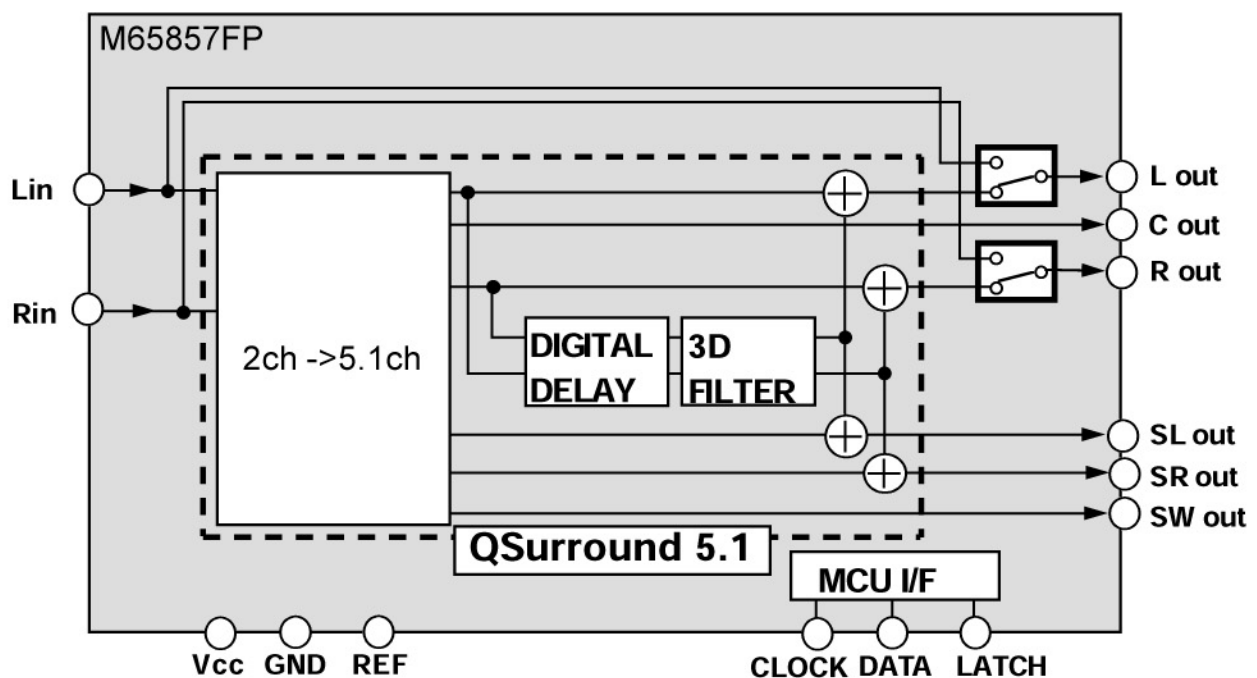
AV Amplifier,Mini-component stereo,Car Audio

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ----- Vcc=4.5 to 5.5V

Rated supply voltage ----- Vcc=5.0V

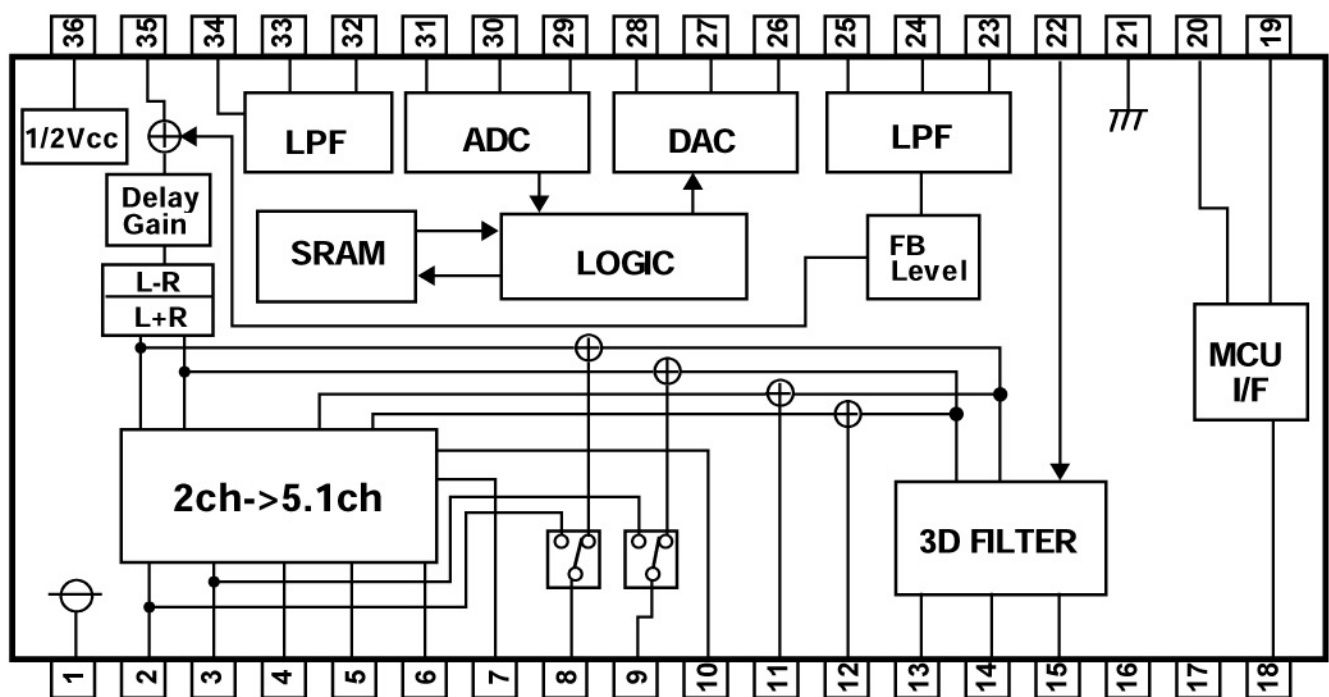
SYSTEM CONFIGURATION



PIN CONFIGURATION (TOP VIEW)

Vcc	1	36	REF
LIN	2	35	DELAYIN
RIN	3	34	LPF1
SWLPF	4	33	LPF2
CBPF2	5	32	LPF3
CBPF1	6	31	ADC1
SWOUT	7	30	ADC2
LOUT	8	29	ADC3
ROUT	9	28	DAC3
COUT	10	27	DAC2
SLOUT	11	26	DAC1
SROUT	12	25	LPFO1
3DR	13	24	LPFO2
3DFIL	14	23	LPFO3
3DL	15	22	3DIN
TEST1	16	21	GND
TEST2	17	20	LATCH
DATA	18	19	CLOCK

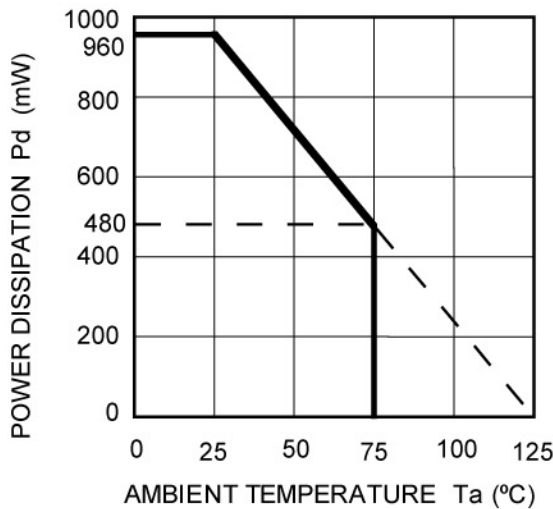
Outline 36P2R

BLOCK DIAGRAM


ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply Voltage		6	V
VI	Input Voltage		-0.3 to Vcc+0.3	V
Pd	Power Dissipation		960	mW
Kθ	Thermal Derating	Ta≥25°C	9.6	mW/°C
Topr	Operating Temperature		-20 to +75	°C
Tstg	Storage Temperature		-40 to +125	°C

THERMAL DERATING (MAXIMUM RATING)



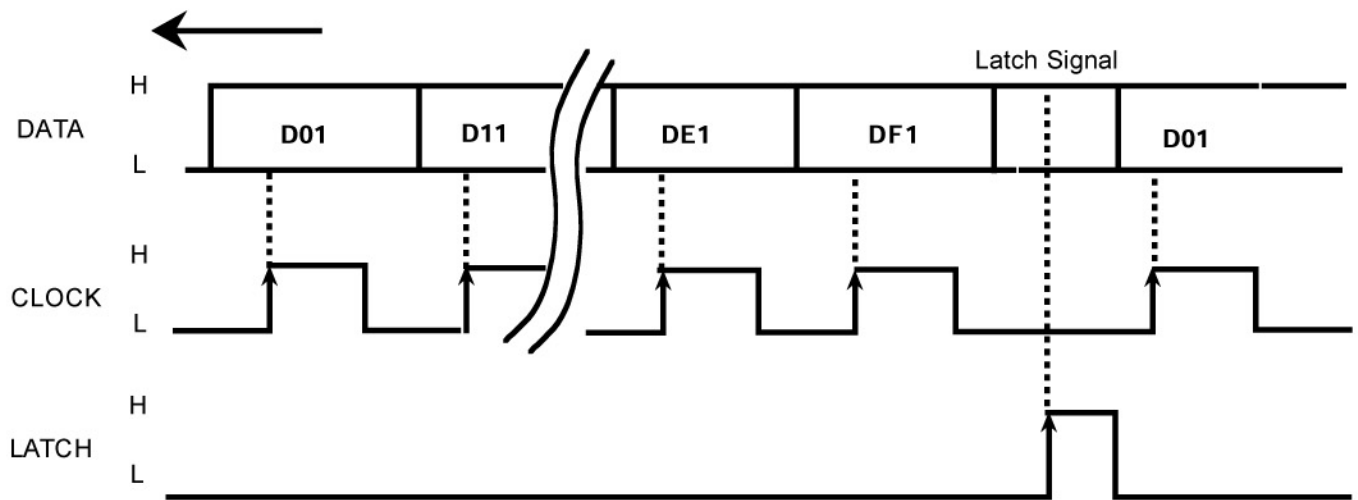
RECOMMENDED OPERATING CONDITION (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
VCC	Supply voltage		4.5	5.0	5.5	V
VIH	Logic"H"level input voltage		Vcc×0.7	—	VCC	V
VIL	Logic"L"level input voltage		GND	—	Vcc×0.3	V

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icc	Circuit Current	No Signal	—	30	50	mA
GV	Voltage Gain	Vi=200mVrms, f=1KHz Bypass, L/Rch	-3	0	3	dB
THD	Total Harmonic Distortion	Vi=200mVrms, f=1KHz Bypass, L/Rch	—	0.006	0.06	%
Vimax	Maximum Input Voltage	THD=1%, f=1KHz Bypass, L/Rch	1.0	1.4	—	Vrms
Vomax	Maximum Output Voltage	THD=1%, f=1KHz Bypass, L/Rch	1.0	1.4	—	Vrms
Vno	Output Noise Voltage	Rg=0, JIS-A Bypass, L/Rch	—	4	10	□Vrms
CS	Channel Separation	Vi=200mVrms, f=1KHz Bypass, L/Rch	—	-80	-65	dB
GV-D	Digital Delay Voltage Gain	Vi=200mVrms, f=1KHz 34pin input, 23pin output Td=40ms	-3	0	3	dB
THD-D	Digital Delay Total Harmonic Distortion	Vi=200mVrms, f=1KHz 34pin input, 23pin output Td=40ms	—	0.6	1.8	%
Vomax-D	Digital Delay Maximum Output Voltage	THD=10%, f=1KHz 34pin input, 23pin output Td=40ms	0.7	1.0	—	Vrms
Vno-D	Digital Delay Output Noise Voltage	Rg=0, JIS-A 23pin output Td=40ms	—	50	300	□Vrms

DATA and CLOCK



The DATA is read by rising edge of CLOCK signal, and
DATA is loaded by rising edge of LATCH signal.

DATA CONTROL SPECIFICATION

Chip address

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
Mode	Input Mode	Center ON/OFF	Rear effect	Surround effect	Delay time		Delay LPF	Delay ON/OFF	Delay gain		Delay feed back			1	0

SETTING CODE

(1) Mode (Bypass/QSurround™5.1)

MODE	D0
By pass	0
QSurround™5.1	1

(2) INPUT

INPUT	D1
Mono	0
Stereo	1

(3) CENTER

INPUT	D2
OFF	0
ON	1

(4) Surround output

Surround output	D3
OFF	0
ON	1

(5) Surround effect

Surround effect	D4
Narrow	0
Wide	1

(6) Delay time

Delay time (msec)	D5	D6
20	0	0
30	1	0
40	0	1
50	1	1

(7) Delay LPF

Cut-off frequency

Cut-off frequency	D7
f _c =3KHz	0
7KHz	1

(9) Delay gain

Delay gain	D9	DA
Gain 1 Low	0	0
2	1	0
3	0	1
4 High	1	1

(10) Delay feed back gain

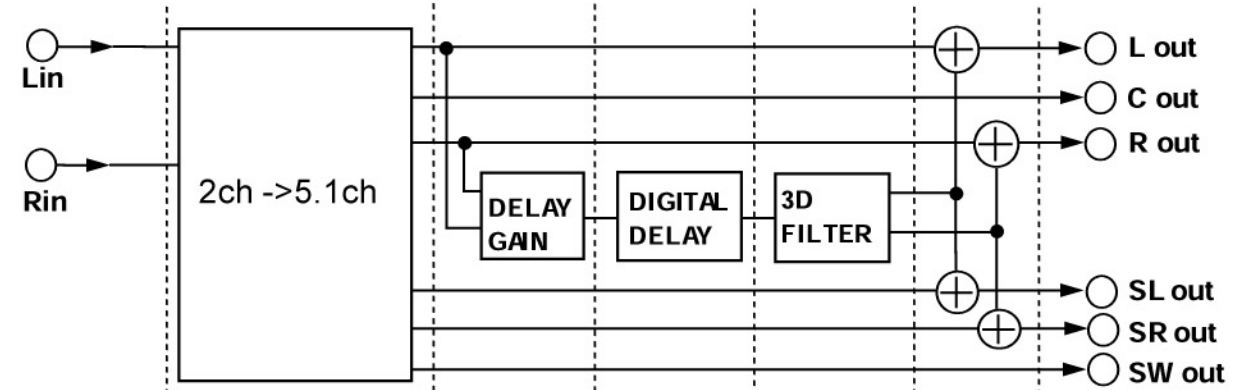
Feedback gain	DB	DC	DD
- 3dB	0	0	0
- 6dB	1	0	0
- 9dB	0	1	0
- 12dB	1	1	0
- ∞	1	1	1

(8) Delay effect

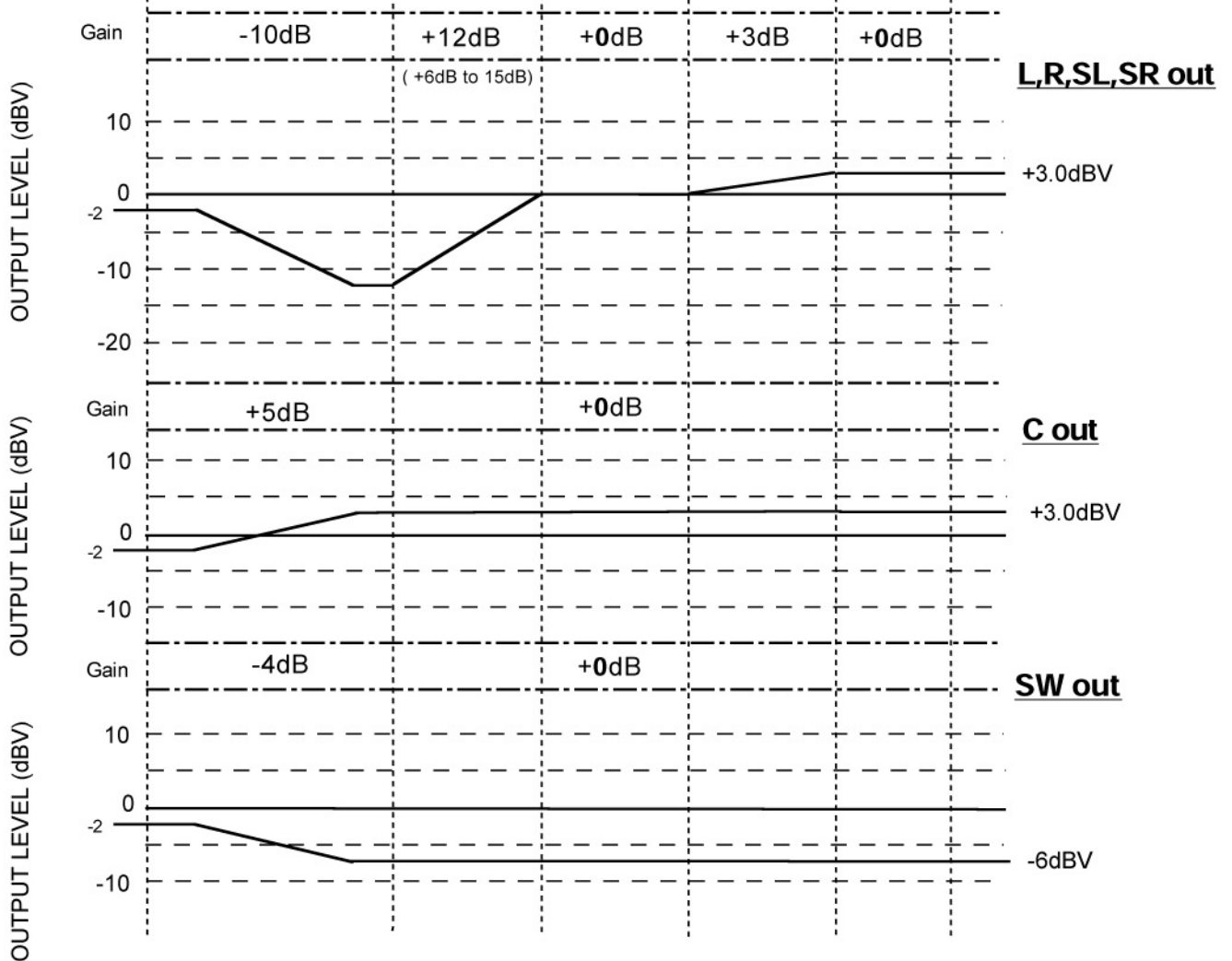
Delay effect	D8
OFF	0
ON	1

Level Diagram

QSurround™5.1 MODE



**INPUT
L,R IN**



Application circuit

