155Mbps ATM SAR

General Description

The TC358541F chip has been designed for use in an Asynchronous Transfer Mode (ATM) User Network Interface (UNI). Packet stream to/from ATM link trough packet buffer, traffic shaping and buffer management per VP and VC basis, and full support for the ATM Forum UNI 4.0 traffic management specifications is provided, as well as the standard UTOPIA interface.

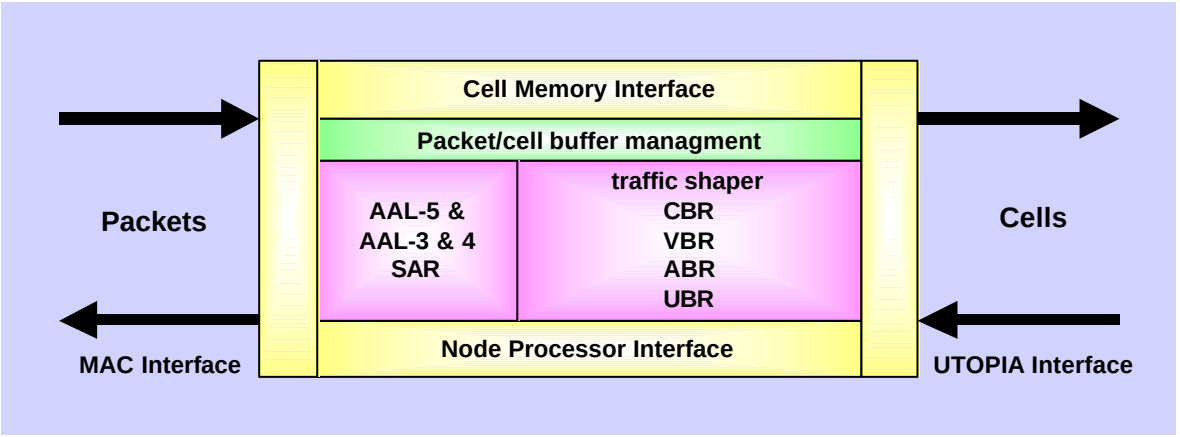
Transmit packets are sent to the TC358541F chip on a flow-controlled, byte-wide interface. Each packet contains a circuit identifier header. A packet is segmented according to the AAL type specified for that circuit and is placed on a linked-list cell queue in SRAM buffer. The cell queue is managed per VC and VP basis. Up to 4095 circuits are supported. The cell queues are served by a traffic shaper, which allows CBR, VBR, ABR and UBR traffic.

The TC358541F chip implements UBR with PCR and MCR parameters. Also, ABR using the explicit rate flow control (ER) ATM Forum UNI 4.0 compliant and Generic Flow Control (GFC) ITU-T SG13 are supported. The TC358541F chip receives cells via the UTOPIA interface. VPI/VCI(MID) fields are then mapped to a local circuit identifier directly. Cells are checked and reassembled on a linked-list cell queue in SRAM buffer. The reassembled packet is moved to one of two packet queues according to the priority set per circuit. All CRCs are also checked. The packets are then passed to the receive MAC interface with flow-control, where a header is attached to identify the associated circuit.

Features

- Full OC3/STM-1 line-rate segmentation and reassembly for UTOPIA link
- Up to 4095 VPI/VCI circuits supported and up to 1K MIDs per VPI/VCI circuit
- ABR (ATM Forum UNI 4.0 compliant)
- UBR with MCR parameter
- ITU-T and ATM Forum compliant ATM User Network Interface
- AAL5 and AAL3/4 SAR support
- Supports up to 4 VPs with bandwidth allocation
- Supports PVC and SVC connections
- Supports F4 and F5 OAM flows
- Traffic shaper supporting peak rate, sustained rate,minimum guaranteed rate, maximum burst size and priority level per VC basis
- GFC support
- UTOPIA Level 1 compliant media interface
- 32-bit CRC generation and checking for AAL5
- Transmit buffer management per VC and VP basis
- Open MAC-style interface for packet transfer up to 200 Mbps with flow control
- Two priority packet queues in MAC-style receive interface
- M68000-style node processor interface
- Supporting 1 Megaword (64-bit word) SRAM buffer
- 0.3µm CMOS technology
- 3.3V power supply
- 3.3V I/O with 5V input tolerance
- -40 … +85°C temperature range
- 240 pin HQFP package
  (body size 32x32 sqmm with 0.5mm pin pitch)

Block Diagram



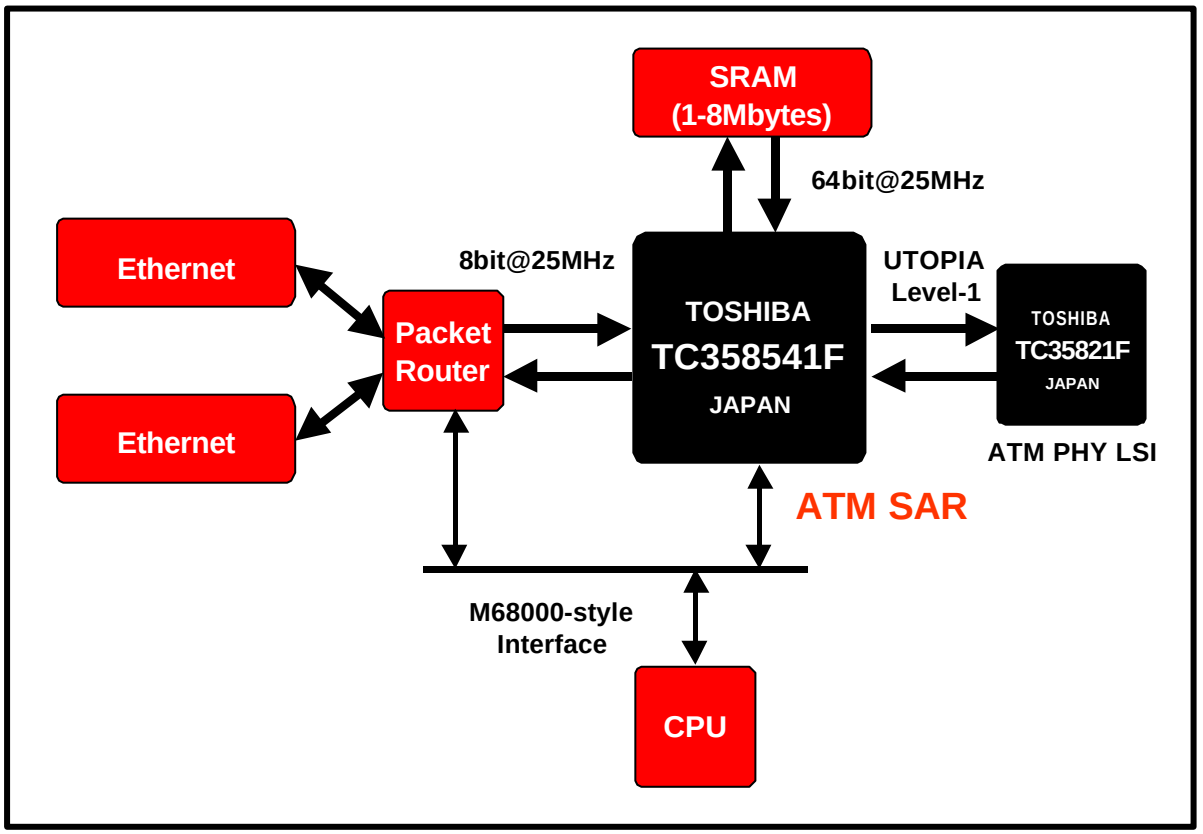
155Mbps ATM SAR

Applications

•High performance ATM switches and Hubs

Application Examples

•This is an Ethernet to ATM Switch system. A packet router between The TC358541F and Ethernet is developed with a visitor's specification for visitor itself.



CAUTION