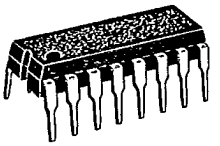
MN4018B/MN4018BS

Presettable Divide-by-N Counters

■ Description

The MN4018B/S are presettable divide-by-N counters composed of a 5-bit Johnson counter.
Frequency is divided into 1/2, 1/4, 1/6, 1/8 and 1/10 by connecting the output of $\overline{O}_0 \sim \overline{O}_4$ to D input, and frequency is also divided into 1/3, 1/5, 1/7 and 1/9 by connecting the output of $\overline{O}_0 \sim \overline{O}_4$ to the D input through gate.
MR and PL are asynchronous. When MR = "H", $\overline{O}_0 \sim \overline{O}_4$ are all "H"; when PL = "H", On is contradiction of Pn.
Counter advances by one on the going edge of CP input. Proper counter sequence is given since the lock protection gate is available.
The MN4018B/S are equivalent to MOTOROLA MC14018B and RCA CD4018B.

P-3



16-Pin • Plastic DIL Package

P-4

16-Pin • Panaflat Package (SO-16D)

■ Truth Table

CP	MR	PL	$P_0 \sim P_4$	$\overline{O}_n$
↘	L	L	×	$\overline{O}_n$
↗	L	L	×	$\overline{D}_n$
×	L	H	L	H
×	L	H	H	L
×	H	×	×	H

Note) × : don't care

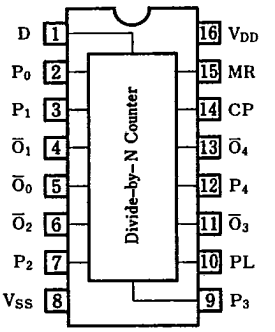
■ Functional Selection Table

Dividing number	Output to D	Remarks
10	$\overline{O}_4$	External connection is not necessary
8	$\overline{O}_3$	
6	$\overline{O}_2$	
4	$\overline{O}_1$	
2	$\overline{O}_0$	
9	$\overline{O}_3 \cdot \overline{O}_4$	External AND gate is necessary
7	$\overline{O}_2 \cdot \overline{O}_3$	
5	$\overline{O}_1 \cdot \overline{O}_2$	
3	$\overline{O}_0 \cdot \overline{O}_1$	

Pin Explanation

PL : Load input
$P_0 \sim P_4$: 4-bit input
D : Data input
CP : Clock input (↗)
MR : Reset input
$\overline{O}_0 \sim \overline{O}_4$: Output (4 bit)

Pin Configuration



■ Maximum Ratings (Ta=25℃)

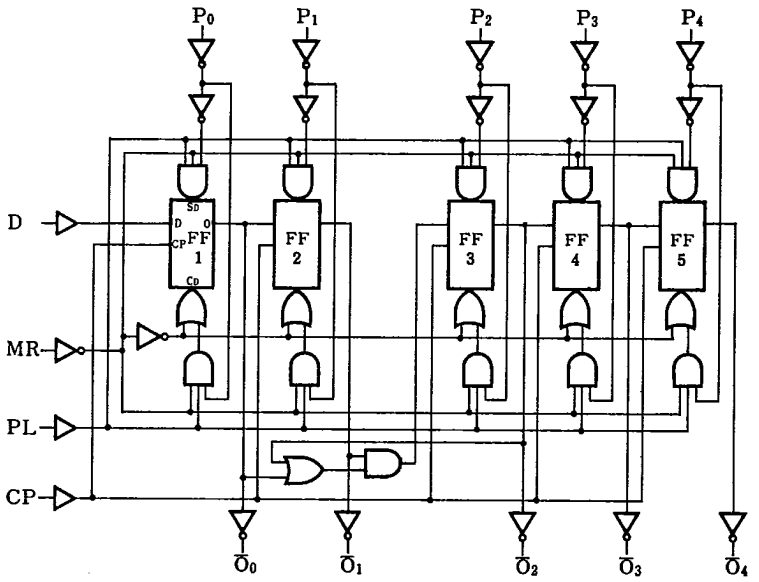
Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} |I_O|<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} |I_O|<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	|I_O|<1μA V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	|I_O|<1μA V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

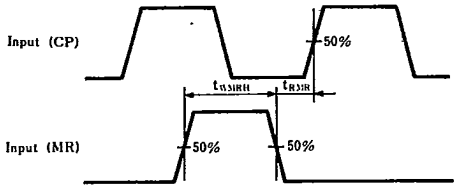
Logic Diagram



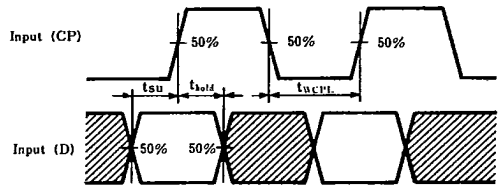
■ Switching Characteristics ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→$\overline{O}$ (H→L)	5	t_{PHL}	—	185	555	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time CP→$\overline{O}$ (L→H)	5	t_{PLH}	—	145	435	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time PL→$\overline{O}$ (H→L)	5	t_{PHL}	—	205	615	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time PL→$\overline{O}$ (L→H)	5	t_{PLH}	—	175	525	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time MR→$\overline{O}$ (L→H)	5	t_{PLH}	—	140	420	ns
	10		—	55	165	
	15		—	40	120	
Set-up Time D→CP	5	t_{su}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
Hold Time D→CP	5	t_{hold}	—	−45	30	ns
	10		—	−15	10	
	15		—	−10	10	
Minimum Clock Pulse Width	5	t_{WCPL}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Minimum MR Pulse Width	5	t_{WMRH}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
Minimum PL Pulse Width	5	t_{WPLH}	—	75	225	ns
	10		—	25	75	
	15		—	20	60	
MR Recovery Time	5	t_{RMR}	—	70	210	ns
	10		—	20	60	
	15		—	15	45	
PL Recovery Time	5	t_{RPL}	—	85	255	ns
	10		—	30	90	
	15		—	20	60	
Maximum Clock Frequency	5	fmax	2	4	—	MHz
	10		6	11	—	
	15		8	16	—	
Input Capacitance		C_I	—	—	7.5	pF

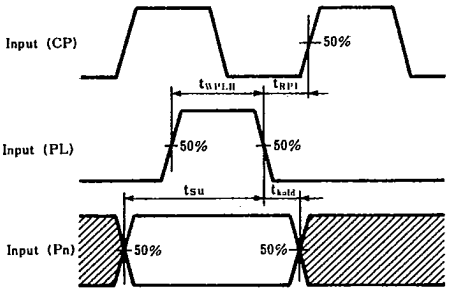
• Dynamic Signal Waveforms



Waveforms showing minimum MR pulse width and MR recovery time



Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D



Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL; set-up and hold times are shown as positive values but may be specified as negative values.

■ Timing Diagram