CY74FCT16501T
CY74FCT162501T
CY74FCT162H501T

SCCS057B - August 1994 - Revised September 2001

18-Bit Registered Transceivers

Features

- **I_{off} supports partial-power-down mode operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6 mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16501T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162501T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**

CY74FCT162H501T Features:

- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

These 18-bit universal bus transceivers can be operated in transparent, latched or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock inputs (CLKAB and CLKBA). For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by $\overline{OEBA}$, LEBA, and CLKBA.

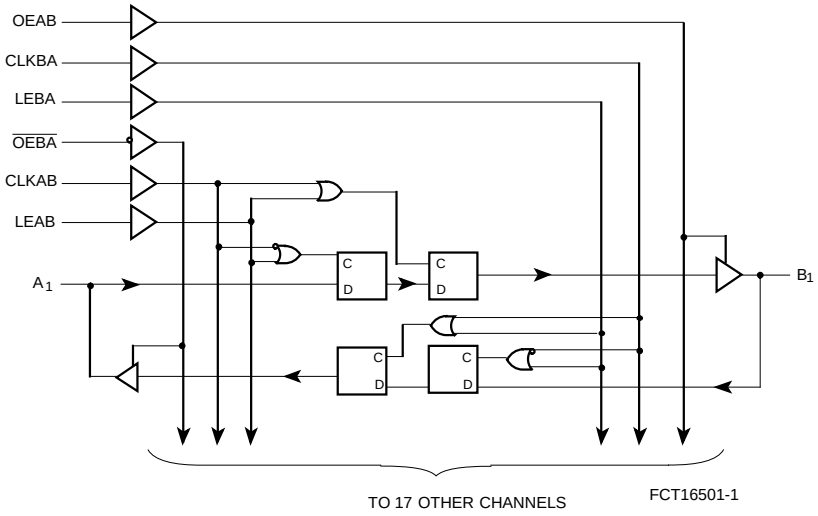
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16501T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

THE CY74FCT162501T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162501T is ideal for driving transmission lines.

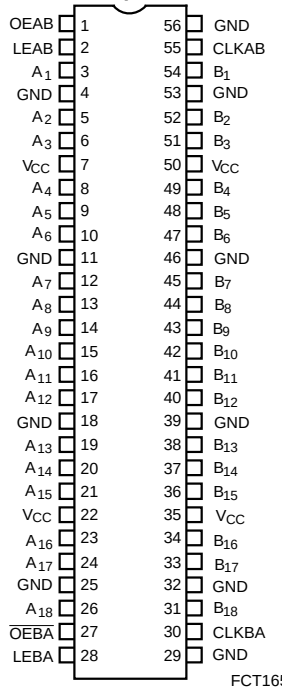
The CY74FCT162H501T is a 24-mA balanced output part, that has “bus hold” on the data inputs. The device retains the input’s last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

Functional Block Diagram



Pin Configuration

SSOP/TSSOP
Top View



FCT16501-2

Pin Description

Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs[1]
B	B-to-A Data Inputs or A-to-B Three-State Outputs[1]

Function Table[2, 3]

Inputs				Outputs
OEAB	**LEAB**	**CLKAB**	**A**	**B**
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	⌟⌜	L	L
H	L	⌟⌜	H	H
H	L	L	X	B[4]
H	L	H	X	B[5]

Maximum Ratings[6, 7]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied..... –55°C to +125°C

DC Input Voltage..... –0.5V to +7.0V

DC Output Voltage..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin)..... –60 to +120 mA

Power Dissipation..... 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	5V ± 10%

Notes:

1. On the 74FCT162H501T these pins have bus hold.
2. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance
   ⌟⌜ = LOW-to-HIGH Transition
4. Output level before the indicated steady-state input conditions were established.
5. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
6. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
7. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Conditions		Min.	Typ.[8]	Max.	Unit
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_H	Input Hysteresis[9]					100		mV
V_{IK}	Input Clamp Diode Voltage		V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	Standard	V_{CC}=Max., V_I=V_{CC}				±1	µA
		Bus Hold					±100	
I_{IL}	Input LOW Current	Standard	V_{CC}=Max., V_I=GND				±1	µA
		Bus Hold					±100	µA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[10]		V_{CC}=Min.,	V_I=2.0V	−50			µA
				V_I=0.8V	+50			µA
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[10]		V_{CC}=Max., V_I=1.5V				TBD	mA
I_{OZH}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=2.7V				±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=0.5V				±1	µA
I_{OS}	Short Circuit Current[11]		V_{CC}=Max., V_{OUT}=GND		−80	−140	−200	mA
I_O	Output Drive Current[11]		V_{CC}=Max., V_{OUT}=2.5V		−50		−180	mA
I_{OFF}	Power-Off Disable		V_{CC}=0V, V_{OUT}≤4.5V[12]				±1	µA

Output Drive Characteristics for CY74FCT16501T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162501T, CY74FCT162H501T

Parameter	Description	Test Conditions	Min.	Typ.[8]	Max.	Unit
I_{ODL}	Output LOW Current[11]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[11]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Notes:

8. Typical values are at V_{CC}= 5.0V, T_A= +25˚C ambient.
9. This parameter is specified but not tested.
10. Pins with bus hold are described in Pin Description.
11. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
12. Tested at +25˚C.

Capacitance[9] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[8]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Sym.	Parameter	Test Conditions[13]		Min.	Typ.[8]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN}\leq$0.2V $V_{IN}\geq V_{CC}$–0.2V	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current TTL inputs HIGH	V_{CC}= Max., V_{IN} = 3.4V[14]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[15]	V_{CC}=Max., Outputs Open OEAB=$\overline{OEBA}$=V_{CC} or GND One Input Toggling, 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[16]	V_{CC}=Max., Outputs Open f_0 =10MHz (CLKAB) 50% Duty Cycle OEAB=$\overline{OEBA}$=V_{CC} LEAB = GND, One Bit Toggling f_1 = 5MHz, 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	
		V_{CC}=Max., Outputs Open f_0 = 10MHz (CLKAB) 50% Duty Cycle OEAB=$\overline{OEBA}$=V_{CC} LEAB=GND Eighteen Bits Toggling f_1=2.5MHz, 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	3.8	6.5[17]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.5	20.8[17]	

Notes:

13. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
14. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
15. This parameter is not directly testable, but is derived for use in Total Power Supply.
16. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
17. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[18]

Parameter	Description		CY74FCT16501AT CY74FCT162501AT		CY74FCT162501CT CY74FCT162H501CT		Unit	Fig. No.[19]
			Min.	Max.	Min.	Max.		
f_{MAX}	CLKAB or CLKBA frequency[20]		—	150	—	150	MHz	—
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A		1.5	5.1	1.5	4.6	ns	1,3
t_{PLH} t_{PHL}	Propagation Delay LEBA to A, LEAB to B		1.5	5.6	1.5	5.3	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay CLKBA to A, CLKAB to B		1.5	5.6	1.5	5.3	ns	1,5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to A, $\overline{OEAB}$ to B		1.5	6.0	1.5	5.6	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to A, $\overline{OEAB}$ to B		1.5	5.6	1.5	5.2	ns	1,7,8
t_{SU}	Set-Up Time, HIGH or LOW A to CLKAB, B to CLKBA		3.0	—	3.0	—	ns	4
t_H	Hold Time HIGH or LOW A to CLKAB, B to CLKBA		0	—	0	—	ns	4
t_{SU}	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock LOW	3.0	—	3.0	—	ns	4
		Clock HIGH	1.5	—	1.5	—	ns	4
t_H	Hold Time, HIGH or LOW, A to LEAB, B to LEBA		1.5	—	1.5	—	ns	4
t_W	LEAB or LEBA Pulse Width HIGH[20]		3.0	—	3.0	—	ns	5
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[20]		3.0	—	3.0	—	ns	5
$t_{SK(O)}$	Output Skew[21]		—	0.5	—	0.5	ns	—

Notes:

18. Minimum limits are specified, but not tested, on propagation delays.
19. See “Parameter Measurement Information” in the General Information section.
20. This parameter is guaranteed but not tested.
21. Skew between any two outputs of the same package switching in the same direction. This parameter ensured by design.

Ordering Information CY74FCT16501T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	CY74FCT16501ATPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162501T

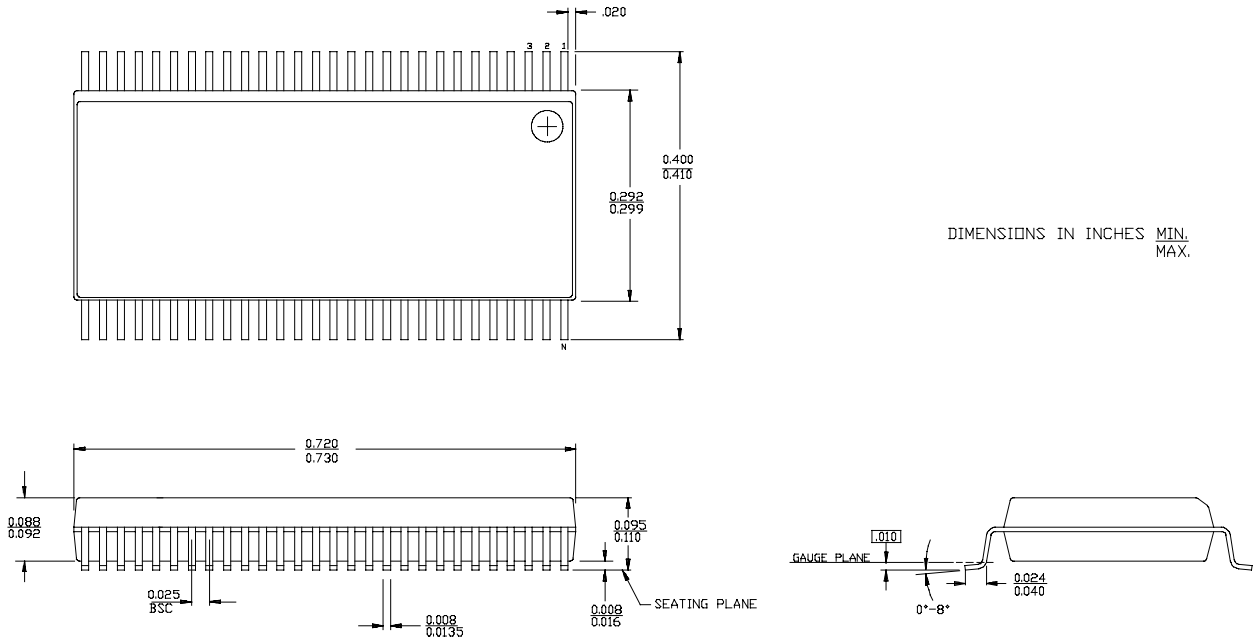
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	74FCT162501CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162501CTPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162501CTPVCT	O56	56-Lead (300-Mil) SSOP	
5.1	74FCT162501ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162501ATPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162501ATPVCT	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H501T

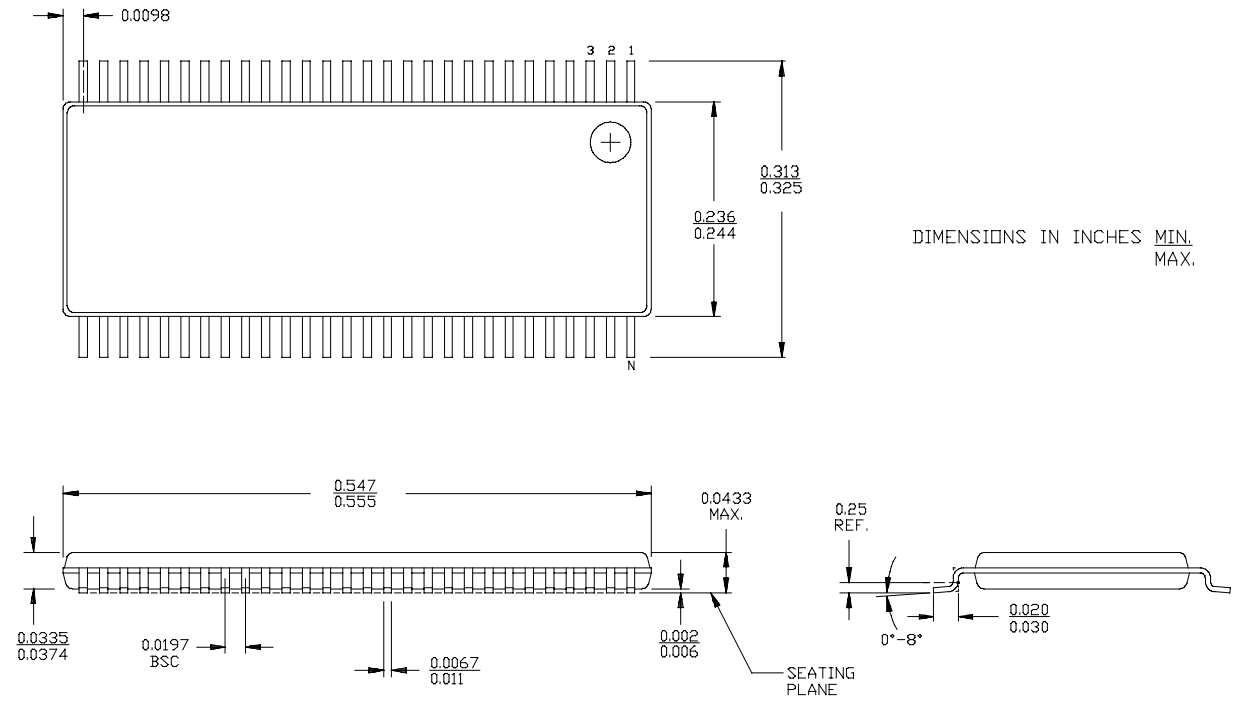
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	74FCT162H501CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	74FCT162H501CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74FCT162501ATPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162501CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162501CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162501ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
74FCT162501ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
74FCT162H501CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162H501CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162H501ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
74FCT162H501ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
74FCT162H501ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
74FCT162H501ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
74FCT16501ATPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162501ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT162501ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT16501ATPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16501ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT16501ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT16501ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT16501ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
FCT162501ATPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162501CTPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162501CTPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162501CTPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162H501CTPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162H501CTPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162H501CTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

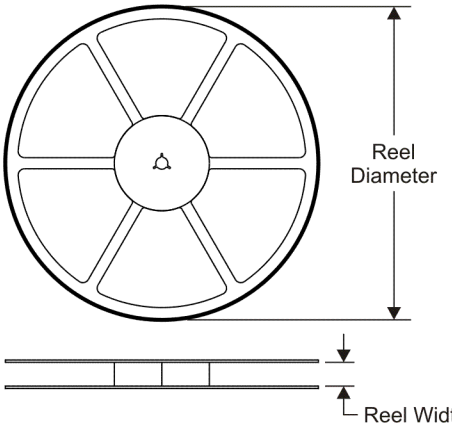
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

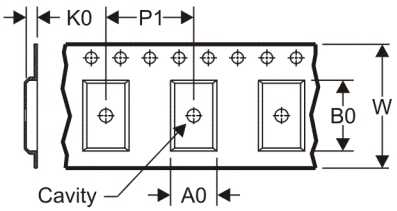
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

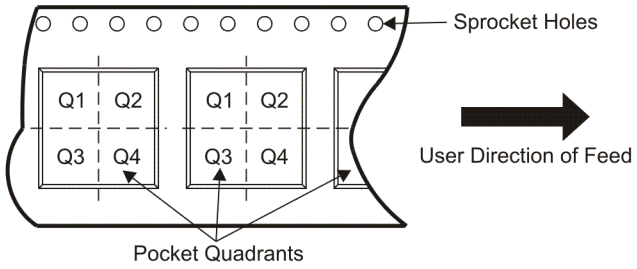


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

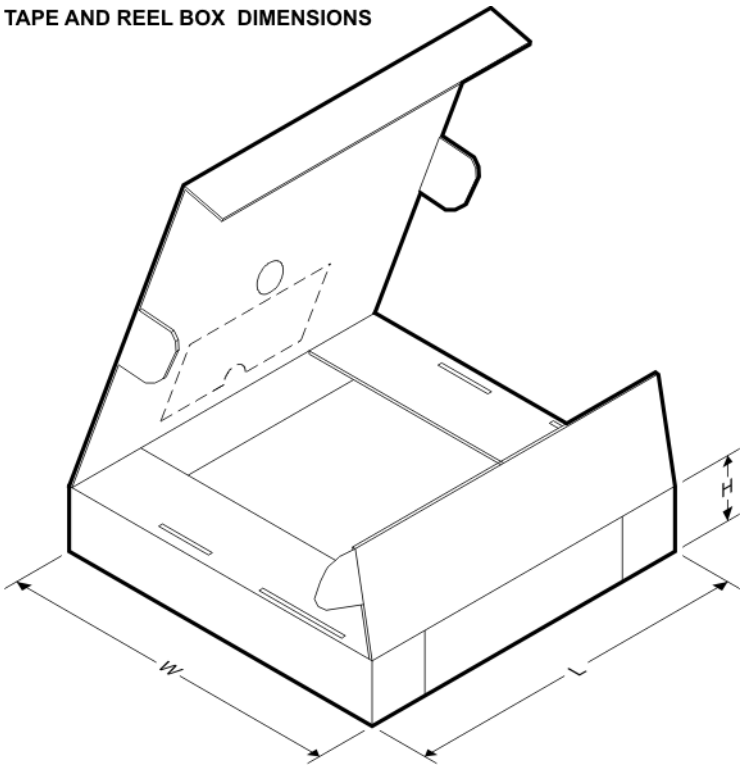
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162501ATPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
74FCT162501CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
74FCT162501CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
74FCT162H501CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

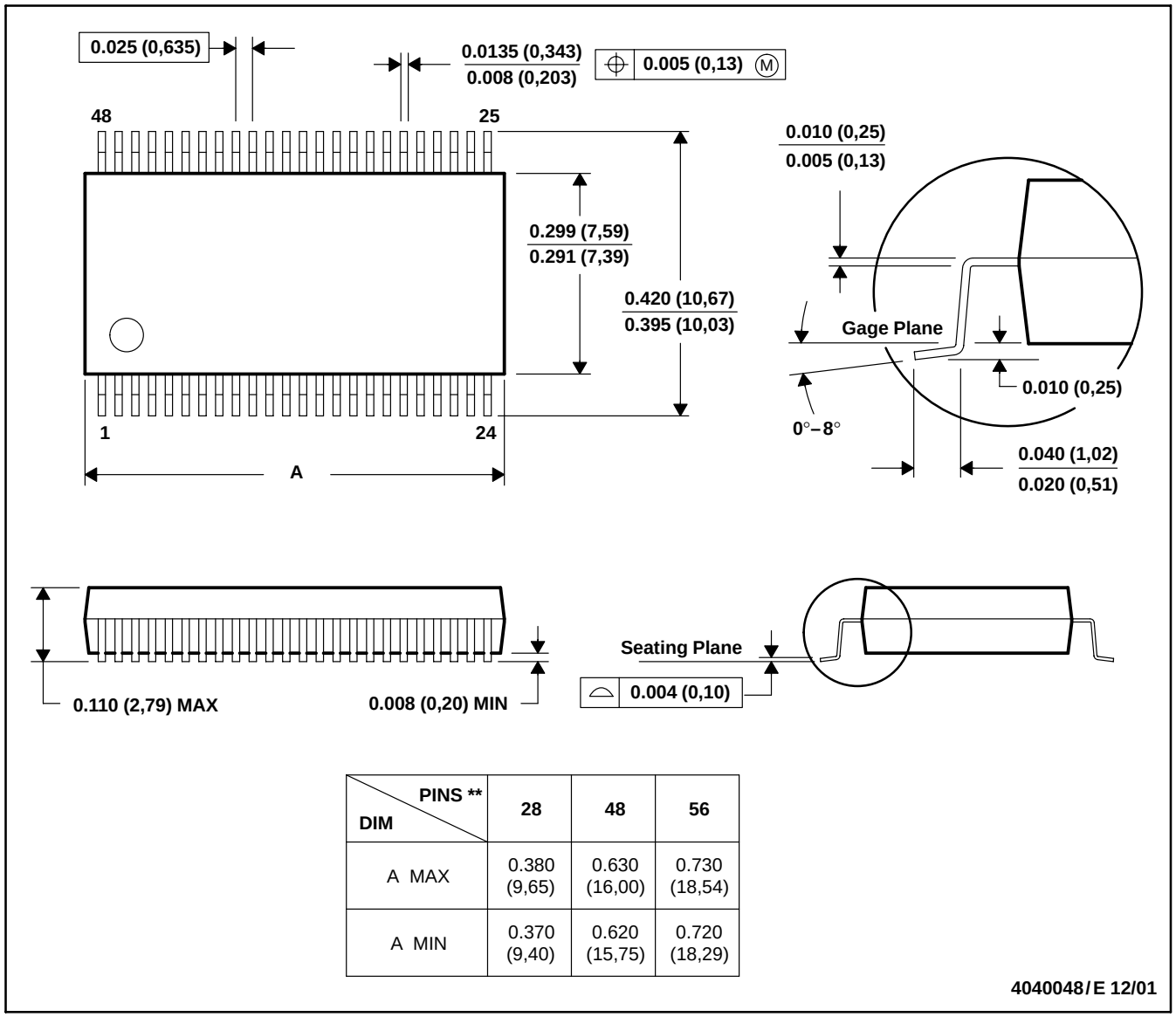


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162501ATPVCT	SSOP	DL	56	1000	346.0	346.0	49.0
74FCT162501CTPACT	TSSOP	DGG	56	2000	346.0	346.0	41.0
74FCT162501CTPVCT	SSOP	DL	56	1000	346.0	346.0	49.0
74FCT162H501CTPACT	TSSOP	DGG	56	2000	346.0	346.0	41.0

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



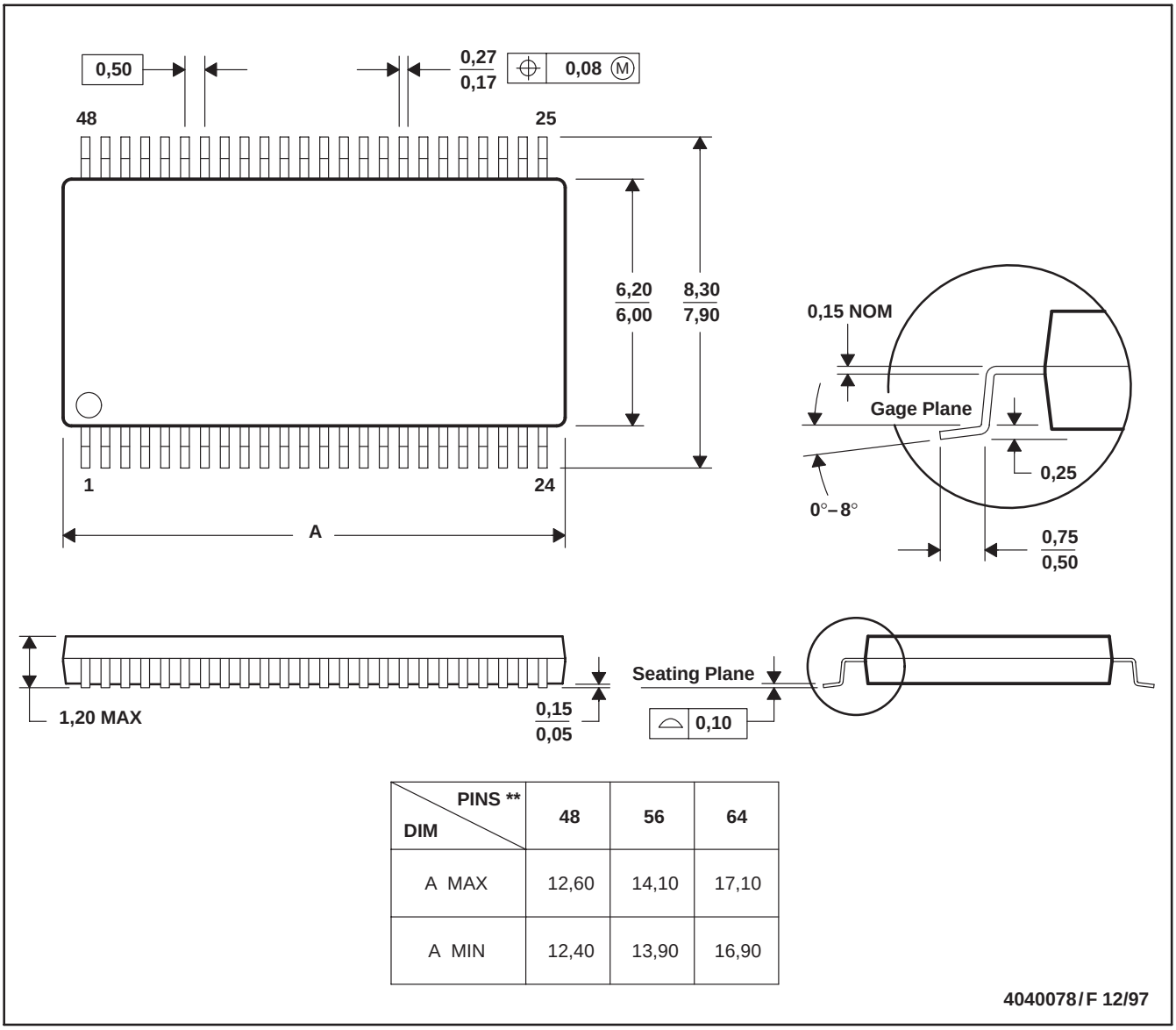
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74FCT162501ATPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85	FCT162501A	
74FCT162501CTPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85	FCT162501C	
74FCT162H501CTPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85	FCT162H501C	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

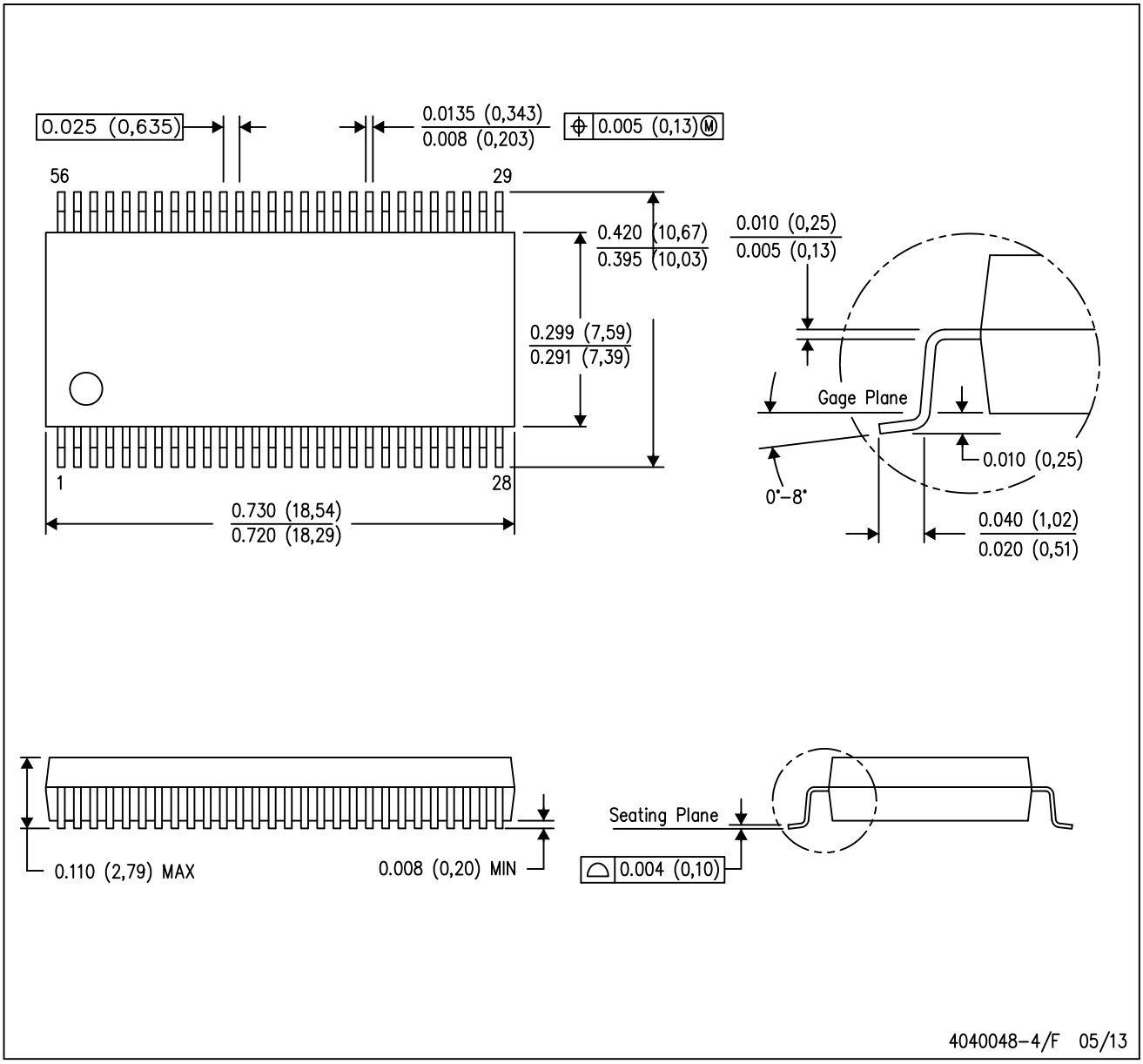
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

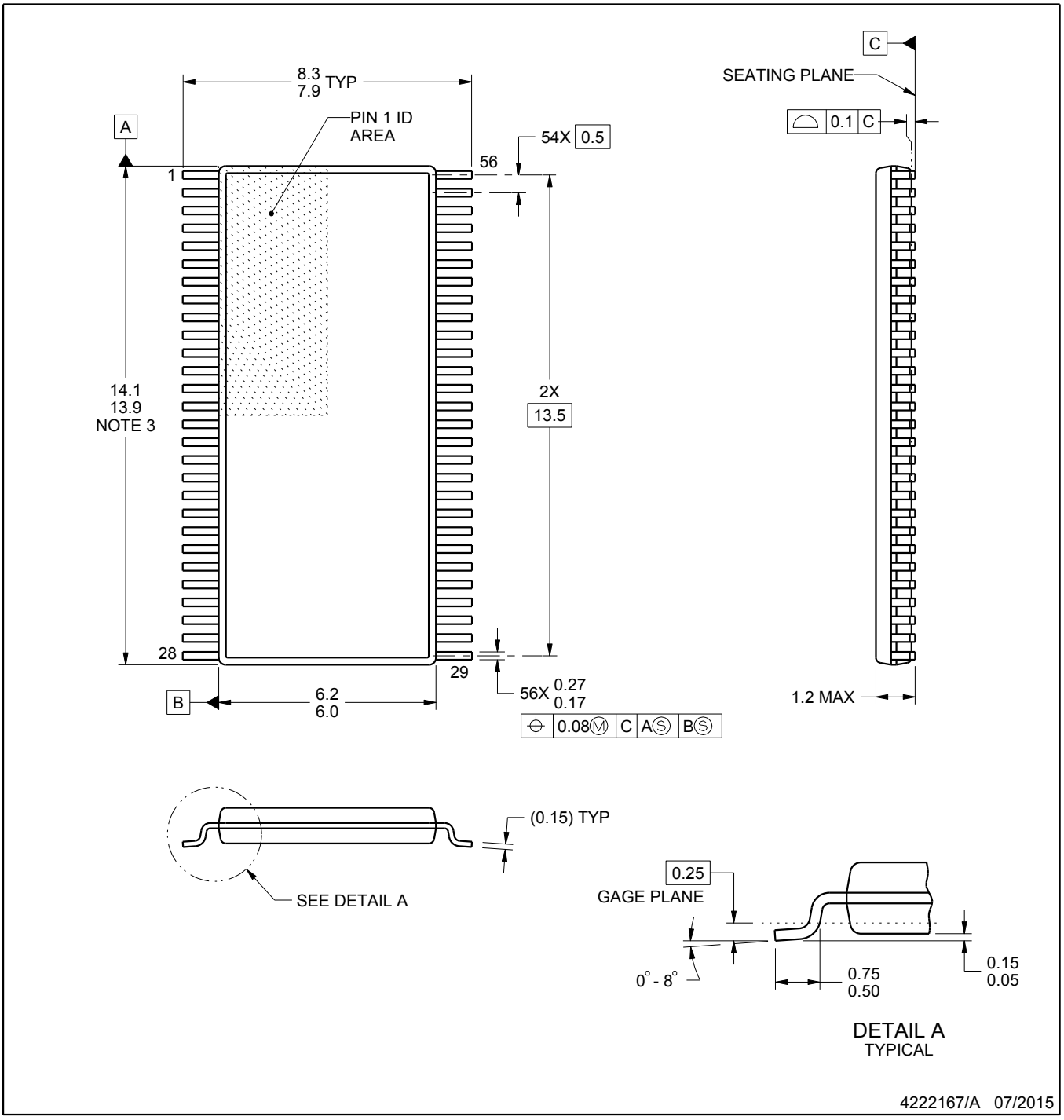
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

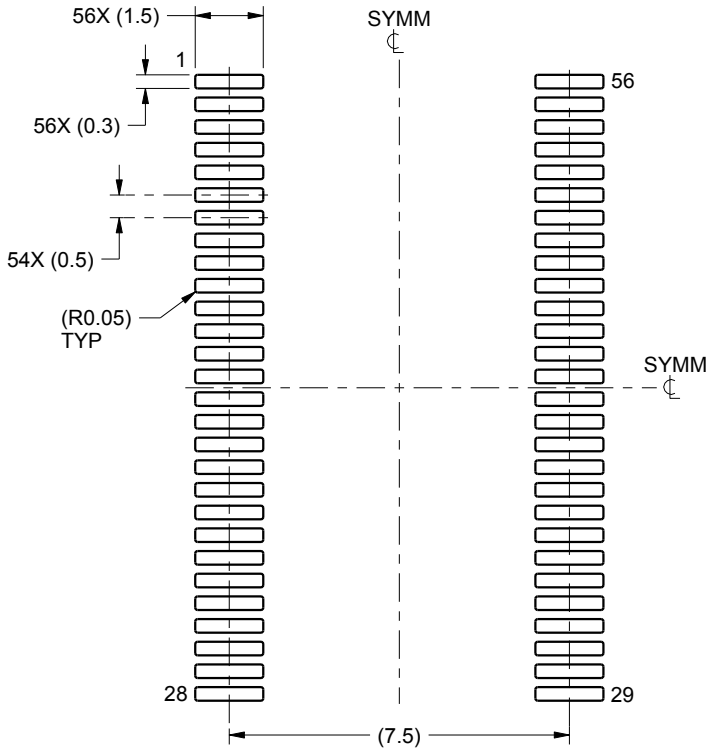
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

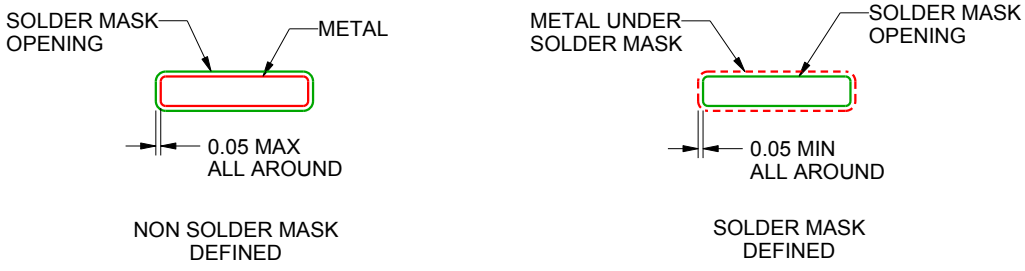


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

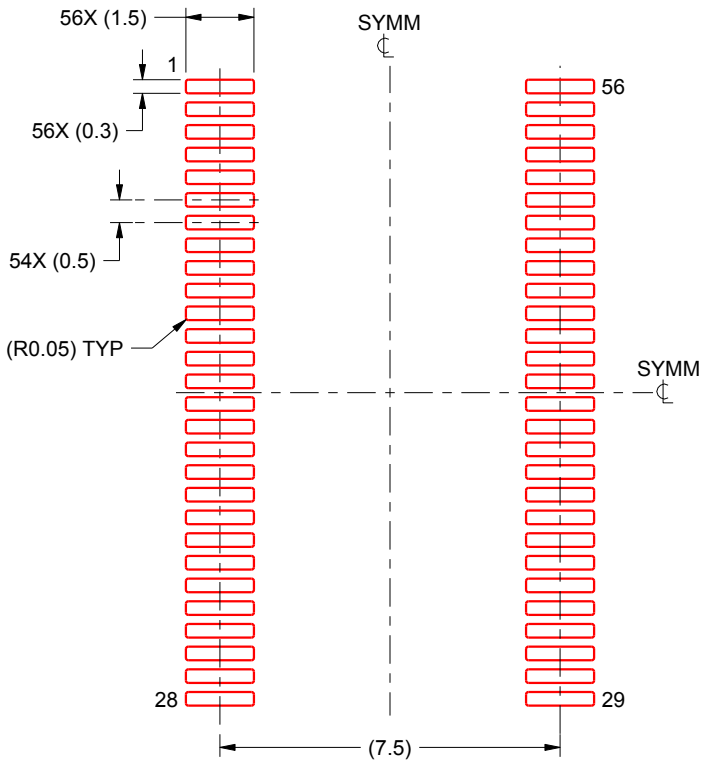


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265