Enpirion® Power Evaluation Board

ED8101 Digital Single-Phase PWM controller Evaluation Board User Guide

Description

The ED8101 is a true-digital single-phase PWM controller optimally configured for use with the Altera Power Train ET4040. The ET4040 is a 40A, high speed, high density, monolithic power stage IC with integrated current and temperature sensing features in a 5.5mm x 7.5mm x 0.95mm, 46 pin QFN package.

Evaluation Board Overview

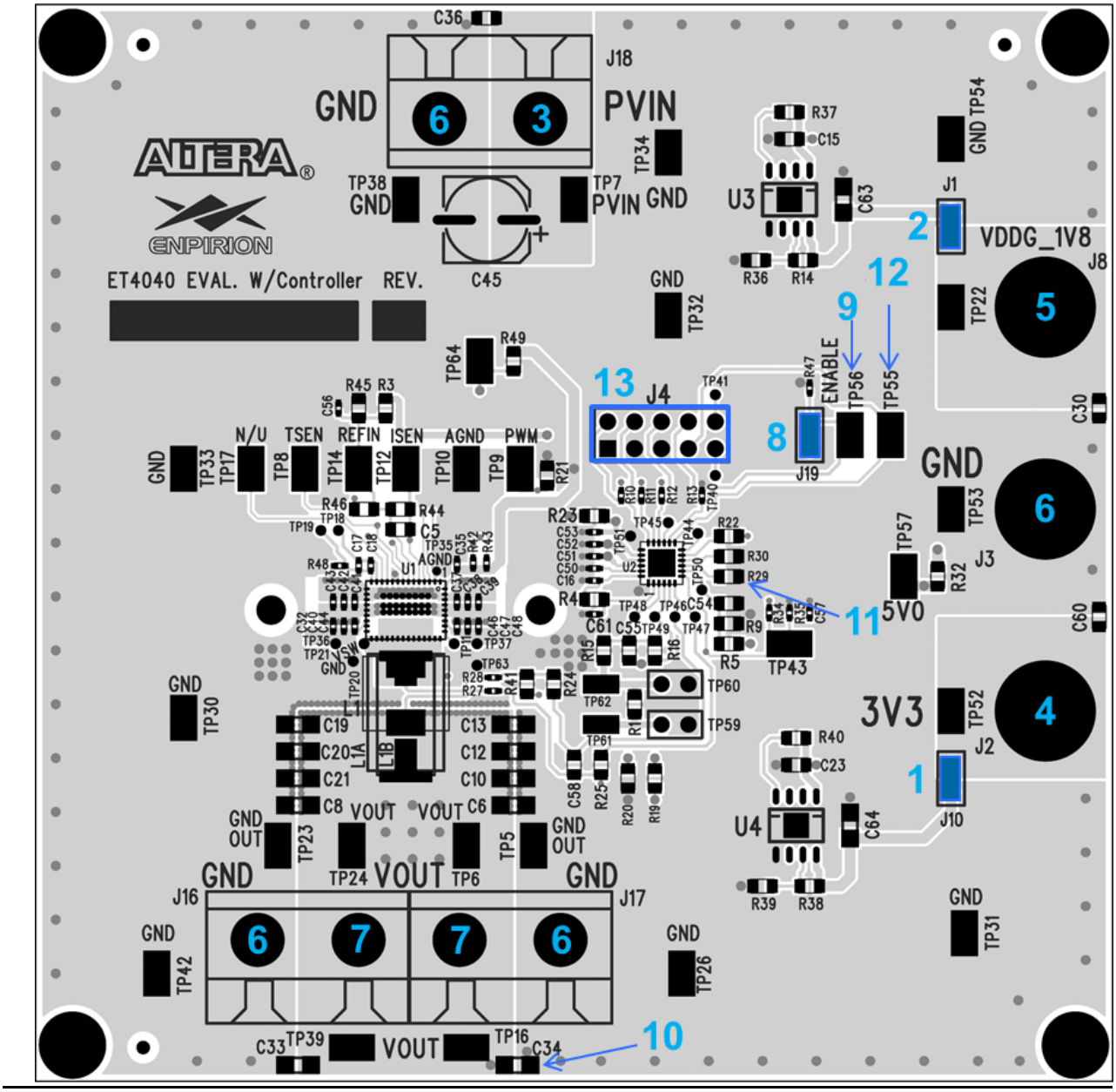


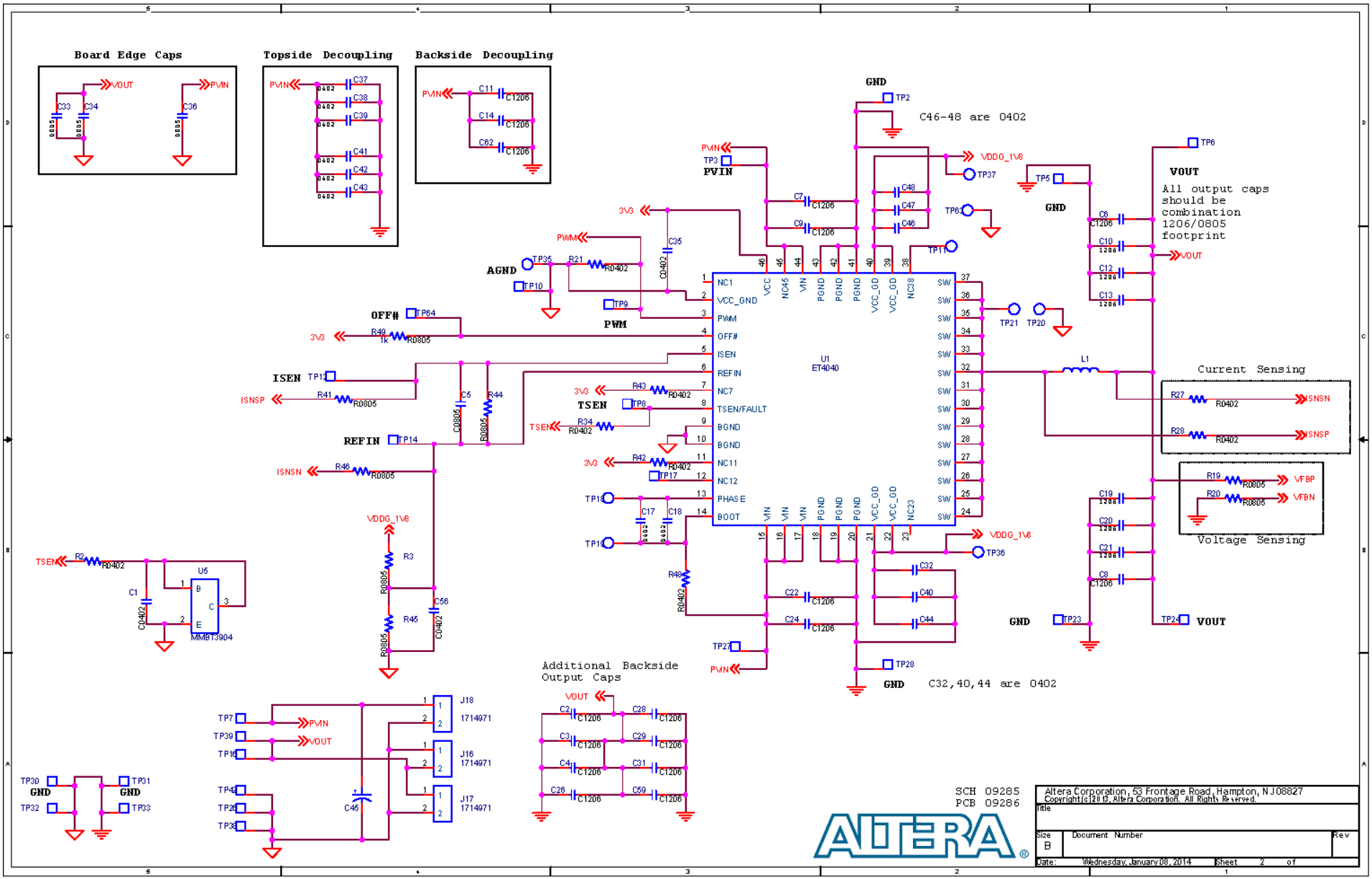
Figure 1. ET4040 and ED8101 Evaluation Board Illustration (Top Layer)

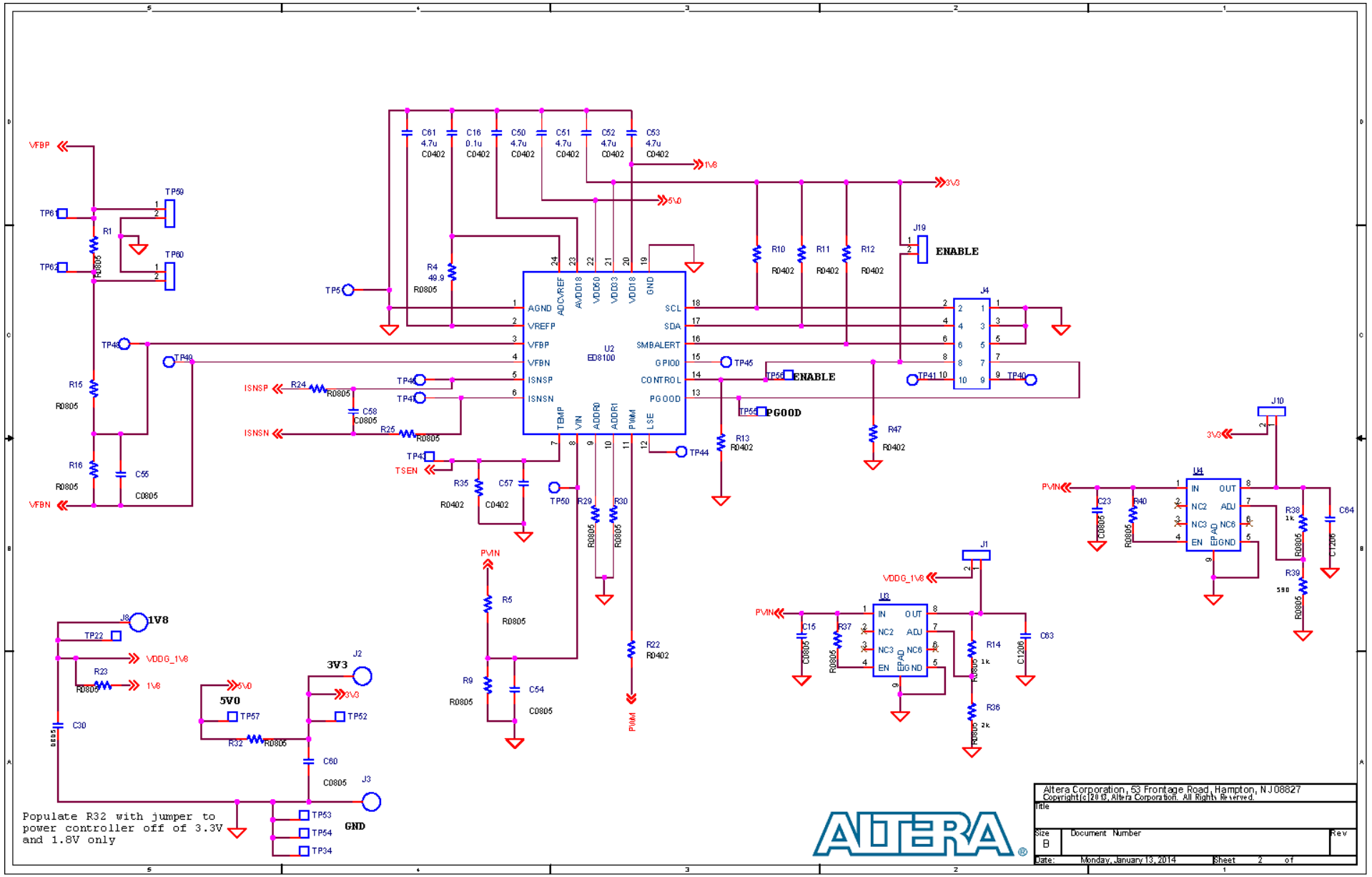
Instructions

The numbers in the instructions below correspond to the numbers in Figure 1.

1) **PVIN to VCC (3.3V) Control Voltage LDO Connector (J10)** – Add jumper to J10 to supply the control voltage to both ET4040 and controller ED8101 from PVIN through a LDO, otherwise this control voltage has to be supplied from external separate power supply.
2) **PVIN to ET4040 Gate Drive (VDDG_1V8) LDO Connector (J1)** – Add jumper to J1 to supply the ET4040 gate drive voltage (1.8V) from PVIN through a LDO, otherwise this gate drive voltage has to be supplied from external separate power supply.
3) **PVIN (J18)** – Connect 4.5V to 14.5V supply on J18. Do not turn on until everything is connected correctly.
4) **VCC –** if the jumper J10 was not set, an external 3.3V control voltage supply has to be provided to power the controller and power train.
5) **ET4040 Gate Drive Voltage (VDDG_1V8)** – if the jumper J1 was not set, an external supply has to be provided to power the gate drive voltage.
6) **GND** – Connect the input ground to J18 and the output ground to J16, J17.
7) **VOUT** – Connect the load to J16, J17.
8) **ENABLE (J19)** – The jumper on J19 enables the digital controller ED8101 if this controller has been pre-configured. Please note that do not connect J19 and J14 simultaneously as it will overdrive the enable signal.
9) **ENABLE test point (TP56)** - Leave J19 open and use an external signal to TP56 to toggle the enable on and off.
10) **Output Voltage Sensing Point (C34)** – The output voltage differential sensing is across the board edge decoupling capacitor C34, this is the best probe location for output ripple, load regulation and load transient.
11) **PMBus address selection resistor (R29, R30)** – These two resistors on the evaluation board are zero Ohm, so the PMBus address is 0x40, please refer to the datasheet of ED8101 for more information about the PMBus selection via external resistors.
12) **PGOOD (TP55)** - This is the digital output pin which indicates the state of the power rail. The power good thresholds are stored in the controller device as factor relative to the nominal output voltage.
13) **Digital Interface Connector (J14)** – This evaluation board can be interfaced with user PC through the PMBus communication interface. The digital controller ED8101 can be re-configured or monitored using the ED81xx Power Designer Graphic User Interface (GUI) software. Please refer to the Power Designer GUI user guild for more information about configuring or monitoring the digital controller.

Evaluation Board Schematic




U2
ED8100
AGND
VREFP
VFBP
VFBN
ISNSP
ISNSN
TEMP
VIN
ADDR0
ADDR1
PWM
LSE
ADCVREF
AVDD18
VDD50
VDD33
VDD18
GND
SCL
SDA
SMBALERT
GPIO0
CONTROL
PGOOD
ENABLE
PGOOD
1V8
3V3
5V0
PVIN
VDDG_1V8
TSEN
PWM
Populate R32 with jumper to power controller off of 3.3V and 1.8V only
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Size B
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Rev
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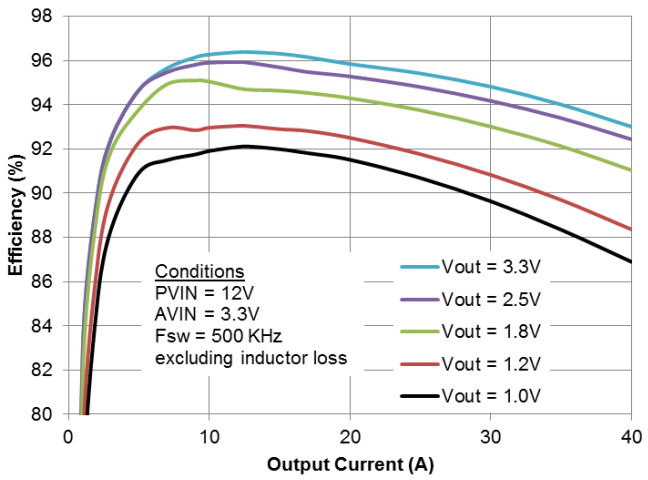
Bill of Materials

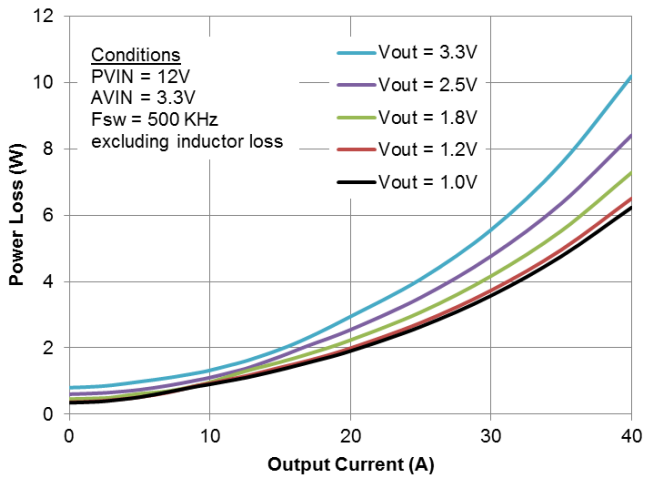
Designator	Qty	Description
C10, C12, C20, C21, C33, C34	6	CAP CER 47UF 20% 6.3V X7S 1206
C13, C19	2	CAP CER 100UF 6.3V X5R 1206
C15, C23, C30, C60	4	CAP CER 10UF 16V 10% X5R 1206
C55	1	CAP CERAMIC 22PF 50V NP0 0805
C9, C11, C14, C22, C62-64	7	CAP CER 22UF 25V 10% X5R 1206
C16	1	CAP CER 0.1UF 25V X5R 0402
C17, C18	2	CAP CER 0.22UF 16V X7R 0402
C35, C37, C38, C40-42, C44, C46, C47		CAP CER 1.0UF 16V X5R 10% 0402
C50-53, C61		CAP CERAMIC 4.7UF 6.3V X5R 0402
C45		CAP ELECT 150UF 25V FK SMD
J2, J3, J8		BANANA JACK
J4		DUAL ROW 5 PINS/ROW SQUARE POST HEADER CENTERLINE: 0.1" (2.54MM)
J16-J18		TERMINAL BLOCK, 2 POSITION, 32A, PCB MOUNT
J1, J10, J19		CONN HEADER 2POS 0.1" T/H
L1		130nH 10.5 x 9.5 x 8.0 mm size inductor with L terminals from Mag Layers
R5		RES 9.1K OHM 1/8W 1% 0805 SMD
R9, R14, R16, R38		RES 1.00K OHM 1/8W 1% 0805 SMD
R15		RES 1.69K OHM 1/8W 1% 0805 SMD
R3, R24, R29, R30, R32, R37, R40, R41, R46, R49		0 OHM JUMPER 1/8W 0.125W 0805 THICK FILM CHIP RESISTOR
R1, R4		RES 49.9 OHM 1/8W 1% 0805 SMD
R19, R20, R22, R42, R43		RESISTOR ZERO OHM 1/10W 5% 0805 SMD
R10-R13		RES 13.3K OHM 1/10W 1% 0402 SM
R25, R44		RES 1.5K OHM 1/8W 0.1% 0805 SMD
R48		RES 511 OHM 1/16W 1% 0402 SMD
R36		RES 2.0K OHM 1/8W 0.1% 0805 SMD
R35		RES 20K OHM 1/10W 1% 0402 SMD
R34		RES 10K OHM 1/10W 1% 0402 SMD
R39		RES 590 OHM 1/8W 1% 0805 SMD
TP2, TP3, TP-TP10, TP12-TP17, TP22-TP24, TP26-TP28, TP30-TP34, TP38, TP39, TP42, TP43, TP52-TP57, TP61, TP62		TEST POINT SURFACE MOUNT
C1-C8, C24, C26, C28, C29, C31, C32, C36, C39, C43, C48, C49, C54, C56, C57, C59, J5, R2, R6-8, R17, R18, R21, R23, R26-R28, R31, R33, R45, R47, U5		COMPONENT NOT USED ** DO NOT INSTALL **
U1		ET4040 40A ADAPTIVE GATE DRIVING USING 7.5x5.5 46L DIE
U2		ED8101N00NQI QFN 24L (4MM x 4MM x 0.95MM)
U3, U4		EY1602SI-ADJ 40V Low Quiescent Current, 50mA Linear Regulator SOIC8 GTP

Typical Performance

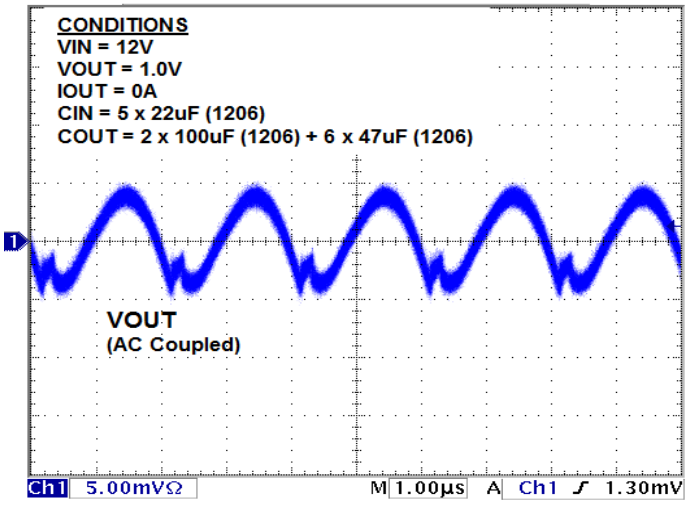
Efficiency vs. Output Current



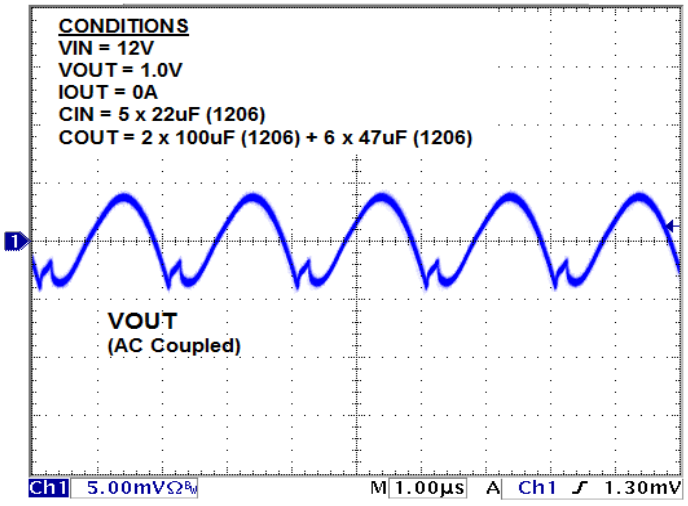
Power Loss vs. Output Current



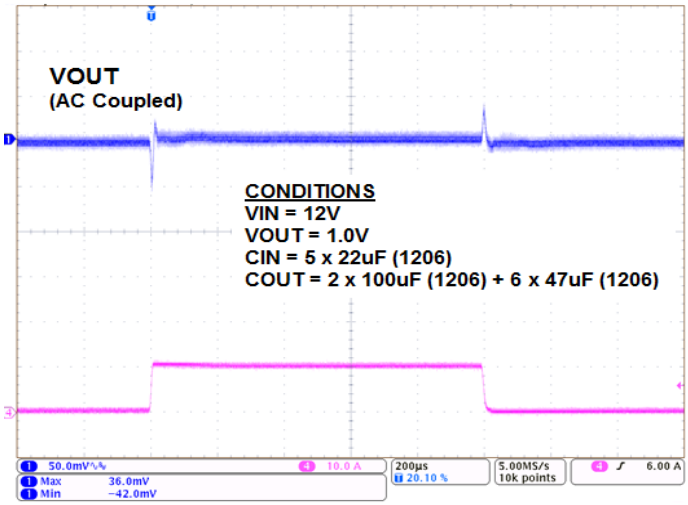
Output Ripple at 500 MHz



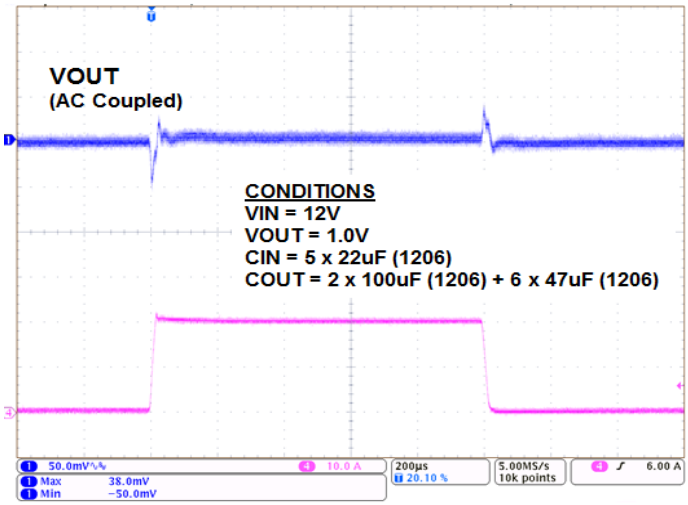
Output Ripple at 20 MHz



Load Transient from 0 to 10A



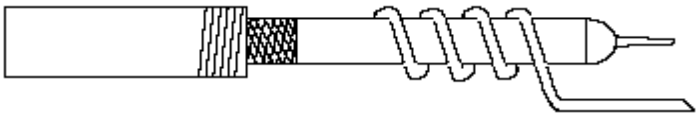
Load Transient from 0 to 20A



Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make output ripple, load regulation and load transient measurements across the load decoupling capacitor C34, this is the output voltage differential sensing point.
2. Measure input and output current with series ammeters or accurate shunt resistors. Measure input voltage at TP3 or TP27, measure output voltage at TP6 or TP24, this will eliminate voltage drop across the line and load cables that can produce false readings. This is especially important when measuring efficiency.
3. Use a low-loop-inductance scope probe tip similar to the one shown below to measure switching signals and input / output ripple to avoid noise coupling into the probe ground lead. For more accurate ripple measurement, please see Enpirion App Note regarding this subject.



4. The board includes a push-pull digital IO test point for the PGOOD signal and ready to monitor the power GOOD status at clip lead TP55.

Contact Information

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