TEXAS INSTRUMENTS

# TAS5000

## Digital Audio PWM Processor

# Data Manual

December 2000

Digital Audio

SLAS270

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# Contents

# List of Illustrations



# List of Tables

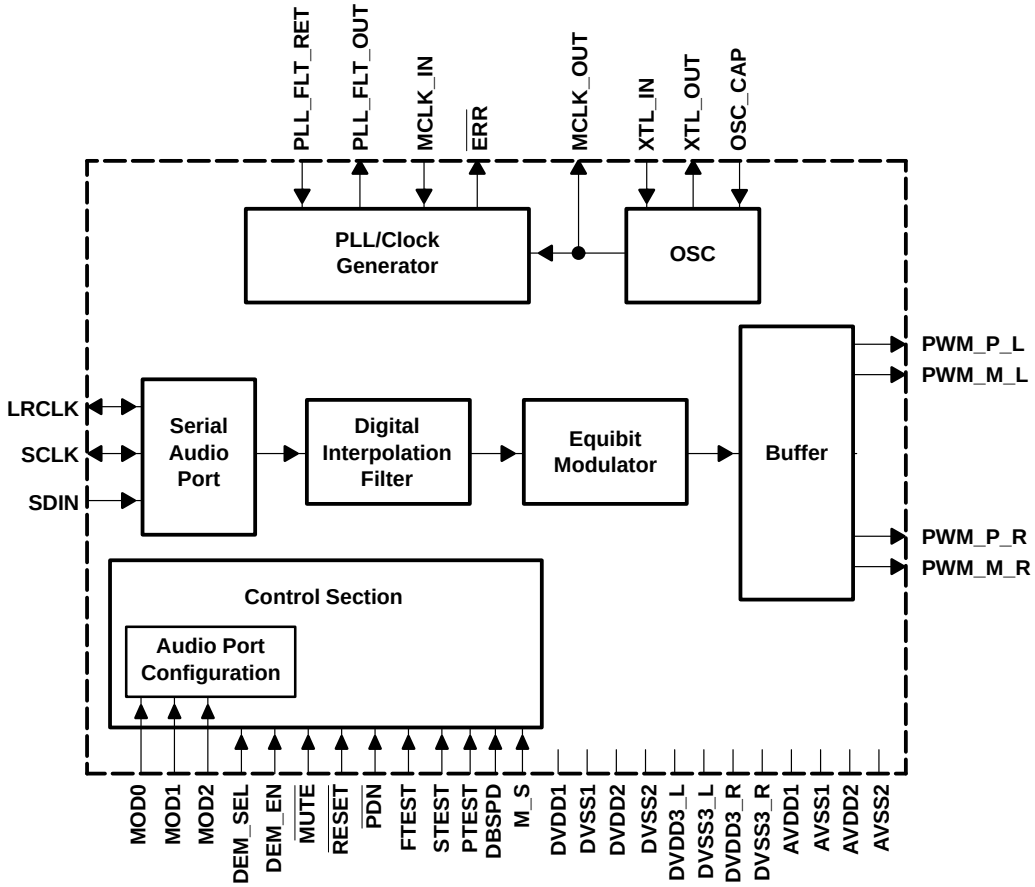
# 1 Introduction

The TAS5000 is an innovative, cost-effective, high-performance 24-bit stereo digital modulator based on Equibit™ technology. This product converts input PCM serial digital audio data to an output PWM audio data stream. The TAS5000 is designed to be connected to two TAS5100 mono true digital amplifiers for driving loudspeakers. This all-digital audio system contains only two analog components in the signal chain—an L-C low-pass filter at the speaker terminals. It can provide up to 90 dB SNR at the speaker terminals. It has a wide variety of serial input options including right justified (16, 20, or 24-bit), IIS (16, 20, or 24-bit), left justified (16-bit), or DSP (16-bit) data formats. It is fully compatible with AES standard sampling rates of 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz including providing de-emphasis for 44.1 kHz, and 48 kHz sample rates. The TAS5000 and TAS5100 system can be used in a range of products such as microcomponent systems, PC speakers, home theater in a box, convergence products, A/V receivers, or TV sets.

## 1.1 Features

- True Digital Audio Amplifier
- High Quality Audio
- 16-, 20-, or 24 Bit Input Data
- Sampling Rates: 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz
- Supports Master and Slave Modes
- 90 dB SNR (EIAJ) and Dynamic Range at the Speaker Terminals
- 3.3 V Power Supply Operation
- Economical 48-Pin TQFP Package
- Digital De-Emphasis: 44.1 kHz and 48 kHz
- High Power Efficiency
- Clock Oscillator Circuit for Master Modes
- Low Jitter Internal PLL
- Mute
- Good Phase Characteristics
- Excellent PSRR

## 1.2 Functional Block Diagram



## 1.3 Suggested System Block Diagrams

See application notes for more details.

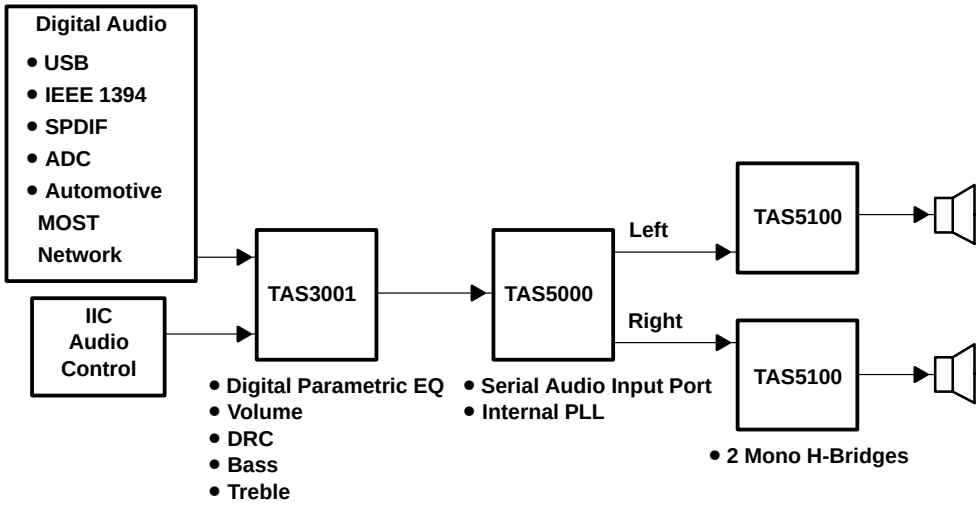



**Figure 1–1. System #1: Stereo Configuration Using Two TAS5100 Amplifiers**

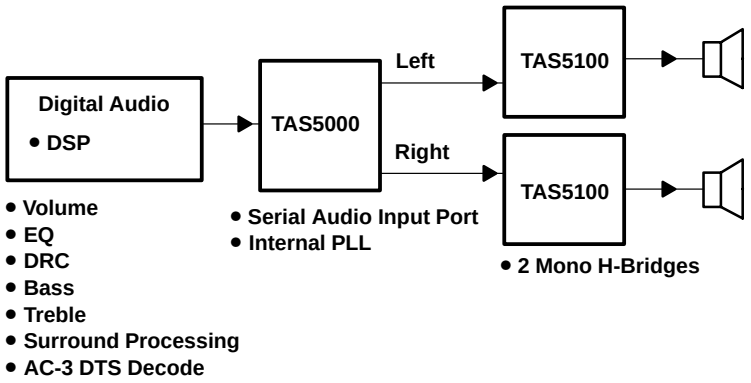



**Figure 1–2. System #2: Stereo Configuration With DSP**

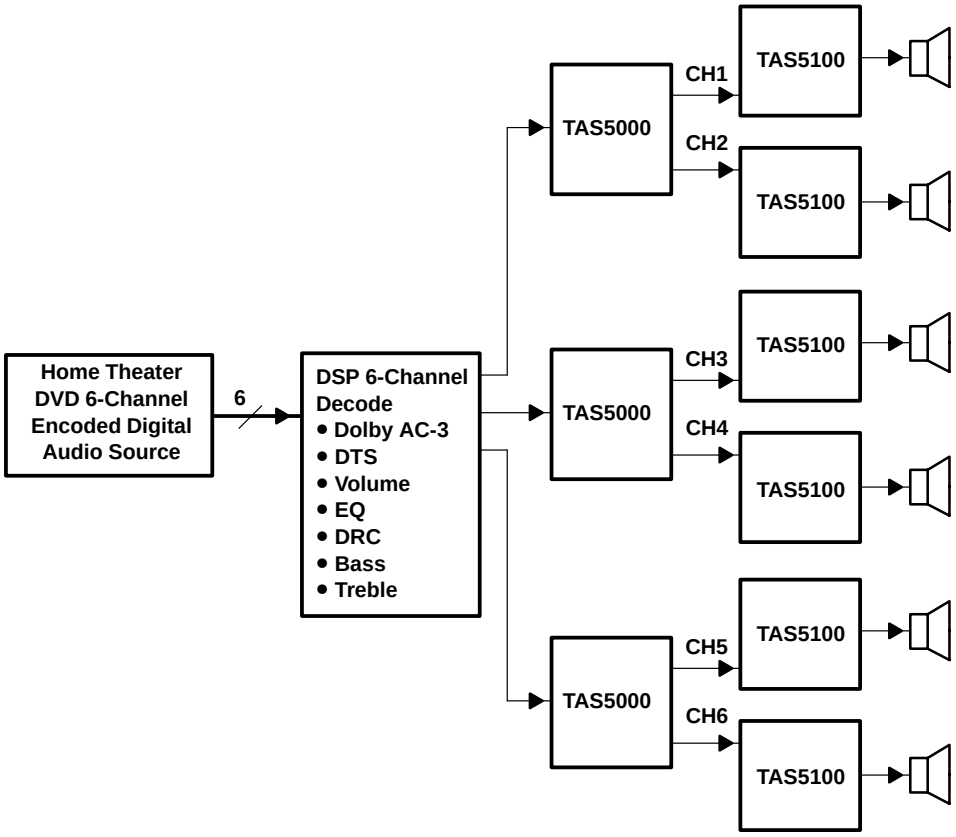
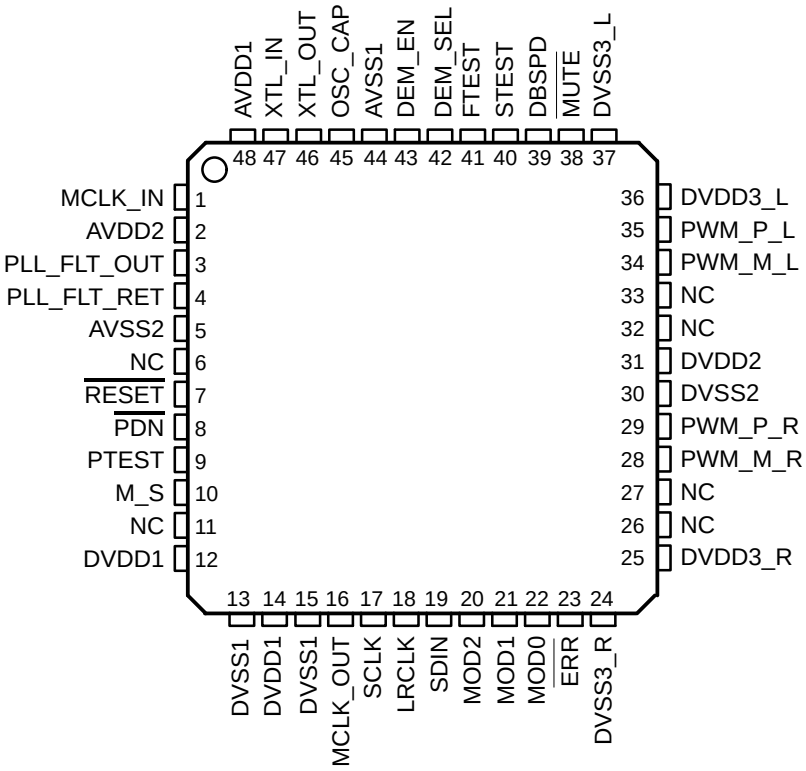



**Figure 1–3. System #3: 6-Channel Audio Playback**

## 1.4 Terminal Assignments

**48-Pin TQFP PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## 1.5 Ordering Information

| $T_A$ | PACKAGE |
|---|---|
| 0°C to 70°C | TAS5000PFB |

## 1.6 Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AVDD1 | 48 | I | Analog supply for oscillator |
| AVDD2 | 2 | I | Analog supply for PLL |
| AVSS1 | 44 | I | Analog ground for oscillator |
| AVSS2 | 5 | I | Analog ground for PLL |
| DBSPD | 39 | I | Indicates sample rate is double speed (88.2 kHz or 96 kHz), active high |
| DEM_EN | 43 | I | De-emphasis enable, active high |
| DEM_SEL | 42 | I | De-emphasis select (0 = 44.1 kHz, 1 = 48 kHz) |
| DVDD1 | 12, 14 | I | Digital voltage supply for logic |
| DVDD2 | 31 | I | Digital voltage supply for PWM reclocking |
| DVDD3_L | 36 | I | Digital voltage supply for PWM output (left) |
| DVDD3_R | 25 | I | Digital voltage supply for PWM output (right) |
| DVSS1 | 13, 15 | I | Digital ground for Logic |
| DVSS2 | 30 | I | Digital ground for PWM reclocking |
| DVSS3_L | 37 | I | Digital ground for PWM output (left) |
| DVSS3_R | 24 | I | Digital ground for PWM output (right) |
| $\overline{\text{ERR}}$ | 23 | O | System error flag, active low |
| FTEST | 41 | I | Tied to DVSS1 for normal operation |
| LRCLK | 18 | I/O | Left/right clock (input when M_S = 0; output when M_S = 1) |
| MCLK_IN | 1 | I | MCLK input |
| MCLK_OUT | 16 | O | Buffered system clock output if M_S = 1; otherwise set to 0 |
| MOD0 | 22 | I | Serial interface selection pin, bit 0 |
| MOD1 | 21 | I | Serial interface selection pin, bit 1 |
| MOD2 | 20 | I | Serial interface selection pin, bit 2 (MSB) |
| M_S | 10 | I | Master/slave, Master=1, Slave=0 |
| $\overline{\text{MUTE}}$ | 38 | I | Muted signal = 0, Normal mode = 1 |
| NC | 6, 11, 26, 27, 32, 33 | | No connection |
| OSC_CAP | 45 | I | Oscillator cap return |
| $\overline{\text{PDN}}$ | 8 | I | Power down, active low |
| PTEST | 9 | I | Tied to DVSS1 for normal operation |
| PLL_FLT_OUT | 3 | O | Output terminal for external PLL filter |
| PLL_FLT_RET | 4 | I | Return for external PLL filter |
| PWM_M_L | 34 | O | PWM left output (differential –) Positive H-bridge side |
| PWM_M_R | 28 | O | PWM right output (differential –) Positive H-bridge side |
| PWM_P_L | 35 | O | PWM left output (differential +) Positive H-bridge side |
| PWM_P_R | 29 | O | PWM right output (differential +) Positive H-bridge side |
| $\overline{\text{RESET}}$ | 7 | I | Reset (active low) |
| SCLK | 17 | I/O | Shift clock (input when M_S = 0, output when M_S = 1) |
| SDIN | 19 | I | Stereo serial audio data input |
| STEST | 40 | I | Tied to DVSS1 for normal operation |
| XTL_IN | 47 | I | Crystal or clock input (MCLK input) |
| XTL_OUT | 46 | O | Crystal output (not for external usage) NC when XTL_IN is MCLK input |

# 2 Functional Description

## 2.1 Serial Audio Port

The serial audio port consists of a shift clock (SCLK pin), a left/right frame synchronization clock (LRCLK pin), and a data input (SDIN pin). The serial audio port supports standard serial PCM formats (Fs = 44.1 kHz, 48 kHz, 88.2 kHz, or 96 kHz) stereo. See section 2.8 for Serial Interface Formats.

## 2.2 System Clocks – Master Mode and Slave Mode

The TAS5000 allows multiple system clocking schemes. In this document, master mode indicates that the TAS5000 provides system clocks to other parts of the system (M_S=1). Audio system clocks of frequency 256Fs MCLK_OUT, 64 Fs SCLK, and Fs LRCLK are output from this device when it is configured in master mode. Slave mode indicates that a system master other than the TAS5000 provides system clocks (LRCLK, SCLK, and MCLK_IN) to the TAS5000 (M_S = 0). The TAS5000 operates with LRCLK and SCLK synchronized to MCLK. TAS5000 does not require any specific phase relationship between LRCLK and MCLK, but there must be synchronization. If the synchronization between MCLK and LRCLK changes more than 10 MCLK periods during one sample period (LRCLK), the TAS5000 will initiate an internal reset. In the slave mode MCLK_OUT is driven low. Table 2–1 shows all the possible master and slave modes.

## 2.3 Oscillator/Sampling Frequency

The sampling frequency is determined by the crystal (master mode) or master clock in (slave mode) which should be either 11.2896 MHz (Fs = 44.1 kHz) or 12.288 MHz (Fs = 48 kHz). Twice the normal sampling frequency can be selected by using the DBSPD pin which allows usage of Fs = 88.2 kHz or Fs = 96 kHz. In the double-speed slave mode (DBSPD = 1, M_S = 0), the external clock input is either 22.5796 MHz (Fs = 88.2 kHz) or 24.576 MHz (Fs = 96 kHz). Table 2–1 explains the proper clock selection.

## 2.4 Phase Locked Loop (PLL)/Clock Generation

A low jitter PLL is incorporated for internal use. Connections for the PLL external loop filter are provided as PLL_FLT_RET and PLL_FLT_OUT. See Figure 5–1 for a suggested external loop filter. If the PLL loses lock, the error status pin ($\overline{\text{ERR}}$) will go low. Note that $\overline{\text{ERR}}$ can go low for other conditions as well. See section 2.7.7 Error Status Reporting.

**Table 2–1. Oscillator, External Clock, and PLL Functions**

| DESCRIPTION | M_S | DBSPD | XTL_IN (MHz)† | MCLK_IN (MHz)‡ | SCLK (MHz)¶ | LRCLK (kHz)¶ | MCLK_OUT (MHz)# |
|---|---|---|---|---|---|---|---|
| Master, normal speed | 1 | 0 | 11.2896 | — | 2.8224 | 44.1 | 11.2896 |
| Master, normal speed | 1 | 0 | 12.288 | — | 3.072 | 48 | 12.288 |
| Master, double speed | 1 | 1 | — | 22.5792§ | 5.6448 | 88.2 | 22.5792 |
| Master, double speed | 1 | 1 | — | 24.576§ | 6.144 | 96 | 24.576 |
| Slave, normal speed | 0 | 0 | — | 11.2896§ | 2.8224 | 44.1 | Digital GND |
| Slave, normal speed | 0 | 0 | — | 12.288§ | 3.072 | 48 | Digital GND |
| Slave, double speed | 0 | 1 | — | 22.5792§ | 5.6448 | 88.2 | Digital GND |
| Slave, double speed | 0 | 1 | — | 24.576§ | 6.144 | 96 | Digital GND |

† Either a crystal oscillator or an external clock of the specified frequency can be connected to XTL_IN.
‡ MCLK_IN tied low when input to XTL_IN is provided; XTL_IN tied low when MCLK_IN is provided.
§ External MCLK connected to MCLK_IN input
¶ SCLK and LRCLK are outputs when M_S=1, inputs when M_S=0.
# MCLK_OUT is driven low when M_S=0.

## 2.5 Digital Interpolation Filter

The 24-bit high performance linear phase FIR interpolation filter up-samples the input digital data at a rate of 4 times (double speed mode = 88.2 kHz or 96 kHz) or 8 times (normal mode = 44.1 kHz or 48 kHz) the incoming sample rate. This filter provides very low pass-band ripple and optimized time domain transient response for accurate music reproduction.

## 2.6 Digital PWM Modulator

The interpolation filter output is sent to the modulator. This modulator consists of a high performance 4$^{th}$ order digital noise shaper and a PCM to PWM converter. Following the noise shaper, the PCM signal is fed into a very low distortion PCM to PWM conversion block, buffered and output from the chip. The modulation scheme is based on a 2-state control of the H-bridge output.

## 2.7 Control, Status, and Operational Modes

The TAS5000 control section consists of several control-input pins. Three serial mode pins (MOD0, MOD1, and MOD2) are provided to select various serial data formats. During normal operating conditions if any of the MOD0, MOD1, or MOD2 pins changes state, a reset sequence is initiated (see paragraph 2.7.2). Also provided are separate power-down ($\overline{\text{PDN}}$), reset ($\overline{\text{RESET}}$), and mute ($\overline{\text{MUTE}}$) pins. The $\overline{\text{ERR}}$ pin indicates that an error has occurred.

### 2.7.1 Power Up

At power up the $\overline{\text{ERR}}$ pin is asserted low and the PWM outputs go to the hard mute state in which the P outputs are held low and the M outputs are held high. Following initialization, the TAS5000 will come up in the operational state. There are two cases of power-up timing. The first case is shown in Figure 2–1 with $\overline{\text{RESET}}$ preceding $\overline{\text{PDN}}$. The second case is shown in Figure 2–2 with $\overline{\text{PDN}}$ preceding $\overline{\text{RESET}}$.

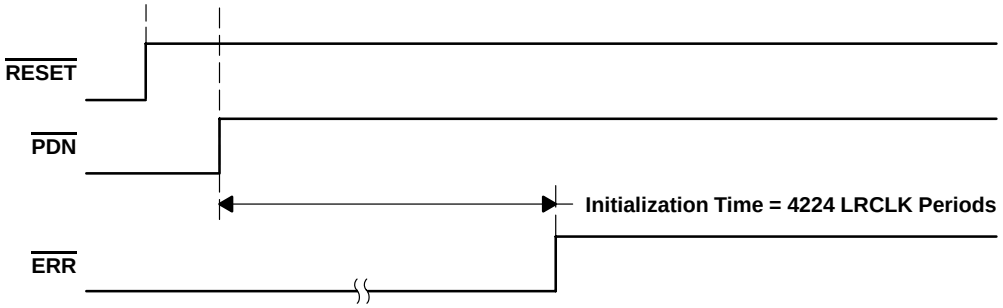



**Figure 2–1. Power-Up Timing ($\overline{\text{RESET}}$ preceding $\overline{\text{PDN}}$)**

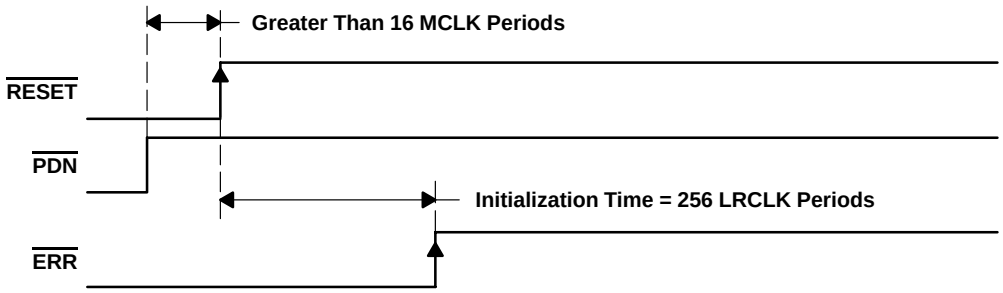



**Figure 2–2. Power-Up Timing ($\overline{\text{PDN}}$ preceding $\overline{\text{RESET}}$)**

### 2.7.2 Reset

The reset signal for the TAS5000 should be applied whenever toggling the M_S, DBSPD signal. This reset is asynchronous. See Figure 2–3 for reset timing. To initiate the reset sequence the $\overline{\text{RESET}}$ pin is asserted low. As long as the pin is held low the chip is in the reset state. During this reset time the PWM outputs are hard-muted (P-outputs held low and M-outputs held high) and the $\overline{\text{ERR}}$ status pin is held low. Assuming $\overline{\text{PDN}}$ is high, the rising edge of the reset pulse begins chip initialization. After 256 LRCLK periods the TAS5000 will begin normal operation.

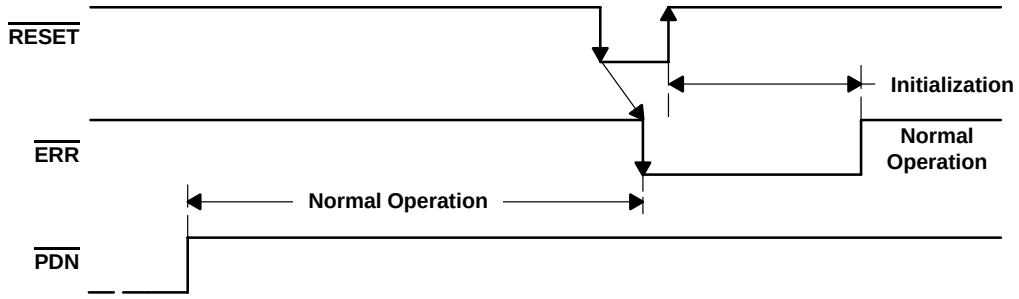



**Figure 2–3. Reset Timing**

### 2.7.3 Power Down

When $\overline{\text{PDN}}$ is low (see Figure 2–4. Power-Down Timing) both the PLL and the oscillator are shut down. Note that power down is an asynchronous operation. To place the device in total power-down mode, both $\overline{\text{RESET}}$ and $\overline{\text{PDN}}$ must be held low. As long as these pins are held low, the chip is in the power-down state and the PWM outputs are hard muted with the P outputs held low and the M outputs held high. To place the device back into normal mode, see section 2.7.1 for power-up timing.

**NOTE:** In order for the dynamic logic to be properly powered down, the clocks should not be stopped before the $\overline{\text{PDN}}$ pin goes low. Otherwise, the device may drain additional supply current.

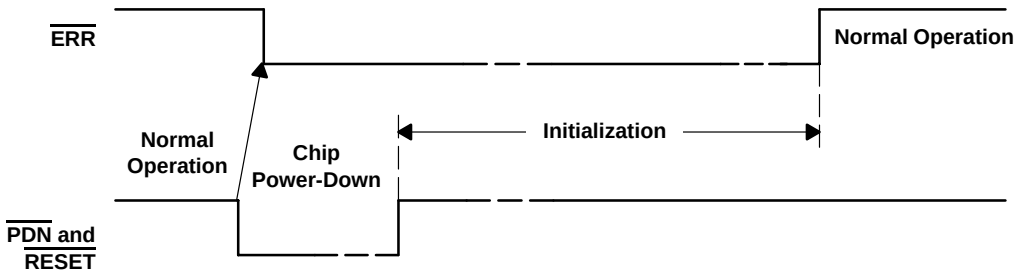



**Figure 2–4. Power-Down Timing**

### 2.7.4 Mute

The TAS5000 provides a mute function that is used when the $\overline{\text{MUTE}}$ pin is asserted low. See Table 2–2 for Mute Description. This mute is a quiet mute; that is, the mute is accomplished by outputting a zero value waveform in which both sides of the differential PWM outputs have a 50% duty cycle.

**Table 2–2. Mute Description**

| $\overline{\text{MUTE}}$ | PWM_P | PWM_M | DESCRIPTION |
|---|---|---|---|
| 0 | 50% Duty cycle | 50% Duty cycle | Mute |
| 1 | DATA | $\overline{\text{DATA}}$ | Normal operation |

### 2.7.5 Double Speed

Double-speed mode is used to support sampling rates of 88.2 kHz and 96 kHz. In order to put the TAS5000 in double-speed mode with the device in normal operating conditions, the $\overline{\text{RESET}}$ pin must be held low while switching the DBSPD pin high. After $\overline{\text{RESET}}$ pin is brought high again, a reset sequence takes place (see paragraph 2.7.2). If the change is at power up, a power up sequence is originated (see paragraph 2.7.1).

### 2.7.6 De-Emphasis Filter

For audio sources that have been pre-emphasized, a precision 50 μs/15 μs de-emphasis filter is provided to support the sampling rates of 44.1 kHz and 48 kHz. Pins DEM_SEL and DEM_EN select the de-emphasis functions. See Figure 2–5 for a graph showing the de-emphasis filtering characteristics. See Table 2–3 for de-emphasis selection.

When the DEM_EN pin or the DEM_SEL pin change state, the PWM outputs go into the quiet mute state. After 128 LRCLK periods for initialization, the PWM outputs are driven to the normal (unmuted) mode.

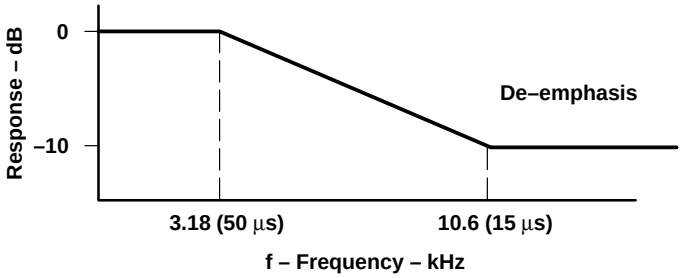



**Figure 2–5. De-Emphasis Filter Characteristics**

#### 2.7.6.1 De-Emphasis Selection

De-emphasis selection is accomplished by using the DEM_SEL and DEM_EN pins. See Table 2–3 for de-emphasis selection description.

**Table 2–3. De-Emphasis Selection**

| DEM_SEL | DEM_EN | DESCRIPTION |
|---|---|---|
| X | 0 | De-emphasis disabled |
| 0 | 1 | De-emphasis enabled for Fs = 44.1 kHz |
| 1 | 1 | De-emphasis enabled for Fs = 48 kHz |

### 2.7.7 Error Status Reporting ($\overline{\text{ERR}}$ pin)

The following is a list of the error conditions that will cause the $\overline{\text{ERR}}$ status pin to be asserted low:

- No clocks
- Clock phase errors

When any of the above conditions is met, the $\overline{\text{ERR}}$ will go low and the PWM outputs will go to the hard mute state. If the error condition is removed, the TAS5000 is reinitialized and the $\overline{\text{ERR}}$ pin will be asserted high.

## 2.8 Serial Interface Formats

The TAS5000 is compatible with eight different serial interfaces. Available interface options are IIS, right justified, left justified, and DSP Frame. Table 2–4 indicates how these options are selected using the MOD0, MOD1, and MOD2 pins.

**Table 2–4. Hardware Selection of Serial Audio Modes**

| MODE | MOD2 PIN | MOD1 PIN | MOD0 PIN | SERIAL INTERFACE SDIN |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 16 bit, MSB first; right justified |
| 1 | 0 | 0 | 1 | 20 bit, MSB first; right justified |
| 2 | 0 | 1 | 0 | 24 bit, MSB first; right justified |
| 3 | 0 | 1 | 1 | 16 bit IIS |
| 4 | 1 | 0 | 0 | 20 bit IIS |
| 5 | 1 | 0 | 1 | 24 bit IIS |
| 6 | 1 | 1 | 0 | 16 bit MSB first, left justified |
| 7 | 1 | 1 | 1 | 16 bit DSP frame |

The following figures illustrate the relationship between the SCLK, LRCLK and the serial data I/O for the different interface protocols. Note that there are always 64 SCLKs per LRCLK. The nondata bits are padded with binary 0.

### 2.8.1 MSB First Right Justified (for 16-, 20-, 24-bits)

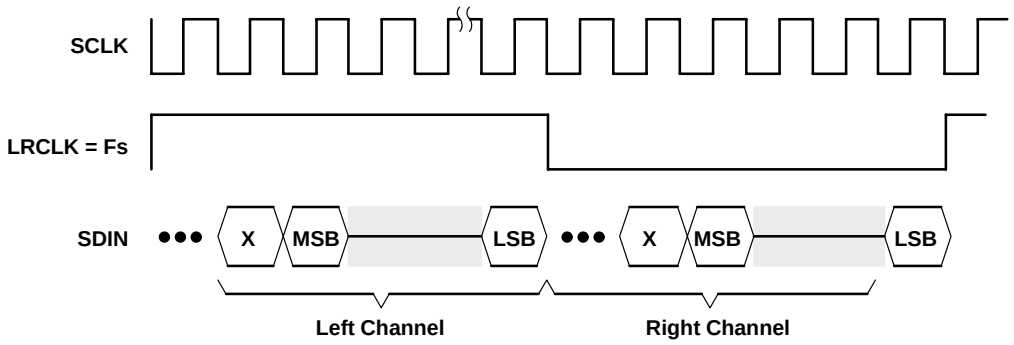



**Figure 2–6. MSB First Right Justified**

Note the following characteristics of this protocol.

- Left channel is received when LRCLK is high.
- Right channel is received when LRCLK is low.
- The SDIN data is justified to the trailing edge of the LRCLK
- SDIN is sampled at the rising edge of SCLK.
- If LRCLK phase changes by more than 10 MCLKs, then the chip automatically resets.

### 2.8.2 IIS Compatible Serial Format ( for 16-, 20-, 24-bits)

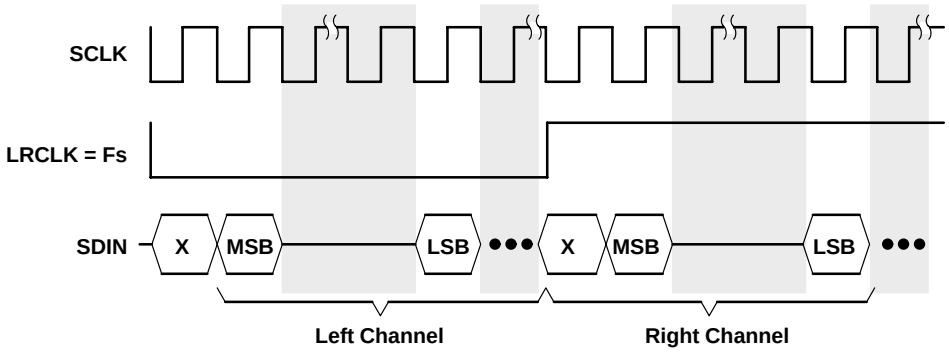



**Figure 2–7. IIS Compatible Serial Format**

Note the following characteristics of this protocol.

- Left channel is received when LRCLK is low.
- Right channel is received when LRCLK is high.
- SDIN is sampled with the rising edge of SCLK.

### 2.8.3 MSB Left Justified Serial Interface Format (for 16 bits)

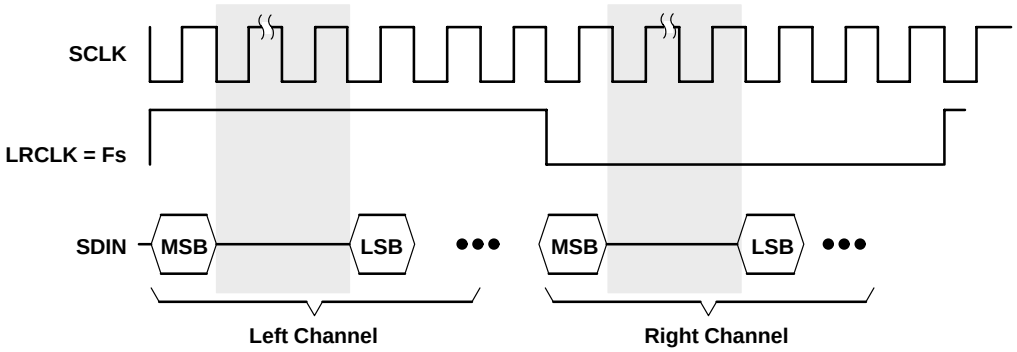



**Figure 2–8. MSB Left Justified Serial Interface Format**

Note the following characteristics of this protocol.

- Left channel is received when LRCLK is high.
- Right channel is received when LRCLK is low.
- The SDIN data is justified to the leading edge of the LRCLK.
- SDIN is sampled with the rising edge of SCLK.

### 2.8.4 DSP Compatible Serial Interface Format (for 16 bits)

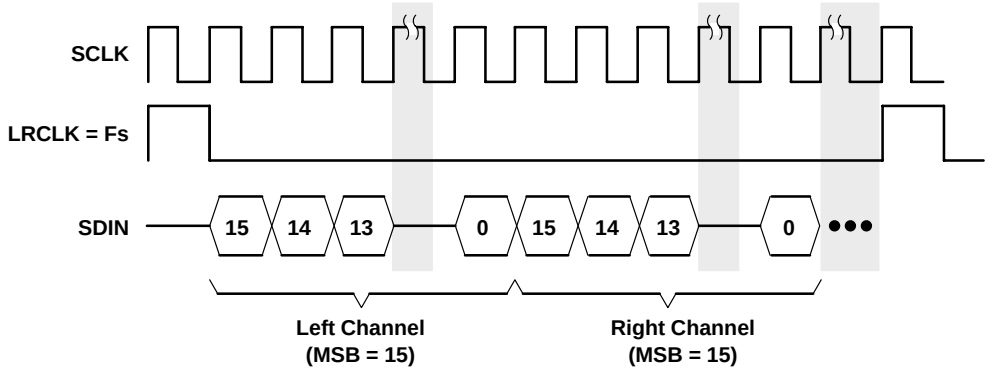



**Figure 2–9. DSP Compatible Serial Interface Format**

Note the following characteristics of this protocol.

- Serial data is sampled with the falling edge of SCLK.

## 2.9 PWM Outputs

Designed to be used with TAS5100.

# 3 Electrical Specifications

## 3.1 Absolute Maximum Ratings†

Analog supply voltage range, $AV_{DD1}$, $AV_{DD2}$) . . . . . –0.3 V to 4.2 V
Digital power supply voltage, $DV_{DD1}$, $DV_{DD2}$, $DV_{DD3\_L}$, $DV_{DD3\_R}$ . . . . . –0.3 V to 4.2 V
Digital input voltage, $V_I$ (see Note 1) . . . . . –0.3 V to $DV_{DDX}$+0.3 V
Operating free-air temperature, $T_A$ . . . . . 0°C to 70°C
Storage temperature, $T_{stg}$ . . . . . –65°C to 150°C
ESD . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. DVDD1, DVDD2, DVDD3_L, DVDD3_R

## 3.2 Recommended Operating Conditions

($T_A$ = 25°C; $DV_{DD1}$ = $DV_{DD2}$ = $DV_{DD3\_L}$ = $DV_{DD3\_R}$ = 3.3 V ±10%, $AV_{DD1}$ = $AV_{DD2}$ = 3.3 V ±10%, Fs = 44.1 kHz)
Voltages at analog inputs and outputs are with respect to ground

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage | Digital | DVDDX‡ | 3 | 3.3 | 3.6 | V |
| Supply current | Digital | Operating | | 18 | | mA |
| | | Power down§ | | 2 | 20 | µA |
| Power dissipation | Digital | Operating | | 59.4 | | mW |
| | | Power down§ | | 6.6 | 72 | µW |
| Supply voltage | Analog | AVDDX¶ | 3 | 3.3 | 3.6 | V |
| Supply current | Analog | Operating | | 8 | | mA |
| | | Power down§ | | 10 | 100 | µA |
| Power dissipation | Analog | Operating | | 26.4 | | mW |
| | | Power down§ | | 33 | 360 | µW |

‡ DVDD1, DVDD2, DVDD3_L, DVDD3_R
§ If the clocks are turned off
¶ AVDD1, AVDD2

## 3.3 Electrical Characteristics

### 3.3.1 Static Digital Specifications

($T_A$ = 25°C; $DV_{DD1}$ = $DV_{DD2}$ = $DV_{DD3\_L}$ = $DV_{DD3\_R}$ = 3.3 V ±10%, $AV_{DD1}$ = $AV_{DD2}$ = 3.3 V ±10%)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | 2 | DVDD1 | V |
| $V_{IL}$ | Low-level input voltage | 0 | 0.8 | V |
| $V_{OH}$ | High-level output voltage, ($I_O$ = –1 mA) | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage, ($I_O$ = 4 mA) | | 0.4 | V |
| | Input leakage current | –10 | 10 | µA |

### 3.3.2 Digital Interpolation Filter and PWM Modulator

($T_A$ = 25°C; $DV_{DD1}$ = $DV_{DD2}$ = $DV_{DD3\_L}$ = $DV_{DD3\_R}$ = 3.3 V ±10%, $AV_{DD1}$ = $AV_{DD2}$ = 3.3 V ±10%, Fs = 44.1 kHz)
All the terms characterized by frequency will scale with the normal mode sampling frequency, Fs.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Pass band | 0 | | 20 | kHz |
| Pass band ripple | | ±0.012 | | dB |
| Stop band | | 24.1 | | kHz |
| Stop band attenuation (24.1 kHz to 152.3 kHz) | 50 | | | dB |
| Group delay | | 700 | | µS |
| PWM modulation index (gain) | | 0.93 | | |

### 3.3.3 TAS5000/TAS5100 System Performance Measured at the Speaker Terminals

Reference section 4.4 in the TAS5100 Data Manual

## 3.4 Switching Characteristics

### 3.4.1 Serial Audio Ports Slave Mode

($T_A$ = 25°C, $DV_{DD1}$ = $DV_{DD2}$ = $DV_{DD3\_L}$ = $DV_{DD3\_R}$ = $AV_{DD1}$ = $AV_{DD2}$ = 3.3 V ±10%)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| f(SCLK) | SCLK frequency | | | 6.144 | MHz |
| $t_{su}$(SDIN) | SDIN setup time before SCLK rising edge | 20 | | | ns |
| $t_h$(SDIN) | SDIN hold time from SCLK rising edge | 10 | | | ns |
| F(LRCLK) | LRCLK frequency | 44.1 | 48 | 96 | kHz |
| | MCLK duty cycle | | 50% | | |
| | SCLK duty cycle | | 50% | | |
| | LRCLK duty cycle | | 50% | | |
| $t_{su}$(LRCLK) | LRCLK edge setup before SCLK rising edge | 20 | | | ns |

### 3.4.2 Serial Audio Ports Master Mode

Load conditions: 50pF

($T_A$ = 25°C, $DV_{DD1}$ = $DV_{DD2}$ = $DV_{DD3\_L}$ = $DV_{DD3\_R}$ = $AV_{DD1}$ = $AV_{DD2}$ = 3.3 V ±10%)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{(MSD)}$ | MCLK to SCLK | 0 | | 5 | ns |
| $t_{(MLRD)}$ | MLCK to LRCLK | 0 | | 5 | ns |
| | SCLK, LRCLK duty cycle | | 50% | | |

### 3.4.3 DSP Serial Interface Mode

($T_A$ = 25°C, $DV_{DD1}$ = $DV_{DD2}$ = $DV_{DD3\_L}$ = $DV_{DD3\_R}$ = $AV_{DD1}$ = $AV_{DD2}$ = 3.3 V ±10%)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| f(SCLK) | SCLK frequency | | | 6.144 | MHz |
| $t_W$(FSHIGH) | Pulse duration, sync | | 1/(64×$f_S$) | | ns |
| $t_{su}$(SDIN), $t_{su}$(LRCLK) | SDIN and LRCLK setup time before SCLK falling edge | 20 | | | ns |
| $t_h$(SDIN), $t_h$(LRCLK) | SDIN and LRCLK hold time from SCLK falling edge | 10 | | | ns |
| | SCLK duty cycle | | 50% | | |

# 4 Parameter Measurement Information

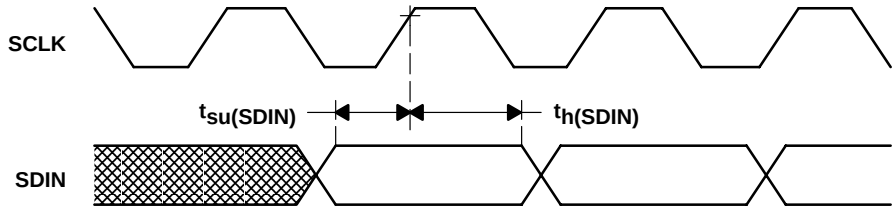
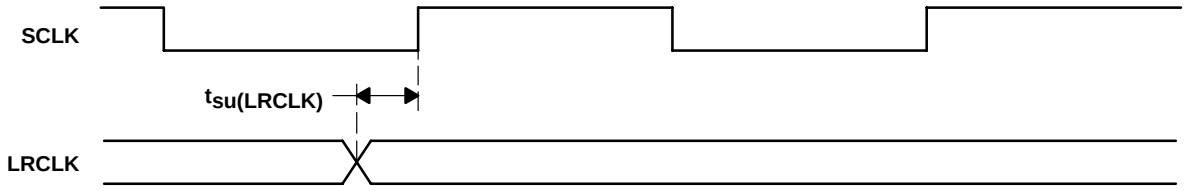



**Figure 4–1. Right Justified, IIS, Left Justified Serial Protocol Timing**




NOTE: Serial data is sampled with the rising edge of SCLK (setup time = 20 ns and hold time = 10 ns)

**Figure 4–2. Right, Left, and IIS Serial Mode Timing Requirement**

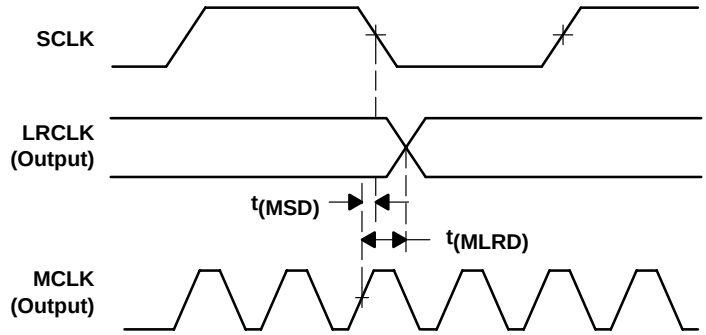



**Figure 4–3. Serial Audio Ports Master Mode Timing**

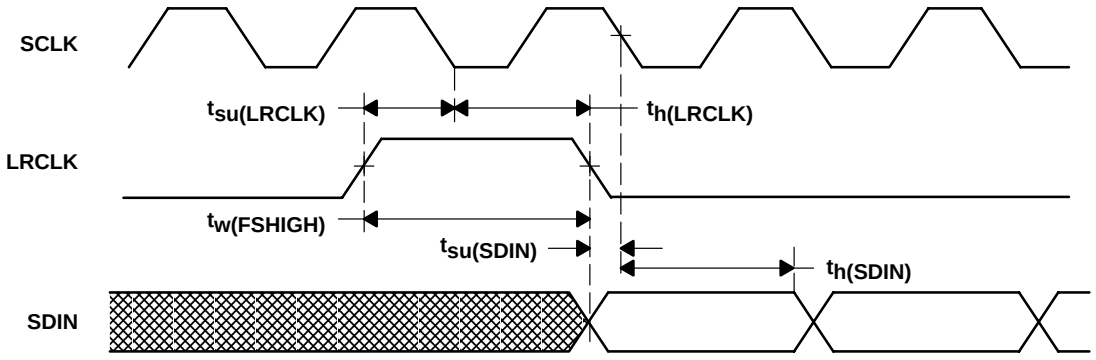



**Figure 4–4. DSP Serial Port Timing**

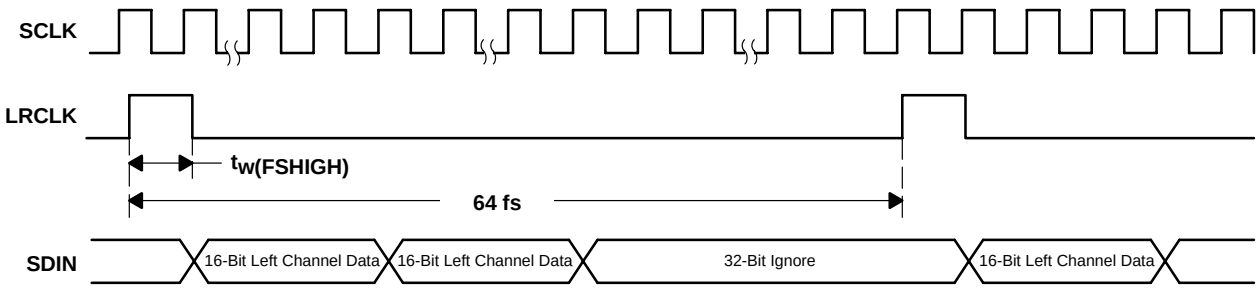
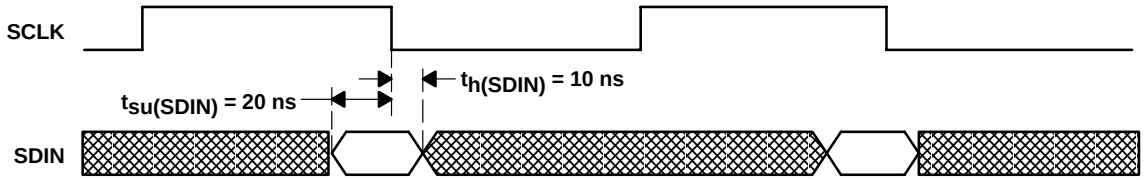


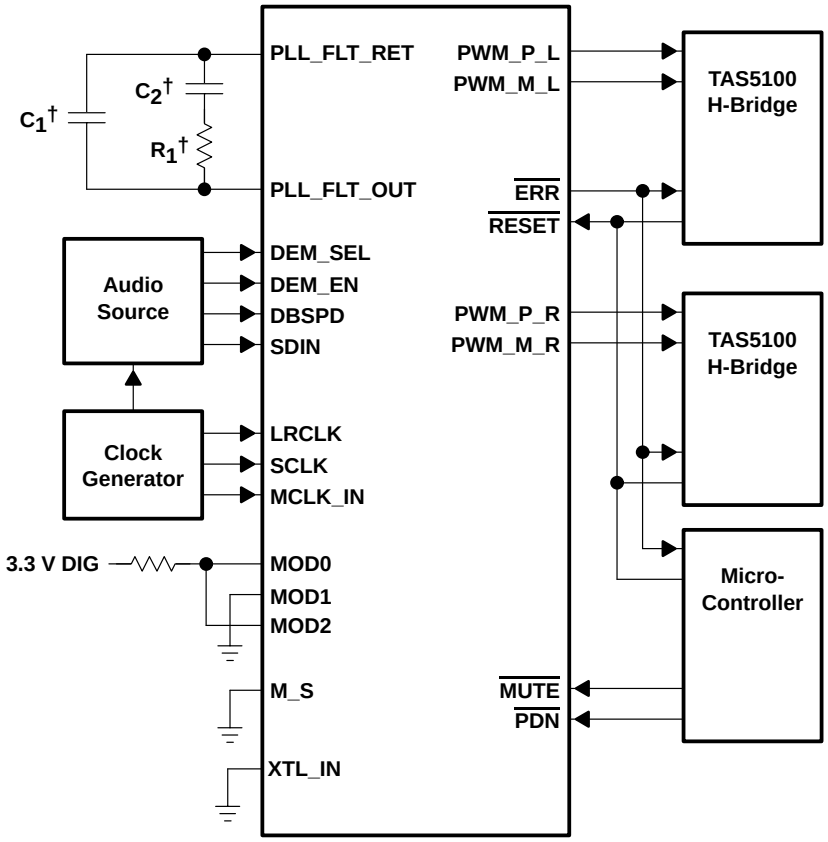

**Figure 4–5. DSP Serial Port Expanded Timing**




NOTE: Serial data is sampled with the falling edge of SCLK (setup time = 20 ns and hold time = 10 ns)

**Figure 4–6. DSP Absolute Timing Requirement**

# 5 Application Information




† See application note for values

**Figure 5–1. Connection Diagram, Slave Mode (typical)**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| TAS5000PFB | NRND | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TAS5000PFBG4 | NRND | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.