



HYB18RL25632AC

HYB18RL25616AC

## Graphics & Speciality DRAMs

256 Mbit DDR Reduced Latency DRAM

Version 1.42

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# HYB18RL25616/32AC

## 256 Mbit DDR Reduced Latency DRAM



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HYB18RL25616/32AC		
Revision History: Current Version 1.42		
		Subjects (major changes since last revision)
Previous Version: 1.34		
		New formatting of the specification document
	16	Elimination of 4mA Driver Strength in MRS
	17	Elimination of Configurations 5 and 6 in Configuration Table.
	23	tCKDQS (max) changed to 3.7ns for all speed sorts tCKDQS (min) changed from 2.3ns to 2.7ns for all speed sorts
	25, 26	Introduction of "Read followed by Write, Write data on bus prior to Read data" timings.
	35	Reference Voltage range changed to 0.49 * VDDQ to 0.51 * VDDQ AC Operation : HSTL strong : VIH and VIL changed to Vref +/- 0.3V
Previous Version: 1.4		
	15	Power up sequence modified: Addresses may be applied with specified setup and hold timings during MRS commands.
Previous Version: 1.41		
22,23	22,23	tDQSQ changed back to tQSQ (typo)
22	22	Data Window = min(tDQSH, tDQSL) - 2 * tQSQmax
23	23	Note 4 : tQSQ and tQSQHZ are absolute values

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## **1 Overview**

### **1.1 Features**

- 256 Megabit (256M)
- 0.17µm process technology
- Cyclic bank addressing for maximum data out bandwidth
- Organization 8M x 32, 16M x 16 in 8 banks
- Non-multiplexed addresses
- Non-interruptible sequential bursts of 2 (2-bit prefetch) and 4 (4-bit prefetch), DDR
- Up to 600Mb/sec/pin data rate
- Programmable Read Latency (RL) of 5..6
- Data valid signal (DVLD) activated as Read Data is available
- Data Mask signals (DM0 / DM1) to mask first and second part of write data burst
- IEEE 1149.1 compliant JTAG Boundary Scan
- Pseudo-HSTL 1.8V IO Supply
- Internal autoprecharge
- Refresh requirements: 32ms at 100°C junction temperature (8k refresh for each bank, 64k refresh commands must be issued in total each 32ms)
- Package T-FBGA 144
- 2.5V V<sub>EXT</sub>, 1.8V V<sub>DD</sub>, 1.8V V<sub>DDQ</sub>

**Table 1 Key timing parameters (Configuration Example x32, x16 device)**

Speed Sort	-3.3	-4.0	-5.0	Units
Frequency	300	250	200	MHz
t <sub>RC</sub>	26.7	28.0	25.0	ns
	8	7	5	cycles
Read latency	6	5	5	cyles

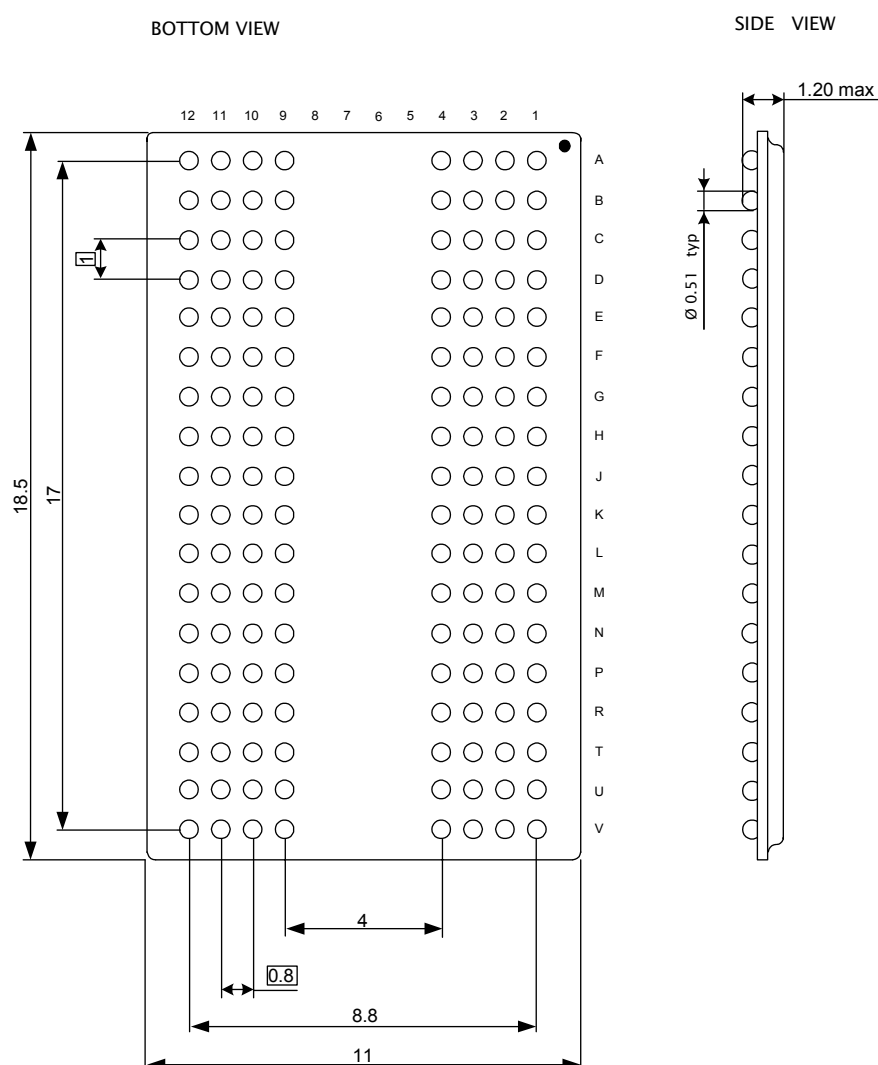
## 1.2 General Description

The Infineon 256M Reduced Latency DRAM (RLDRAM) contains 8 banks x 32 Mb of memory accessible with 32bit or 16bit I/O's in a double data rate (DDR) format where the data is provided and synchronized with a differential echo clock signal. RLDRAM does not require row/column address multiplexing and is optimized for fast random access and high data bandwidth.

RLDRAM is designed for communication data storages like transmit or receive buffers in telecommunication systems as well as data or instruction cache applications requiring large amounts of memory.

## 1.3 Ball Configuration Package and Ballout

**Figure 1 T-FBGA 144 package 256 Mbit DDR Reduced Latency DRAM**



*Note: All dimensions in mm*

Figure 2 Ballout of 256 Mbit Reduced Latency DRAM (x32 configuration)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	VEXT	VREF	VSS					VSS	VEXT	TMS	TCK
B	VSS	DQ8	DQ9	VSSQ					VSSQ	DQ1	DQ0	VSS
C	VSS	DQ10	DQ11	VDDQ					VDDQ	DQ3	DQ2	VSS
D	VSS	DQS1	DQS1#	VSSQ					VSSQ	DQS0#	DQS0	VSS
E	VSS	DQ12	DQ13	VDDQ					VDDQ	DQ5	DQ4	VSS
F	DM0	DQ14	DQ15	VSSQ					VSSQ	DQ7	DQ6	DVLD
G	A5	A6	A7	VDD					VDD	A2	A1	A0
H	A8	A9	VSS	VSS					VSS	VSS	A4	A3
J	AS#	BA2	VDD	VDD					VDD	VDD	BA0	CK
K	WE#	REF#	VDD	VDD					VDD	VDD	BA1	CK#
L	A18	CS#	VSS	VSS					VSS	VSS	A14	A13
M	A15	A16	A17	VDD					VDD	A12	A11	A10
N	DM1	DQ22	DQ23	VSSQ					VSSQ	DQ31	DQ30	NC
P	VSS	DQ20	DQ21	VDDQ					VDDQ	DQ29	DQ28	VSS
R	VSS	DQS2	DQS2#	VSSQ					VSSQ	DQS3#	DQS3	VSS
T	VSS	DQ18	DQ19	VDDQ					VDDQ	DQ27	DQ26	VSS
U	VSS	DQ16	DQ17	VSSQ					VSSQ	DQ25	DQ24	VSS
V	VSS	VEXT	VREF	VSS					VSS	VEXT	TDO	TDI

Figure 3 Ballout of 256Mbit Reduced Latency DRAM (x16 configuration)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	VEXT	VREF	VSS					VSS	VEXT	TMS	TCK
B	VSS	NC	NC	VSSQ					VSSQ	DQ1	DQ0	VSS
C	VSS	NC	NC	VDDQ					VDDQ	DQ3	DQ2	VSS
D	VSS	NC	NC	VSSQ					VSSQ	DQS0#	DQS0	VSS
E	VSS	NC	NC	VDDQ					VDDQ	DQ5	DQ4	VSS
F	DM0	NC	NC	VSSQ					VSSQ	DQ7	DQ6	DVLD
G	A5	A6	A7	VDD					VDD	A2	A1	A0
H	A8	A9	VSS	VSS					VSS	VSS	A4	A3
J	AS#	BA2	VDD	VDD					VDD	VDD	BA0	CK
K	WE#	REF#	VDD	VDD					VDD	VDD	BA1	CK#
L	A19	CS#	VSS	VSS					VSS	VSS	A14	A13
M	A15	A16	A17	VDD					VDD	A12	A11	A10
N	DM1	NC	NC	VSSQ					VSSQ	DQ15	DQ14	A18
P	VSS	NC	NC	VDDQ					VDDQ	DQ13	DQ12	VSS
R	VSS	NC	NC	VSSQ					VSSQ	DQS1#	DQS1	VSS
T	VSS	NC	NC	VDDQ					VDDQ	DQ11	DQ10	VSS
U	VSS	NC	NC	VSSQ					VSSQ	DQ9	DQ8	VSS
V	VSS	VEXT	VREF	VSS					VSS	VEXT	TDO	TDI

Note: NC : No Connect : These signals are internally connected and have parasitic characteristics of an IO. They may optionally be connected to ground for improved heat dissipation.



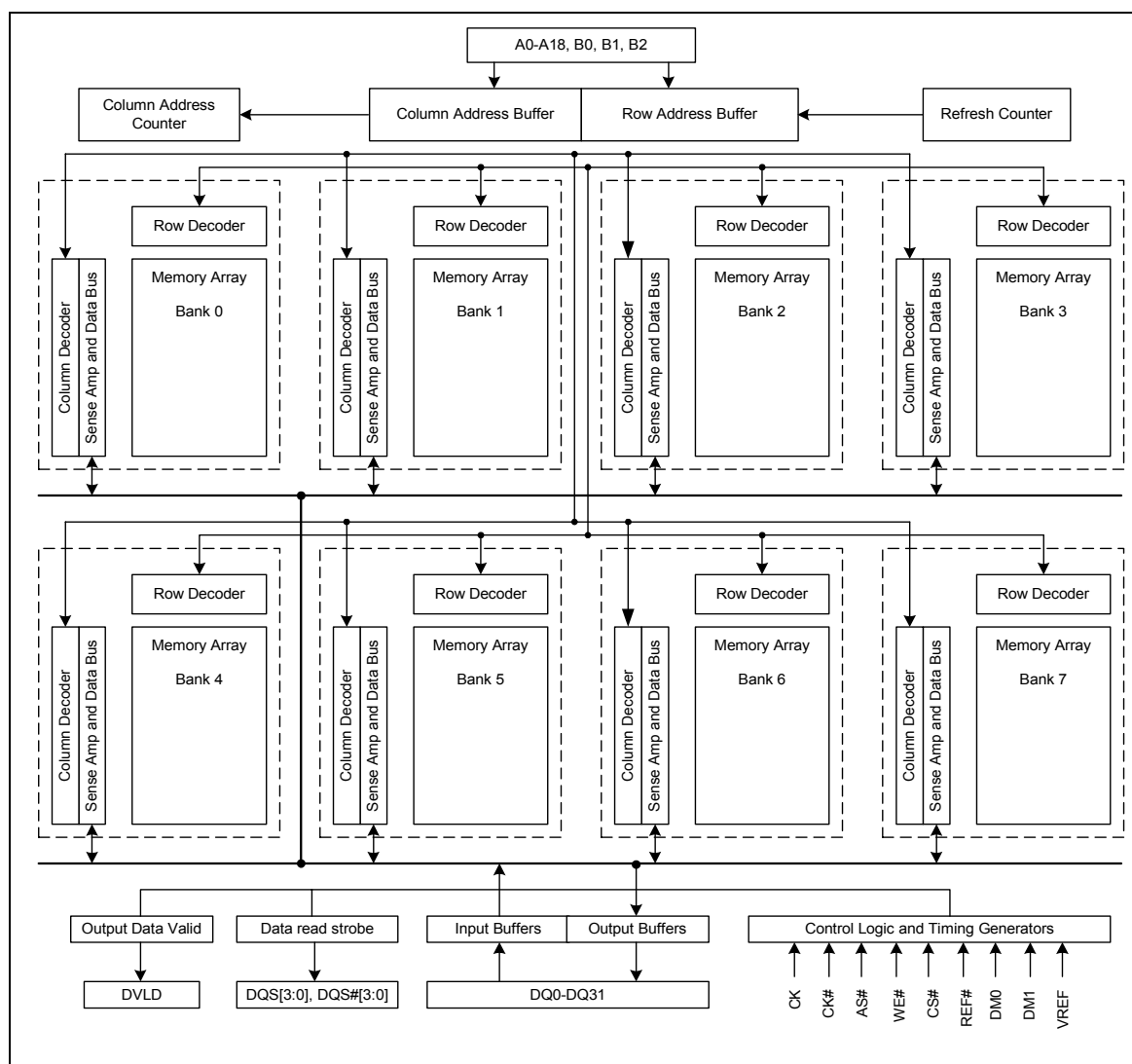
### 1.3.1 Ball Description

**Table 2 Ball description**

Ball	Type	Detailed Function
CK, CK#	Input	Input Clock: CK and CK# are differential clock inputs. Addresses and commands are latched on the rising edge of CK, input data is latched on the both edges of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	Chip Select: CS# enables the command decoder when low and disables it when high. When the command decoder is disabled new commands are ignored, but internal operations continue.
AS#, WE#, REF#	Input	Command Inputs: Sampled at the positive edge of CK. AS#, WE# and REF# define (together with CS#) the command to be executed.
A[19:0]	Input	Address Inputs: A[19:0] define the row and column addresses for READ and WRITE operations. During an MODE REGISTER SET the address inputs A[17:0] define the register settings. The addresses are sampled at the rising edge of CK. In the x32 configuration, A[19] is not used. In the x16 configuration with BL2, A[19] is used.
BA[0:2]	Input	Bank select: Select to which internal bank a command is being applied.
DQ[31:0]	Input/Output	Data Input / Output: The DQ signals form the 32 bit data bus. During READ commands the data is referenced to both edges of DQS/DQS#. During WRITE commands the data is sampled at both edges of CK.
DQSx, DQSx#	Output	Data read strobes : DQSx and DQSx# are the differential data read strobes. During READs, they are transmitted by the RLDRAM and edge-aligned with data. DQSx is ideally 180 degrees out of phase with DQSx#. DQS0, DQS0# are aligned with DQ0-DQ7. DQS1, DQS1# are aligned with DQ8-DQ15. DQS2, DQS2# are aligned with DQ16-DQ23. DQS3, DQS3# are aligned with DQ24-DQ31.
DVLD	Output	Data Valid: The DVLD indicates valid output data. DVLD is edge-aligned with DQSx, DQSx#.
DM0, DM1	Input	Data Mask: DM0 and DM1 are the input masks for WRITE data. The first half of the Input data burst is masked when DM0 is sampled HIGH along with the WRITE command. The second half of the input data burst is masked when DM1 is sampled HIGH along with the WRITE command.
TCK	Input	IEEE 1149.1 Clock Input: JEDEC standard 1.8V IO levels. These pin must be tied to VSS if the JTAG function is not used in the circuit.
TMS, TDI	Input	IEEE 1149.1 Test Inputs: JEDEC standard 1.8V IO levels. These pins may be left not connected if the JTAG function is not used in the circuit.
TDO	Output	IEEE 1149.1 Test Output: JEDEC standard 1.8V IO level tracking VDDQ.
VREF	Supply	Input Reference Voltage: Nominally VDDQ/2. Provides a reference voltage for the input buffers.
VEXT	Supply	Power Supply: 2.5V nominal. See DC Electrical Characteristics and Operating Conditions for range.
VDD	Supply	Power Supply: 1.8V nominal. See DC Electrical Characteristics and Operating Conditions for range.
VDDQ	Supply	Power Supply: Isolated Output Buffer Supply. 1.8V nominal. See DC Electrical Characteristics and Operating Conditions for range.
VSS	Supply	Power Supply: GND
VSSQ	Supply	Power Supply: Isolated Output Buffer Supply. GND
NC	-	No Connect : These pins may be connected to ground to improve heat dissipation.

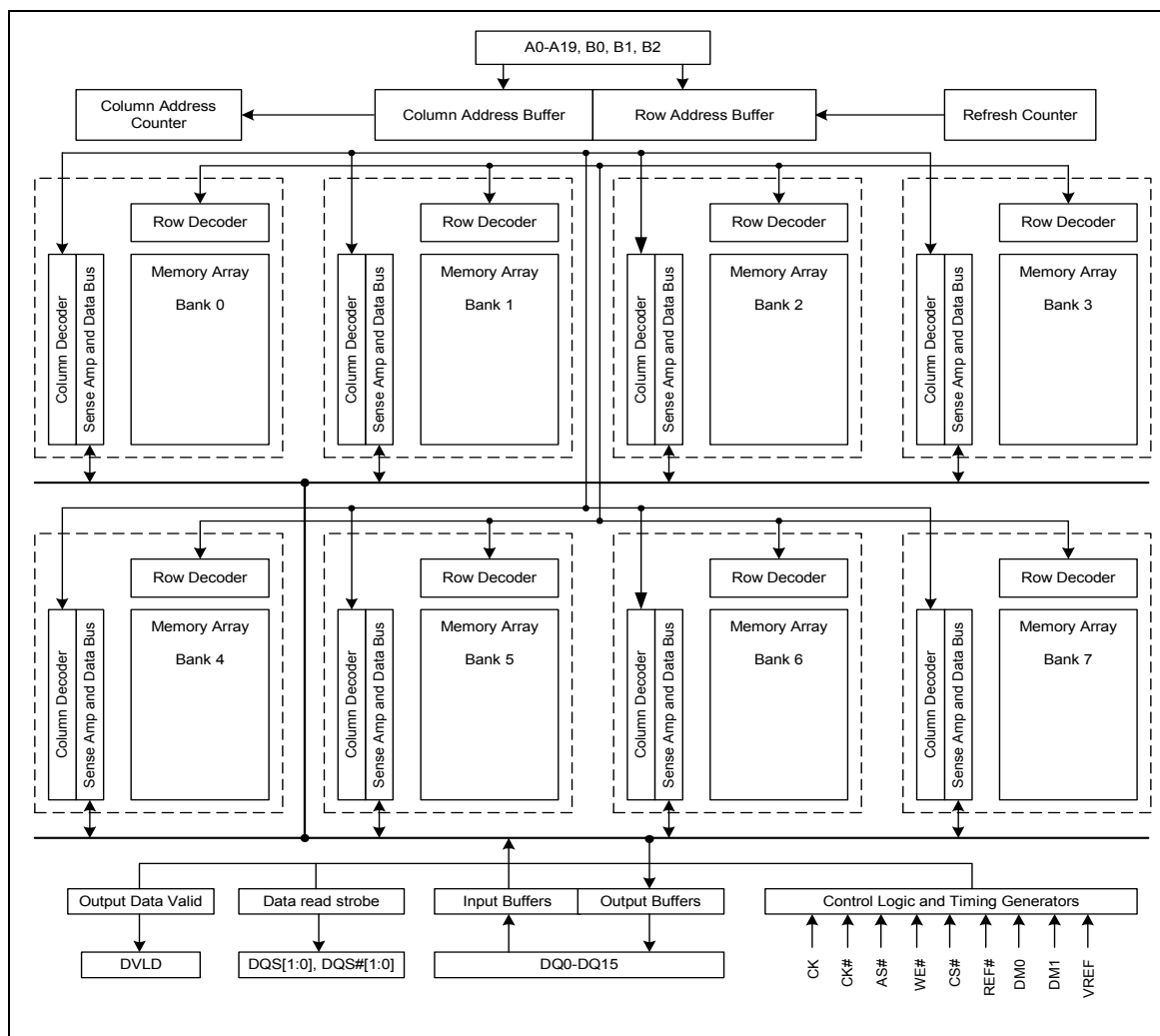
## 1.4 Functional Block Diagram

Figure 4 Functional Block Diagram 8M x 32 Configuration



Note: When the BL4 setting is used, A18 is a "Don't Care"

Figure 5 Functional Block Diagram 16M x 16 Configuration



Note: 1 When the BL4 setting is used, A19 is a "Don't Care".

Note: 2 In the 16Mx16 configuration, only DQS[1:0] & DQS#[1:0] are used

## 1.5 Commands

### 1.5.1 Command Table

According to the functional signal description the following command sequences are possible. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

**Table 3 Truth table**

Operation	Device State	Code	CS#	AS#	WE#	REF#	A[19:0] <sup>1)3)</sup>	BA[2:0]	DM[1:0]
No Operation	Any	NOP	L	H	H	H	X	X	X
Deselect <sup>4)</sup>	Any		H	X	X	X	X	X	X
Mode Register Set <sup>2)</sup>	Idle	MRS	L	L	L	L	Valid	X	X
Read	Any	READ	L	L	H	H	Valid	Valid	X
Write	Any	WRITE	L	L	L	H	Valid	Valid	Valid
Auto Refresh	Idle		L	H	H	L	X	Valid	X

Note: 1: X = "Don't Care" ; H = Logic HIGH; L = Logic LOW

Note: 2: Only A[17:0] are used for the MRS command.

Note: 3: See Table 4

**Table 4 Address Width table**

Data Width	32	16
Burst Length		
BL 2	A[18:0]	A[19:0]
BL 4	A[17:0]	A[18:0]

Note: 1: The x32 and x16 configurations have different ballouts (see Fig. 2 & Fig. 3)

### 1.5.2 Description of Commands

**Table 5 Description of Commands**

Command	Description
DESEL / NOP	The NOP command is used to perform a no operation to the RLDRAM; this is equal to deselecting the chip. Use NOP command to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history.
MRS	The Mode Register is set via the address inputs A[17:0]. See the mode register description in the register description section. The MRS command can only be issued when all banks are idle and no bursts are in progress.
READ	The READ command is used to initiate a burst read access to a bank. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[19:0] selects the data location within the bank.
WRITE	The WR command is used to initiate a burst write access to a bank. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[19:0] selects the data location within the bank. Input data appearing on the DQs is written to the memory array subject to the DMx input logic levels appearing coincident with the WRITE command. If DM0 is registered LOW, the first half of the burst Write data will be written to the memory array, if registered HIGH this data will be ignored i.e, this part of the data word will not be written. If DM1 is registered LOW the second half of the burst Write data will be written to the memory array, if registered HIGH this data will be ignored i.e, this part of the data word will not be written.
AREF	The AREF is used during normal operation of the RLDRAM to refresh the memory content of a bank. The value on the BA[2:0] inputs selects the bank. The refresh address is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AREF command. The RLDRAM requires 64k AREF cycles at an average periodic interval of $0.49 \mu s^1$ (maximum). To improve efficiency a burst of eight AREF commands (One AREF for each bank) can be posted to the RLDRAM at an average periodic interval of $3.9 \mu s^2$ .

Note: 1: Actual refresh is  $32ms/8K/8 = 0.488 \mu s$

Note: 2: Actual refresh is  $32ms/8K = 3.90 \mu s$

## 2 Functional Description

### 2.1 Clocks, Commands and Addresses

Figure 6 Clock Command/Address Timings

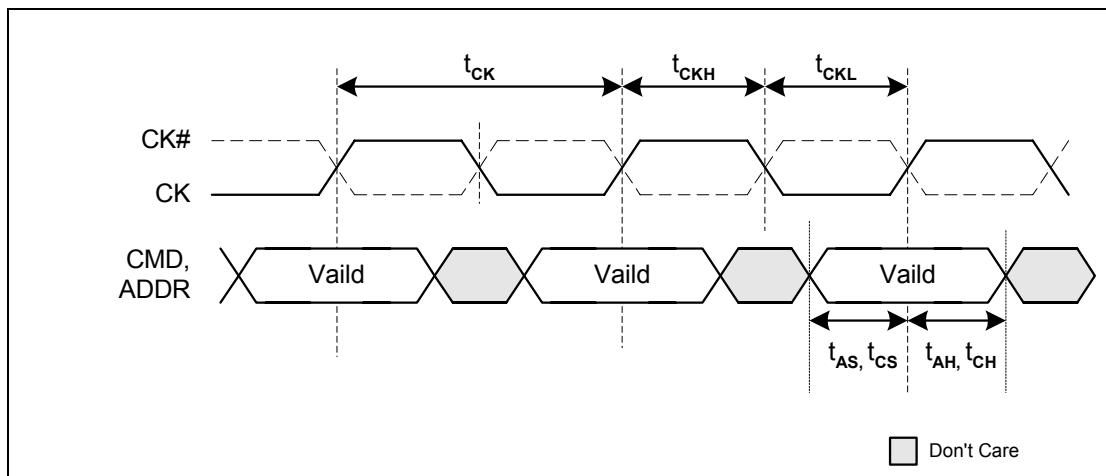


Table 6 General Timing Parameters for -2.5, -3.3 and -5.0 ns speed sorts

Parameter	Symbol	-3.3		-4.0		-5.0		Units
		min	max	min	max	min	max	
Clock								
Clock Cycle Time	$t_{CK}$	3.3	-	4.0	-	5.0	-	ns
Clock high level width	$t_{CKH}$	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
Clock low level width	$t_{CKL}$	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
Setup Times								
Address/Command input setup time	$t_{AS}, t_{CS}$	1.0	–	1.0	–	1.0	–	ns
Hold Times								
Address/Command input hold time	$t_{AH}, t_{CH}$	1.0	–	1.0	–	1.0	–	ns

Note: 1. All timings are measured relatively to the crossing point of CK/CK# and to the crossing point with VREF of the Command and Address signals.

Note: 2. The signal input slew rate must be  $\geq 1V/ns$ .

Note: 3. CK/CK# input slew rate must be  $\geq 1V/ns$  ( $\geq 2V/ns$  if measured differentially).

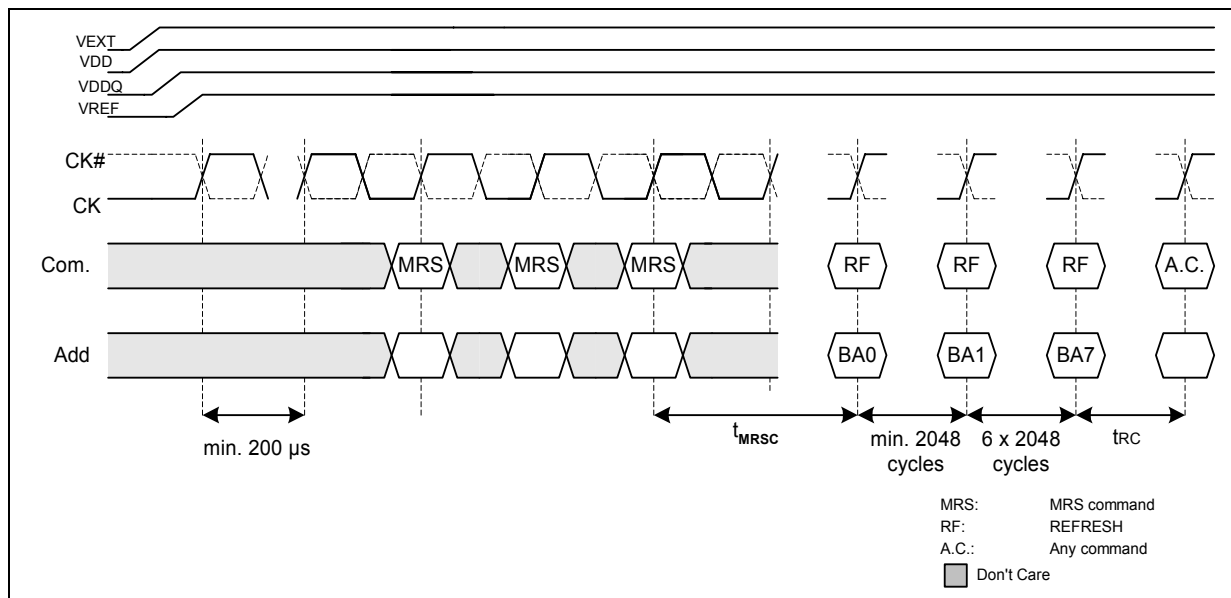
## 2.2 Initialization

The RLDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation or permanent damage to the device.

The following sequence is used for Power-Up:

1. Apply power ( $V_{EXT}$ ,  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$ ) and start clock as soon as the supply voltages are stable. Apply  $V_{DD}$  and  $V_{EXT}$  before or at the same time as  $V_{DDQ}$ , apply  $V_{DDQ}$  before or at the same time as  $V_{REF}$ . There is no timing relation between  $V_{EXT}$  and  $V_{DD}$ , the chip starts the power up sequence only when both voltages are at their nominal level. However, the pad supply must not be applied before the core supplies. Maintain all pins in NOP conditions.
2. Maintain stable conditions for 200  $\mu$ s minimum.
3. Issue three Mode Register Set commands - 2 dummies plus 1 valid MRS (Figure 7).
4. After  $t_{MRSC}$  issue 8 Auto Refresh commands, one on each bank and separated by 2048 cycles.
5. After  $t_{RC}$  the chip is ready for normal operation.

**Figure 7 Power Up Sequence**

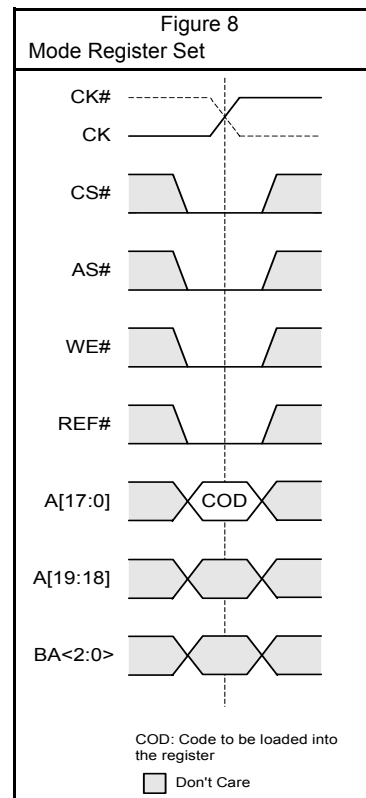
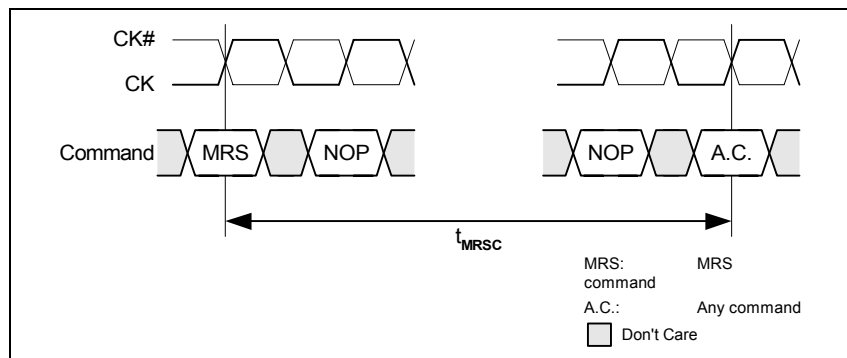


*Note: When the RLDRAM is powered up with the matched impedance mode inactive, the 2048 cycles between the 8 Refresh commands are not required. These cycles are necessary in order to calibrate the Output drivers.*

## 2.3 Mode Register Set Command (MRS)

The mode register stores the data for controlling the operating modes of the memory. It programs the RLDRAM configuration, burst length, test mode and IO options. During a Mode Register Set command the address inputs A<17:0> are sampled and stored in the mode register.  $t_{MRSC}$  must be met before any command can be issued to the RLDRAM. The mode register may only be set immediately after power up sequence.

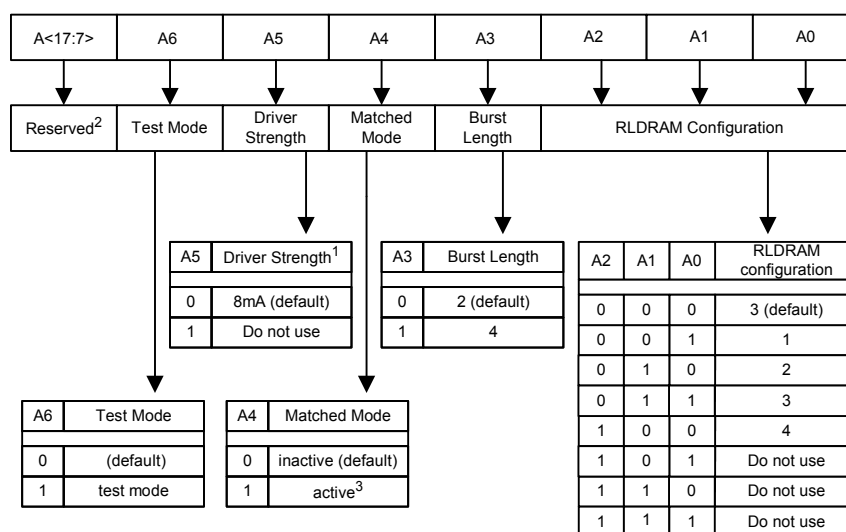
**Figure 9 Mode Register Set Timing**



**Table 7 Timing Parameters MRS**

Parameter	Symbol	-3.3		-4.0		-5.0		Units	Notes
		min	max	min	max	min	max		
Mode Register Set cycle time	$t_{MRSC}$	4	–	4	–	4	–	$t_{CK}$	

**Figure 10 Mode Register Bitmap**



Note: 1 HSTL compliant current specification

Note: 2 Bits A<17:6> must be set to zero

Note: 3 Automatic IO impedance calibration is activated in Matched Mode



## 2.4 Configuration Table

The following table shows, for different operating frequencies, the different RLDRAM configurations that can be programmed into the Mode Register. The Read Latency ( $t_{RL}$ ) and the Write Latency ( $t_{WL}$ ) used by the RLDRAM for the two Burst Lengths (BL) are also indicated. Finally the minimum row cycle time ( $t_{RC}$ ) in clock cycles and in ns are shown as well. The shaded areas correspond to configurations that are not allowed.

**Table 8 RLDRAM configuration table**

Configuration						
Frequency		Unit	1	2	3	4
	$t_{RC}$	cycles	5	6	7	8
	$t_{RL}$	cycles	5	5	5	6
	$t_{WL}$ (BL2)	cycles	2	2	2	3
	$t_{WL}$ (BL4)	cycles	1	1	1	2
300 MHz (-3.3)	$t_{RC}$	ns				26.7
	$t_{RL}$	ns				20
	$t_{WL}$ (BL2)	ns				10
	$t_{WL}$ (BL4)	ns				6.7
250 MHz (-4.0)	$t_{RC}$	ns			28.0	32.0
	$t_{RL}$	ns			20.0	24.0
	$t_{WL}$ (BL2)	ns			8.0	12.0
	$t_{WL}$ (BL4)	ns			4.0	8.0
200 MHz (-5.0)	$t_{RC}$	ns	25.0	30.0	35.0	40.0
	$t_{RL}$	ns	25.0	25.0	25.0	30.0
	$t_{WL}$ (BL2)	ns	10.0	10.0	10.0	15.0
	$t_{WL}$ (BL4)	ns	5.0	5.0	5.0	10.0

Note: 1: The speed sort -3.3 provides parts functional up to 300MHz in the configuration 4 only. The functionality of the configurations 1,2 and 3 is not guaranteed for speed sort -3.3.

Note: 2: The speed sort -4.0 provides parts functional up to 250MHz in the configurations 3 and 4 only. The functionality of the configurations 1 and 2 is not guaranteed for speed sort -4.0.

Note: 3: The speed sort -5.0 provides parts functional in all configurations.

## 2.5 Writes (WR)

### 2.5.1 Write - Basic Information

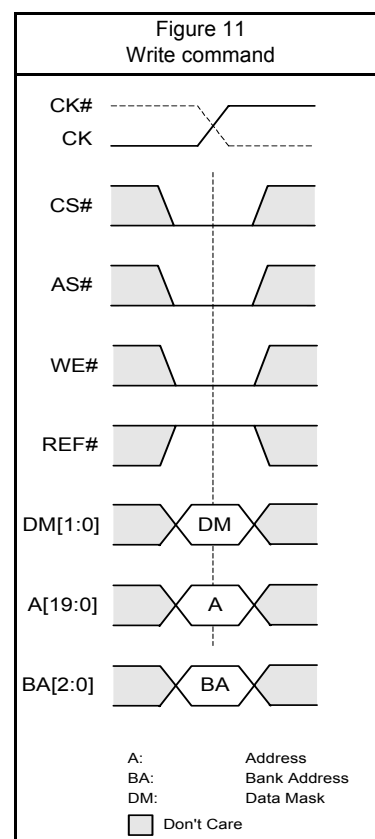
Write accesses are initiated with a WRITE command, as shown in Figure 11. Row and bank addresses are provided together with the WRITE command.

During WRITE commands, data will be registered at both edges of CK according to the programmed burst length BL. The first valid data is registered with the first rising CK edge WL (Write Latency) cycles after the WRITE command has been issued.

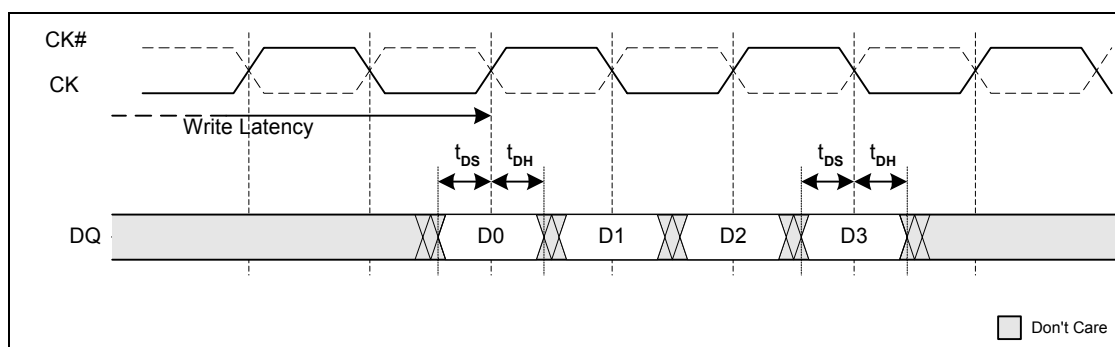
Any WRITE burst may be followed by a subsequent READ command. Figure 17 and Figure 18 illustrate the timing requirements for a WRITE followed by a READ for a burst of 2 and 4 respectively.

Setup and hold time for incoming DQs relative to the CK edges are specified as  $t_{DS}$  and  $t_{DH}$ .

The first or the second part of the incoming data burst is masked if the corresponding DMx signal is sampled HIGH along with the WRITE command. Setup and hold time for DM is the same as for addresses and commands.



**Figure 12 Basic Write Burst Timing**



**Table 9 WRITE Timing Parameters**

Parameter	Symbol	-3.3		-4.0		-5.0		Units	Notes
		min	max	min	max	min	max		
Data-in to CK Setup Time	$t_{DS}$	0.5	–	0.5	–	0.5	–	ns	
Data-in to CK Hold Time	$t_{DH}$	0.5	–	0.5	–	0.5	–	ns	

Note: 1. All timings are measured relative to the crossing point of CK/CK# and to the crossing point with VREF of the Command and Address signals.

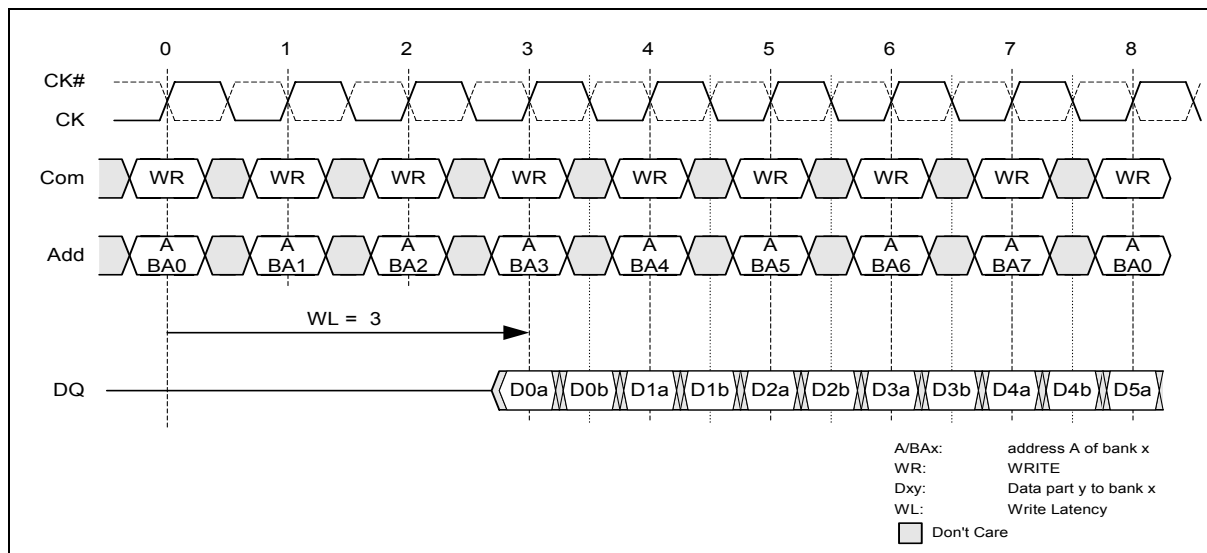
Note: 2. The signal input slew rate must be  $\geq 1V/ns$ .

Note: 3. CK/CK# input slew rate must be  $\geq 1V/ns$  ( $\geq 2V/ns$  if measured differentially).

## 2.5.2 Write - Cyclic Bank Access

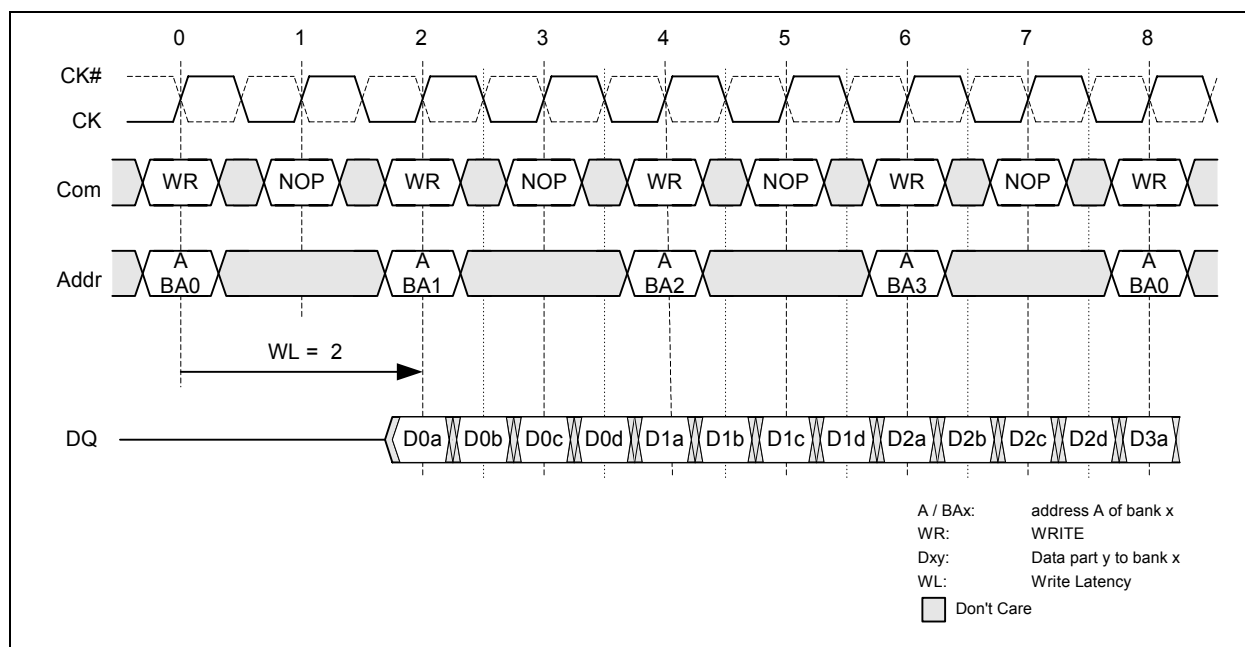
### 2.5.2.1 Burst Length (BL) = 2

Figure 13 Write Burst Basic Sequence, BL = 2, WL = 3



### 2.5.2.2 Burst Length (BL) = 4

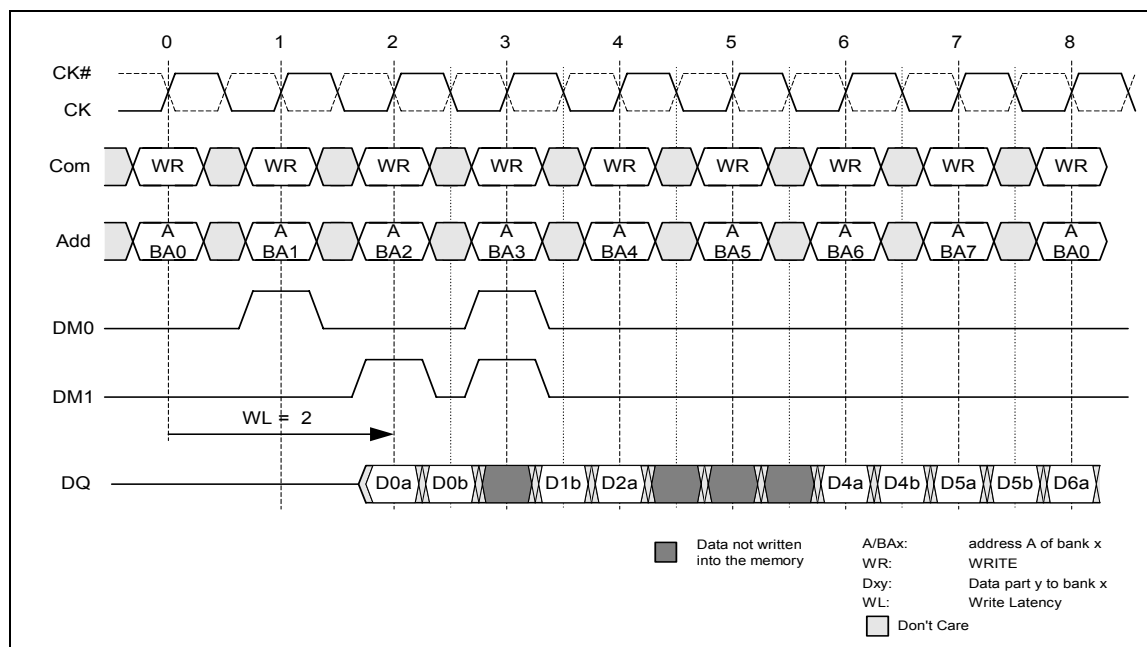
Figure 14 Write Burst Basic Sequence, BL = 4, WL = 2



## 2.5.3 Write Data Mask Timing

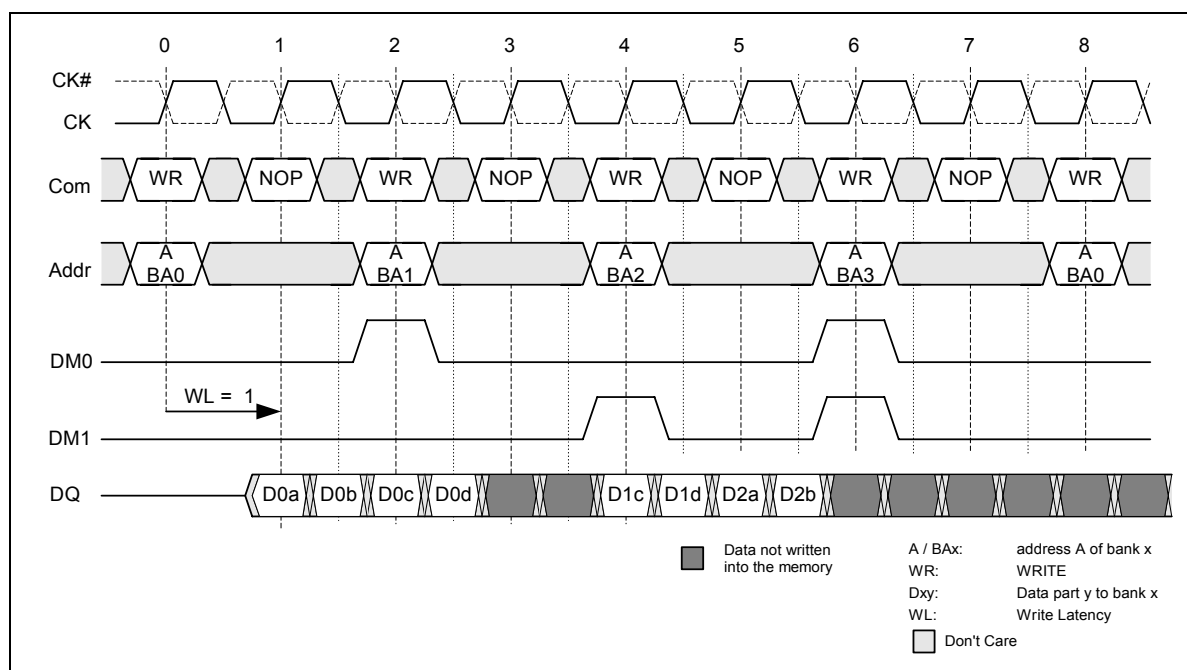
### 2.5.3.3 Burst Length (BL) = 2

Figure 15 Write Data Mask Timing, BL = 2, WL = 2



### 2.5.3.4 Burst Length (BL) = 4

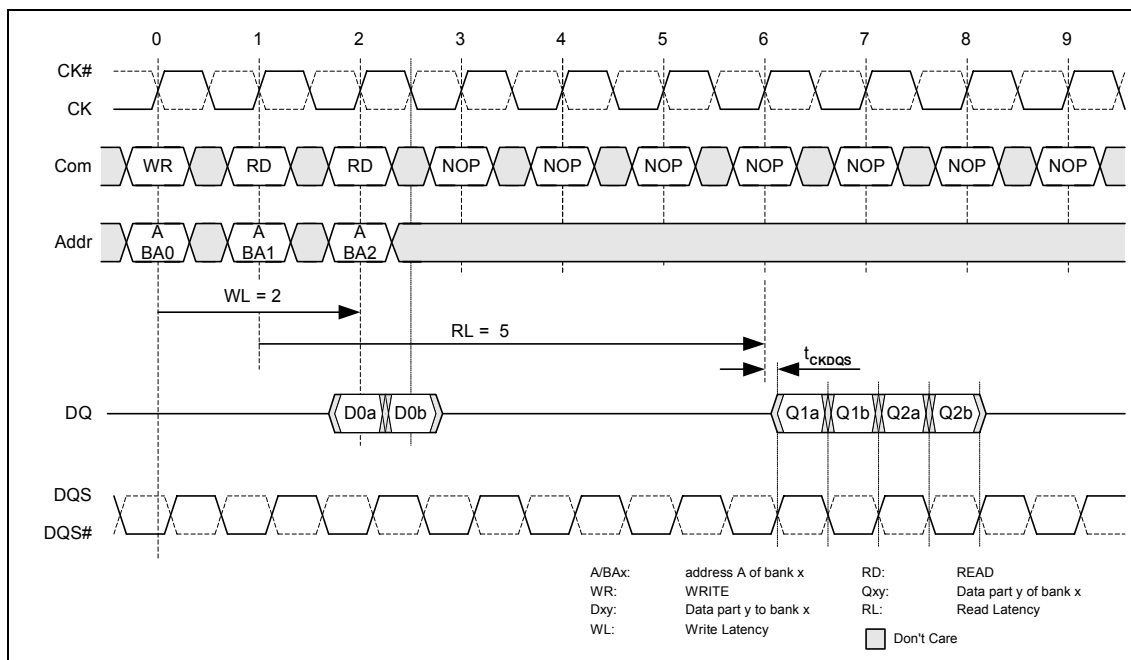
Figure 16 Write Data Mask Timing, BL=4, WL = 1



## 2.5.4 Write followed by Read

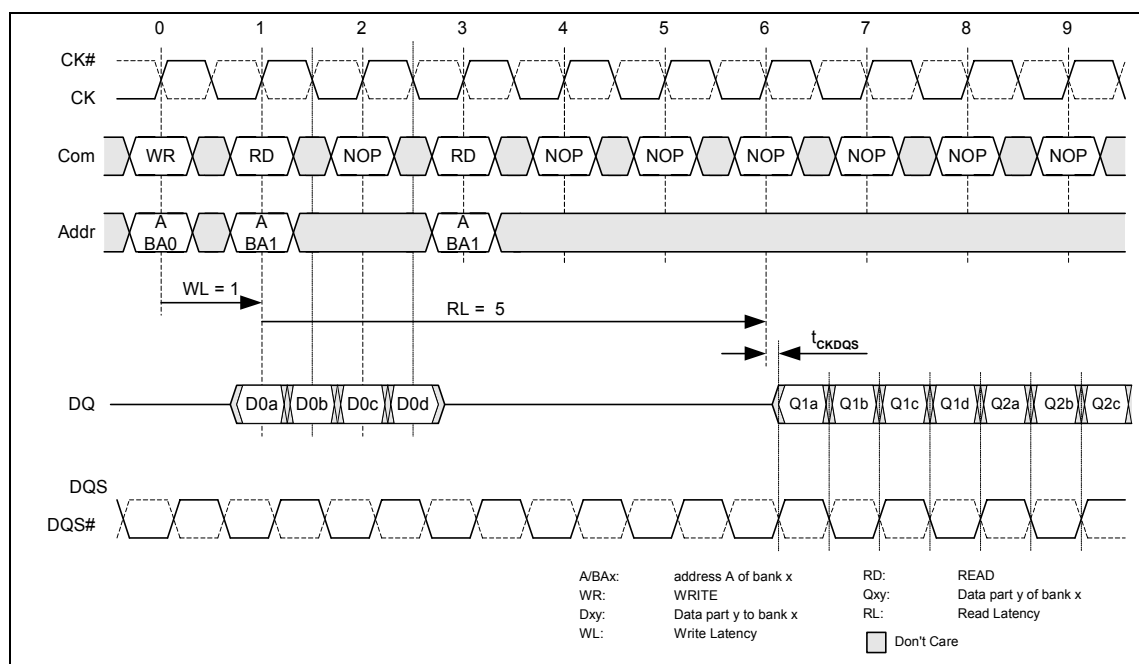
### 2.5.4.5 Burst Length (BL) = 2

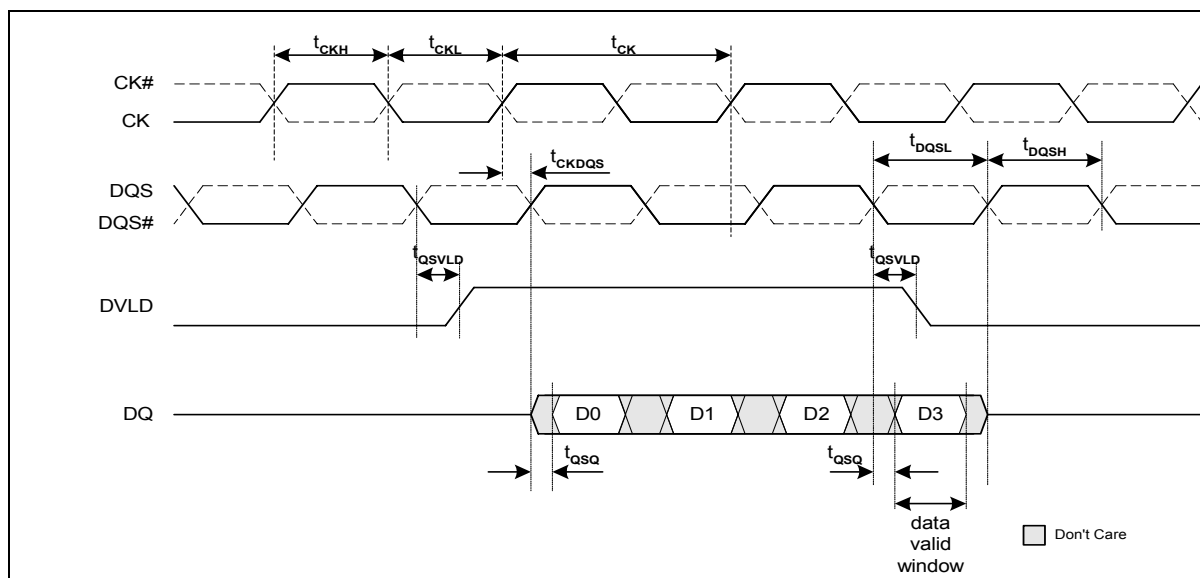
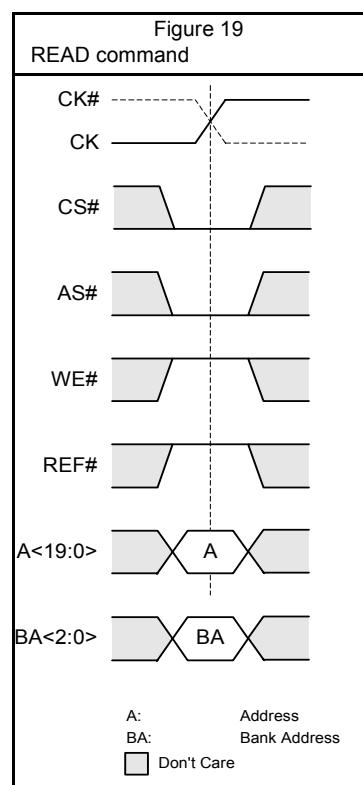
Figure 17 Write followed by Read BL = 2, RL = 5, WL = 2



### 2.5.4.6 Burst Length (BL) = 4

Figure 18 Write followed by Read BL = 4, RL = 5, WL = 1





**Table 10 READ Timing Parameters for -2.5, -3-3 and -5.0 speed sorts**

Parameter	Symbol	-3.3		-4.0		-5.0		Units	Notes
		min	max	min	max	min	max		
Read Cycle Timing Parameters for Data and Data Strobe									
DQS / DQS# high pulse width	$t_{DQSH}$	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
DQS / DQS# low pulse width	$t_{DQSL}$	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
DQS edge to Clock edge skew	$t_{CKDQS}$	2.7	3.7	2.7	3.7	2.7	3.7	ns	
DQS edge to output data edge	$t_{QSQ}$		0.3		0.3		0.3	ns	4
DQS edge to Data Out HiZ	$t_{QSQHZ}$		0.4		0.4		0.4	ns	4
DQS edge to DVLD edge	$t_{QSVLD}$	-0.4	0.4	-0.4	0.4	-0.4	0.4	ns	

Note: 1 All timings are measured relatively to the crossing point of CK/CK# (DQSx/DQSx#), and to the crossing point with VREF of the Command and Address signals.

Note: 2. The signal input slew rate must be  $\geq 1V/ns$ .

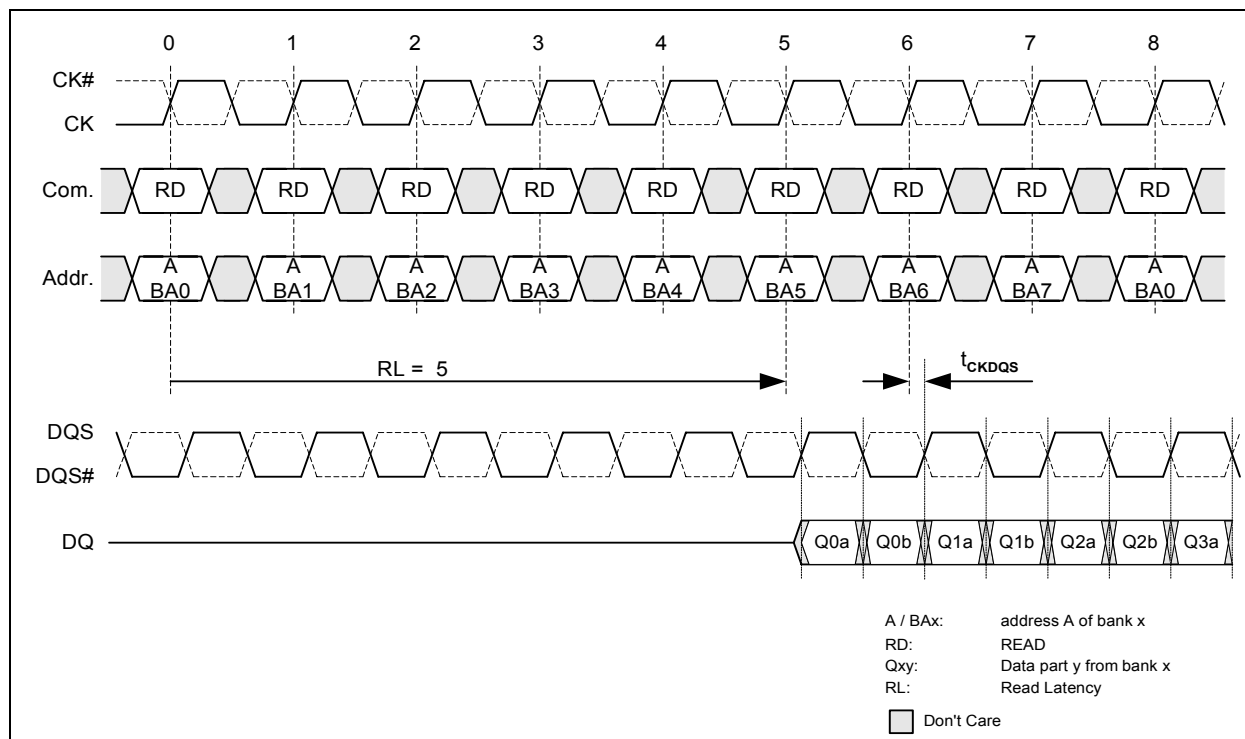
Note: 3. CK/CK# input slew rate must be  $\geq 1V/ns$  ( $\geq 2V/ns$  if measured differentially).

Note: 4.  $t_{DQSQ}$  and  $t_{QSQHZ}$  are absolute values.

## 2.6.2 Read - Cyclic Bank Access

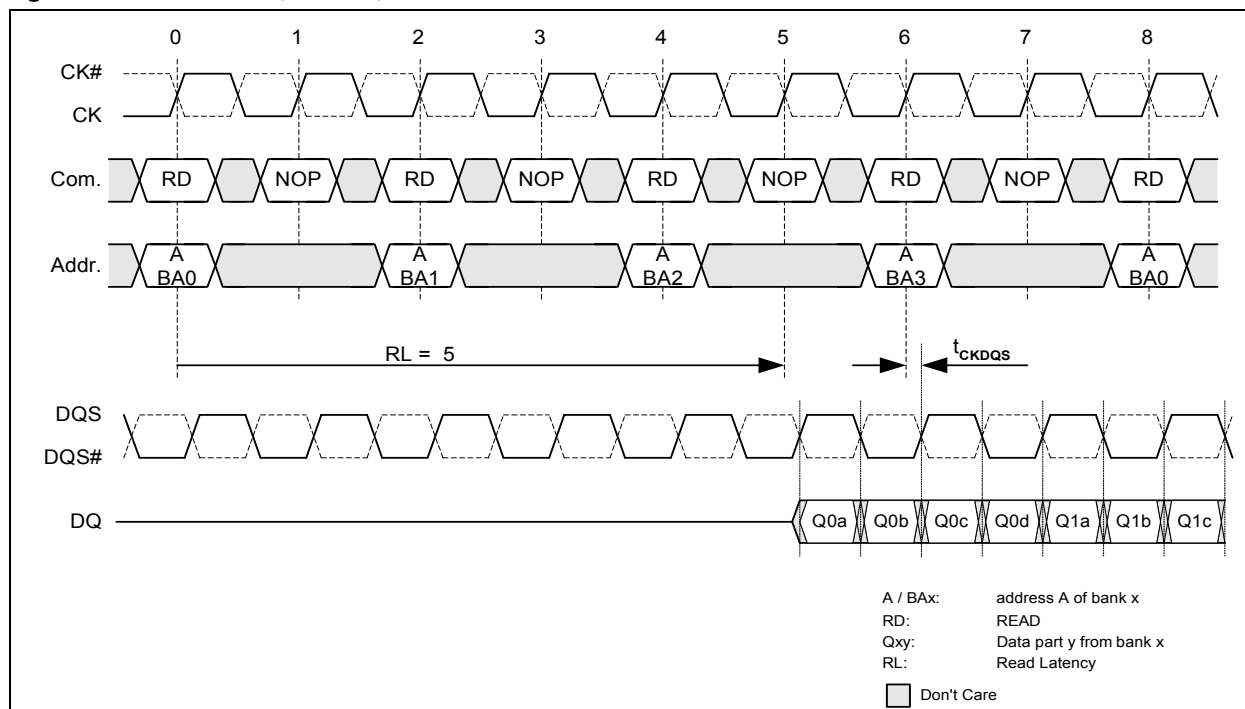
### 2.6.2.1 Burst Length (BL) = 2

Figure 21 Read Burst, BL = 2, RL = 5



### 2.6.2.2 Burst Length (BL) = 4

Figure 22 Read Burst, BL = 4, RL = 5





### 2.6.3 Read followed by Write

Figure 23 Read followed by Write, BL=2, RL = 5, WL = 2

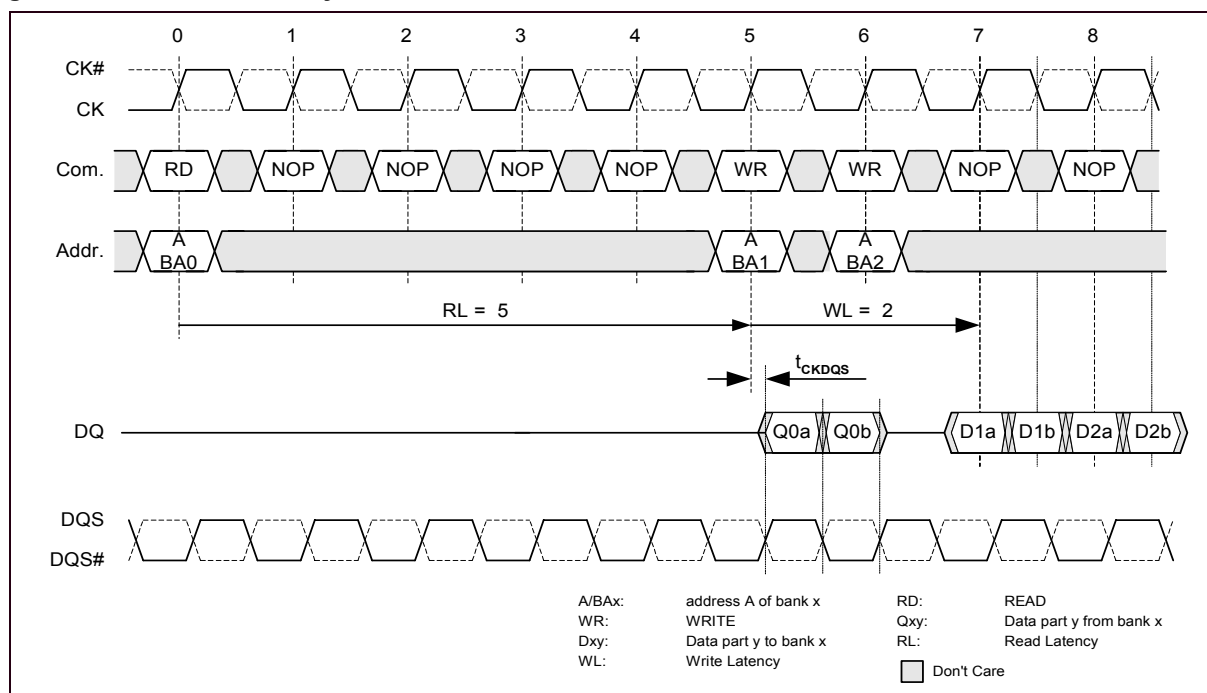


Figure 24 Read followed by Write, Write data on bus prior Read data, BL=2, RL=5, WL=2

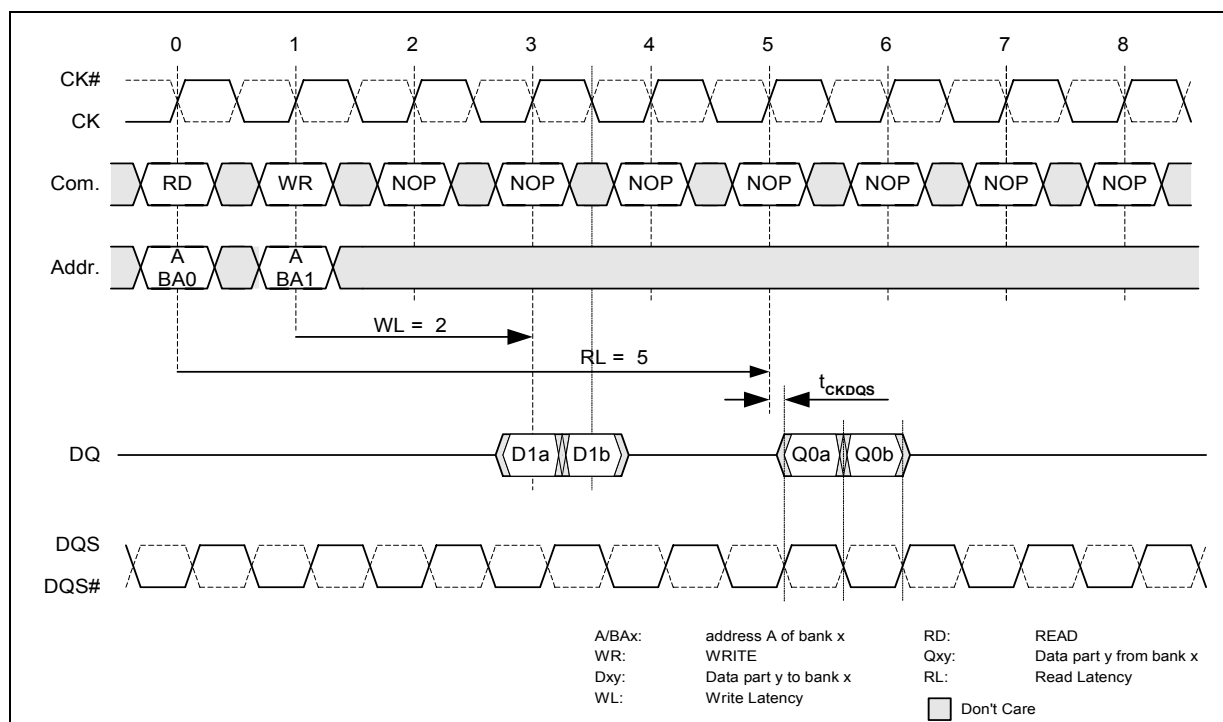


Figure 25 Read followed by Write, BL=4, RL = 5, WL = 1

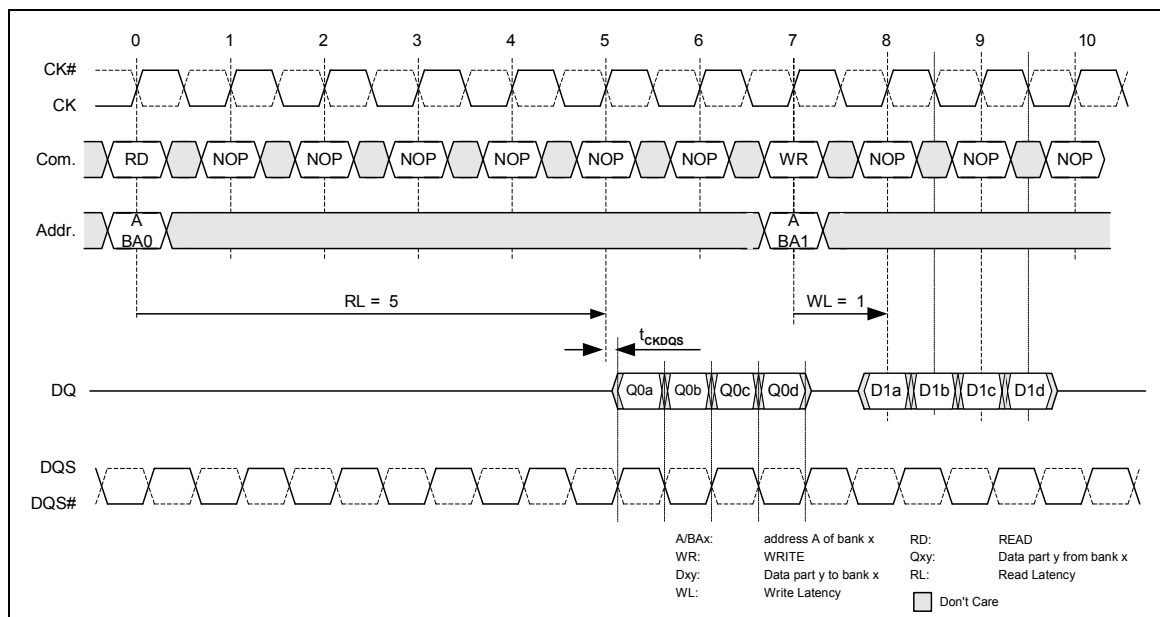
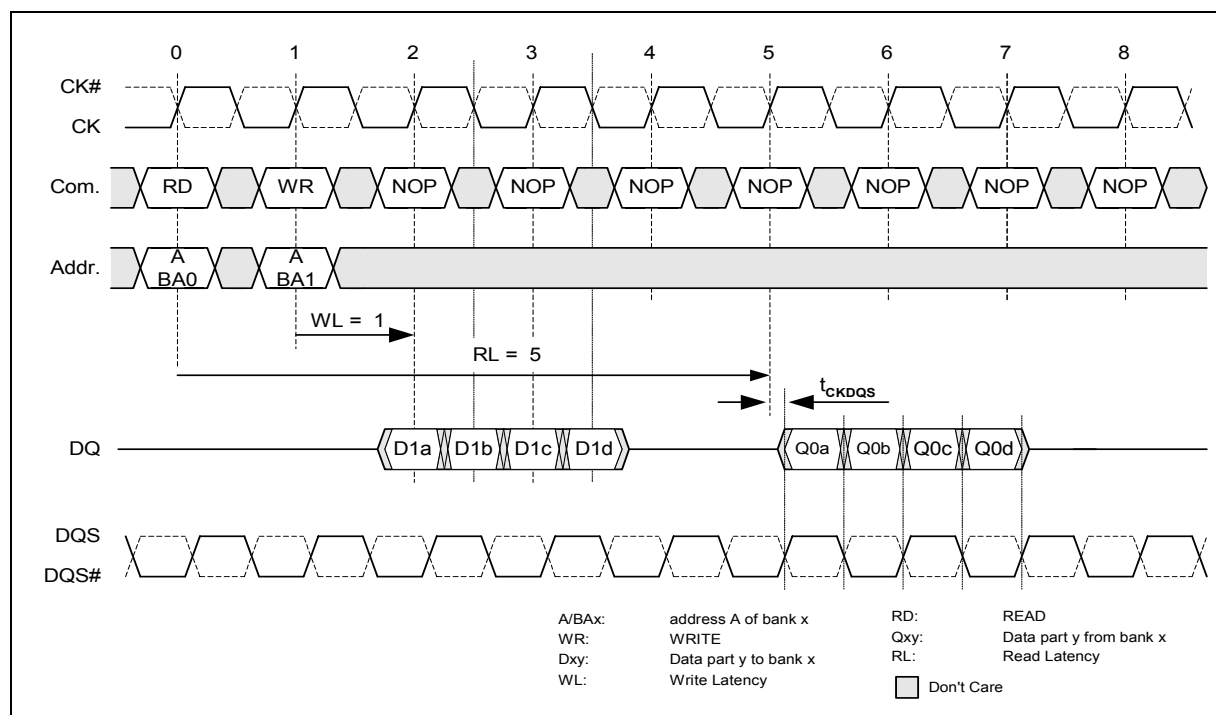


Figure 26 Read followed by Write, write data on system bus prior read data, BL=4, RL=5, WL=1



### **3 IEEE 1149.1 Serial Boundary Scan (JTAG)**

The RLDRAM incorporates a serial boundary scan Test Access Port (TAP). This port operates fully compliant with IEEE Standard 1149.1-1990. It contains a TAP controller, instruction register, boundary scan register, bypass register, and ID code register.

It is possible to operate the RLDRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied low while TDI, TMS and TDO may be left unconnected. Upon power-up, the TAP will come up in a reset state which will not interfere with the normal operation of the device.

#### **3.1 Test Access Port (TAP)**

##### **3.1.1 Test Clock (TCK)**

The test clock is used only with the TAP controller. The pin must be tied low if the TAP is not used.

##### **3.1.2 Test Mode Select (TMS)**

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used.

##### **3.1.3 Test Data-In (TDI)**

The TDI pin is used to serially input information into the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is connected to the most significant bit (MSB) of any register (see Figure 27). This pin may be left unconnected if the TAP is not used.

##### **3.1.4 Test Data-Out (TDO)**

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Figure 28). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see Figure 27). This pin may be left unconnected if the TAP is not used.

#### **3.2 TAP Registers**

Registers are connected between the TDI and TDO pins and allow data to be scanned into and shifted out of the RLDRAM test circuitry (see Figure 27). Only one register is selected at a time through the instruction register. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

##### **3.2.1 Instruction Register**

Eight-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in Figure 27. Upon power-up, the instruction register is internally preloaded with the IDCODE instruction.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

##### **3.2.2 Bypass Register**

The bypass register is a single-bit register that can be placed between the TDI and TDO pins. This allows data to be shifted through the RLDRAM with minimal delay.

The bypass register is set LOW during the Capture-DR state when the BYPASS instruction is loaded in the instruction register.

### 3.2.3 Boundary Scan Register

The boundary scan register is connected to all the IO pins on the RLDRAM. It allows to observe and control the data flowing into and out of the device, depending on the instruction being loaded in the instruction register.

The boundary scan register is 104 bits long. The register is the same for the x16 and x32 configurations of the RLDRAM. Pins not used in the x16 configurations read a HIGH into the boundary scan register in the Capture-DR controller state.

Differential inputs (CK/CK#) and outputs (DQSx/DQSx#) are equipped with two boundary scan cells each. Thus, the differential nature of these pins is not visible to the test circuitry. However, it is recommended that during testing differential signals are always applied to these pin pairs.

### 3.2.4 Identification (ID) Register

The ID register is loaded with a hardwired, vendor-specific, 32-bit code during the Capture-DR state when the IDCODE instruction is loaded in the instruction register. The code can be shifted out when the TAP controller is in the Shift-DR state. Two different codes are implemented for the x16 and x32 configurations of the RLDRAM (see Table 11).

**Table 11 ID Register Definition**

	Revision Number				Part Number																Infineon JEDEC Code																L S B
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
x16	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1				
x32	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1				

## 3.3 TAP Instructions

The TAP implements the 6 instructions BYPASS, EXTEST, SAMPLE/PRELOAD and IDCODE for user access (see Table 12). The implementation of these instructions fully complies with the IEEE standard. All other instructions are reserved and should not be used.

**Table 12 JTAG Instruction Register**

Instruction Register Code		Instruction	Description
Hex	x7 .. x0		
00	0000 0000	EXTEST	Selects the boundary scan register to be connected between TDI and TDO. Data received at input pins are sampled and loaded into the boundary scan register. Data driven by output pins are determined from values contained in the boundary scan register.
05	0000 0101	SAMPLE / PRELOAD	Selects the boundary scan register to be connected between TDI and TDO. Data received at input pins are sampled and loaded into the boundary scan register. Initial output data are shifted into the boundary scan register prior to an EXTEST instruction. Instruction does not interfere with the normal operation of the device.
21	0010 0001	IDCODE	Selects the ID code register to be connected to TDI and TDO. Instruction does not interfere with the normal operation of the device.
FF	1111 1111	BYPASS	Selects the bypass register to be connected between TDI and TDO. Instruction does not interfere with the normal operation of the device.

### 3.4 Boundary Scan Exit Order

#### 3.4.1 x16 Configuration

Scan Reg#	Reg Content	Pin Descr	Pin Name	Ball #		Ball #	Pin Name	Pin Descr	Reg Content	Scan Reg #
27	Data	I/O	DQ1	B10		B3	DQ9	I/O	Enb Data	26
28	Enb									25
29	Data	I/O	DQ0	B11		B2	DQ8	I/O	Enb Data	24
30	Enb									23
31	Data	I/O	DQ3	C10		C3	DQ11	I/O	Enb Data	22
32	Enb									21
33	Data	I/O	DQ2	C11		C2	DQ10	I/O	Enb Data	20
34	Enb									19
35	Data	O	DQS0#	D10		D3	DQS1#	O	Data	18
36	Data	O	DQS0	D11		D2	DQS1	O	Data	17
37	Data	I/O	DQ4	E11		E2	DQ12	I/O	Enb Data	16
38	Enb									15
39	Data	I/O	DQ5	E10		E3	DQ13	I/O	Enb Data	14
40	Enb									13
41	Data	I/O	DQ6	F11		F2	DQ14	I/O	Enb Data	12
42	Enb									11
43	Data	I/O	DQ7	F10		F3	DQ15	I/O	Enb Data	10
44	Enb									9
45	Data	O	DVLD	F12		F1	DM0	I	Data	8
46	Data	I	A1	G11		G2	A6	I	Data	7
47	Data	I	A2	G10		G3	A7	I	Data	6
48	Data	I	A0	G12		G1	A5	I	Data	5
49	Data	I	A3	H12		H1	A8	I	Data	4
50	Data	I	A4	H11		H2	A9	I	Data	3
51	Data	I	B0	J11		J2	B2	I	Data	2
52	Data	I	CK	J12		J1	AS#	I	Data	1
53	Data	I	CK#	K12		K1	WE#	I	Data	104
54	Data	I	B1	K11		K2	REF#	I	Data	103
55	Data	I	A14	L11		L2	CS#	I	Data	102
56	Data	I	A13	L12		L1	A19	I	Data	101
57	Data	I	A10	M12		M1	A15	I	Data	100
58	Data	I	A12	M10		M3	A17	I	Data	99
59	Data	I	A11	M11		M2	A16	I	Data	98
60	Data	I	A18	N12		N1	DM1	I	Data	97
61	Data	I/O	DQ31	N10		N3	DQ23	I/O	Enb Data	96
62	Enb									95
63	Data	I/O	DQ30	N11		N2	DQ22	I/O	Enb Data	94
64	Enb									93
65	Data	I/O	DQ29	P10		P3	DQ21	I/O	Enb Data	92
66	Enb									91
67	Data	I/O	DQ28	P11		P2	DQ20	I/O	Enb Data	90
68	Enb									89
69	Data	O	DQS3	R11		R2	DQS2	O	Data	88
70	Data	O	DQS3#	R10		R3	DQS2#	O	Data	87
71	Data	I/O	DQ26	T11		T2	DQ18	I/O	Enb Data	86
72	Enb									85
73	Data	I/O	DQ27	T10		T3	DQ19	I/O	Enb Data	84
74	Enb									83
75	Data	I/O	DQ24	U11		U2	DQ16	I/O	Enb Data	82
76	Enb									81
77	Data	I/O	DQ25	U10		U3	DQ17	I/O	Enb Data	80
78	Enb									79

Note: 1: Input pins are connected to Observe-Only Boundary Scan Register Cells.

Note: 2: Output pins are connected to Force-Only Boundary Scan Register Cells.

Note: 3: IO pins are connected to Control-and-Observe Boundary Scan Register Cells.

Note: 4: For BL 4 the content of the register 101 will be set to 0 if A19 is not connected. Otherwise, the register content will be equal to the logical value applied to pin A19.

### 3.4.2 x32 Configuration

Scan Reg#	Reg Content	Pin Descr	Pin Name	Ball #		Ball #	Pin Name	Pin Descr	Reg Content	Scan Reg #
27	Data	I/O	DQ1	B10		B3	DQ9	I/O	Enb Data	26
28	Enb									25
29	Data	I/O	DQ0	B11		B2	DQ8	I/O	Enb Data	24
30	Enb									23
31	Data	I/O	DQ3	C10		C3	DQ11	I/O	Enb Data	22
32	Enb									21
33	Data	I/O	DQ2	C11		C2	DQ10	I/O	Enb Data	20
34	Enb									19
35	Data	O	DQS0#	D10		D3	DQS1#	O	Data	18
36	Data	O	DQS0	D11		D2	DQS1	O	Data	17
37	Data	I/O	DQ4	E11		E2	DQ12	I/O	Enb Data	16
38	Enb									15
39	Data	I/O	DQ5	E10		E3	DQ13	I/O	Enb Data	14
40	Enb									13
41	Data	I/O	DQ6	F11		F2	DQ14	I/O	Enb Data	12
42	Enb									11
43	Data	I/O	DQ7	F10		F3	DQ15	I/O	Enb Data	10
44	Enb									9
45	Data	O	DVLD	F12		F1	DM0	I	Data	8
46	Data	I	A1	G11		G2	A6	I	Data	7
47	Data	I	A2	G10		G3	A7	I	Data	6
48	Data	I	A0	G12		G1	A5	I	Data	5
49	Data	I	A3	H12		H1	A8	I	Data	4
50	Data	I	A4	H11		H2	A9	I	Data	3
51	Data	I	B0	J11		J2	B2	I	Data	2
52	Data	I	CK	J12		J1	AS#	I	Data	1
53	Data	I	CK#	K12		K1	WE#	I	Data	104
54	Data	I	B1	K11		K2	REF#	I	Data	103
55	Data	I	A14	L11		L2	CS#	I	Data	102
56	Data	I	A13	L12		L1	A18	I	Data	101
57	Data	I	A10	M12		M1	A15	I	Data	100
58	Data	I	A12	M10		M3	A17	I	Data	99
59	Data	I	A11	M11		M2	A16	I	Data	98
60	Data	I	NC	N12		N1	DM1	I	Data	97
61	Data	I/O	DQ31	N10		N3	DQ23	I/O	Enb Data	96
62	Enb									95
63	Data	I/O	DQ30	N11		N2	DQ22	I/O	Enb Data	94
64	Enb									93
65	Data	I/O	DQ29	P10		P3	DQ21	I/O	Enb Data	92
66	Enb									91
67	Data	I/O	DQ28	P11		P2	DQ20	I/O	Enb Data	90
68	Enb									89
69	Data	O	DQS3	R11		R2	DQS2	O	Data	88
70	Data	O	DQS3#	R10		R3	DQS2#	O	Data	87
71	Data	I/O	DQ26	T11		T2	DQ18	I/O	Enb Data	86
72	Enb									85
73	Data	I/O	DQ27	T10		T3	DQ19	I/O	Enb Data	84
74	Enb									83
75	Data	I/O	DQ24	U11		U2	DQ16	I/O	Enb Data	82
76	Enb									81
77	Data	I/O	DQ25	U10		U3	DQ17	I/O	Enb Data	80
78	Enb									79

Note: 1: Input pins are connected to Observe-Only Boundary Scan Register Cells.

Note: 2: Output pins are connected to Force-Only Boundary Scan Register Cells.

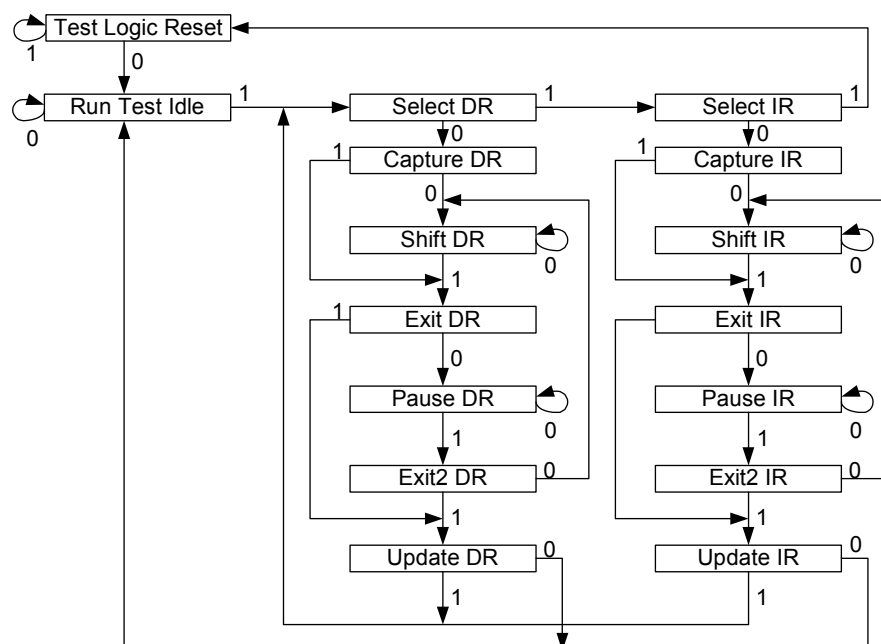
Note: 3: IO pins are connected to Control-and-Observe Boundary Scan Register Cells.

Note: 4: For BL 4 the content of the register 101 will be set to 0 if A18 is not connected. Otherwise, the register content will be equal to the logical value applied to pin A18.



### 3.7 JTAG TAP Controller State Diagram

Figure 28 TAP Controller State Diagram



### 3.8 JTAG DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input logic high voltage, DC	V <sub>TIH</sub>	V <sub>REF</sub> + 0.15	-	V <sub>DDQ</sub> + 0.3	V	
Input logic low voltage, DC	V <sub>TIL</sub>	V <sub>SSQ</sub> - 0.3	-	V <sub>REF</sub> - 0.15	V	
Output logic high voltage (I <sub>OH</sub> = -tbd mA)	V <sub>TOH</sub>	V <sub>REF</sub> + tbd	-	-	V	
Output logic low voltage (I <sub>OL</sub> = tbd mA)	V <sub>TOL</sub>	-	-	V <sub>REF</sub> - tbd	V	



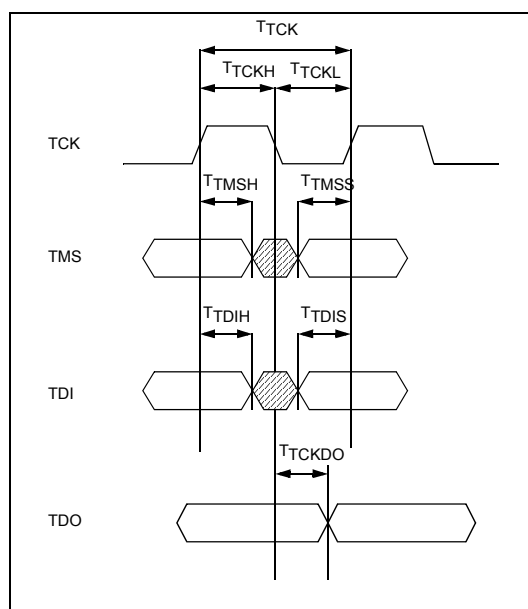
### 3.9 JTAG AC Operating Conditions

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Input logic high voltage, AC	$V_{TIH}$	$V_{REF}+0.3$	-	$V_{DDQ}+0.3$	V	
Input logic low voltage, AC	$V_{TIL}$	$V_{SSQ}-0.3$	-	$V_{REF}-0.3$	V	
Input Slew Rate	$T_{TSL}$	1.0	-	-	V/ns	
Input and Output Timing Reference Level	$V_{REF}$		$V_{DDQ}/2$		V	

### 3.10 JTAG AC Electrical Characteristics

Parameter	Symbol	min.	max.	Unit	Notes
TCK Cycle Time	$T_{TCK}$	20	-	ns	
TCK High Pulse Width	$T_{TCKH}$	10	-	ns	
TCK Low Pulse Width	$T_{TCKL}$	10	-	ns	
TCK Low to TDO Valid	$T_{TCKDO}$	-	10	ns	
TDI Set Up Time	$T_{TDIS}$	5	-	ns	
TMS Set Up Time	$T_{TMSS}$	5	-	ns	
TDI Hold Time	$T_{TDIH}$	5	-	ns	
TMS Hold Time	$T_{TMSh}$	5	-	ns	

### 3.11 JTAG Timing Diagram



## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings

- Storage temperature range ..... – 55 to + 150 °C
- Input/output pins voltage ..... – 0.3 to  $V_{DDQ} + 0.3V$
- Inputs and  $V_{REF}$  voltage ..... – 0.3 to  $V_{DDQ} + 0.3V$
- Power supply voltage  $V_{DD}$  ..... – 0.3 to + 2.1V
- Power supply voltage  $V_{EXT}$  ..... – 0.3 to + 2.8V
- Power supply voltage  $V_{DDQ}$  ..... – 0.3 to + 2.1V
- Junction Temperature ..... 0°C to 100°C

*Note:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 4.2 Recommended Power & DC Operation Ratings

All values are recommended operating conditions unless otherwise noted.

**Table 13 Power & DC Operating Conditions**

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Power Supply Voltages	$V_{EXT}$	2.38	2.5	2.63	V	
	$V_{DD}$	1.75	1.8	1.85	V	
Power Supply Voltage for I/O	$V_{DDQ}$	1.7	1.8	1.9	V	
Reference Voltage	$V_{ref}$	0.49* $V_{DDQ}$	0.9	0.51* $V_{DDQ}$	V	1,2,3
Input leakage current	$I_{IL}$	-5		+5	$\mu A$	
CLK Input leakage current	$I_{ILC}$	-5		+5	$\mu A$	
Output leakage current	$I_{OL}$	-5		+5	$\mu A$	
$V_{REF}$ Current	$I_{REF}$	-5		+5	$\mu A$	
Matched Impedance 1.8V						
Input logic high voltage, DC	$V_{IH}$	$V_{ref} + 0.15$	–	$V_{DDQ} + 0.3$	V	
Input logic low voltage, DC	$V_{IL}$	$V_{SSQ} - 0.3$	–	$V_{ref} - 0.15$	V	
Output high voltage	$V_{OH}$	$V_{DDQ}$	-	-	V	
Output low voltage	$V_{OL}$	-	-	0	V	
HSTL strong						
Input logic high voltage, DC	$V_{IH}$	$V_{ref} + 0.1$	–	$V_{DDQ} + 0.3$	V	
Input logic low voltage, DC	$V_{IL}$	$V_{SSQ} - 0.3$	–	$V_{ref} - 0.1$	V	
Output high voltage	$V_{OH}$	$V_{DDQ} - 0.4$	-	-	V	
Output low voltage	$V_{OL}$	-	-	0.4	V	

*Note:* 1. Typically the value of  $V_{ref}$  is expected to be  $0.5 * V_{DDQ}$  of the transmitting device.  $V_{ref}$  is expected to track variations in  $V_{DDQ}$

*Note:* 2. Peak to peak AC noise on  $V_{ref}$  may not exceed 2%  $V_{ref}$  (DC)

*Note:* 3.  $V_{tt}$  of the transmitting device must track  $V_{ref}$  of the receiving device.

*Note:* 4. Recommended on board decoupling capacitors :  $V_{DDQ}$ :  $2 \times 0.1 \mu F$  / device,  $V_{DD}$ :  $2 \times 0.1 \mu F$  / device,  $V_{REF}$ :  $0.1 \mu F$  / device,  $V_{EXT}$ :  $0.1 \mu F$  / device.

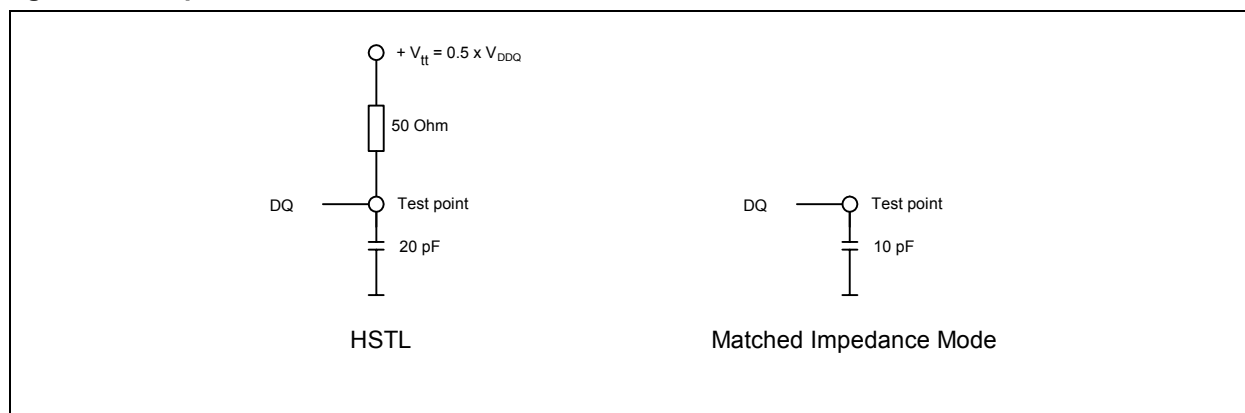
### 4.3 AC Operation Ratings

**Table 14 AC Operation Conditions for Matched Impedance mode**

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Matched Impedance 1.8V						
Input logic high voltage, AC DDR	$V_{IH}$	$V_{ref} + 0.3$	–	$V_{DDQ} + 0.3$	V	
Input logic low voltage, AC DDR	$V_{IL}$	$V_{SSQ} - 0.3$	–	$V_{ref} - 0.3$	V	
Clock Differential Input Voltage (CLK/ CLK#)	$V_{ID}$	0.6	–	$V_{DDQ} + 0.6$	V	
Clock Input Crossing Point (CLK/ CLK#)	$V_{IX}$	$V_{ref} - 0.15$	$V_{ref}$	$V_{ref} + 0.15$	V	
I/O Reference Voltage	$V_{ref}$	$0.49 \cdot V_{DDQ}$		$0.51 \cdot V_{DDQ}$	V	
HSTL strong						
Input logic high voltage, AC DDR	$V_{IH}$	$V_{ref} + 0.3$	–	$V_{DDQ} + 0.3$	V	
Input logic low voltage, AC DDR	$V_{IL}$	$V_{SSQ} - 0.3$	–	$V_{ref} - 0.3$	V	
Clock Differential Input Voltage (CLK/ CLK#)	$V_{ID}$	0.6	–	$V_{DDQ} + 0.6$	V	
Clock Input Crossing Point (CLK/ CLK#)	$V_{IX}$	$V_{ref} - 0.15$	$V_{ref}$	$V_{ref} + 0.15$	V	
I/O Reference Voltage	$V_{ref}$	$0.49 \cdot V_{DDQ}$		$0.51 \cdot V_{DDQ}$	V	

### 4.4 Output Test Conditions

**Figure 29 Output Test Circuits**



Note:  $V_{DDQ} = 1.8V \pm 0.1V$ ,  $T_J = 0^\circ C$  to  $100^\circ C$

### 4.5 Pin Capacitances

**Table 15 Pin Capacitances**

Pin	Min	Typ.	Max	Unit
A<19:0>, BA<2:0>, CS#, AREF#, WE#	2.0	3.0	4.0	pF
CLK, CLK#	2.0	3.0	4.0	pF
DQ<31:0>, DQS0, DQS0#, DQS1, DQS1#, DVLD, DM	2.0	3.0	4.0	pF

## 4.6 Operating Currents

**Table 16 IDD Specifications and Conditions**

Parameter	Symbol/ Freq		Limit Values		Unit	Notes
			x16	x32		
IDD1 (*) Operating Current (Average Power Supply Current)	300MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	Burst Length = 2 $t_{CK}=\min$ , $t_{RC}=\min$ , 1 bank active, Address change one time during min $t_{RC}$ , Read/Write command cycling <sup>1.)</sup>
	250MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	
	200MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	
IDD4R (*) Operating Current (Average Power Supply Current)	300MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	Burst Length = 4 $t_{CK}=\min$ , $t_{RC}=\min$ , 4 banks interleave, address change with each bank activation, continuous read operation <sup>1.)</sup>
	250MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	
	200MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	
IDD8 (*) Operating Current (Average Power Supply Current)	300MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	Burst Length = 2 $t_{CK}=\min$ , $t_{RC}=\min$ , 8banks interleave, address change with each bank activation, continuous read operation <sup>1.)</sup>
	250MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	
	200MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	
Standby Current	300MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	$t_{CK}=\min$ All banks idle, $\overline{CS}=1$ address/data toggling one time/4 clk clock inputs
	250MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	
	200MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	
Auto Refresh Current	300MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	$t_{CK}=\min$ All banks idle, $\overline{CS}=1$ 64k refresh commands/ 32ms
	250MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	
	200MHz	VDD VEXT	tbd tbd	tbd tbd	mA mA	