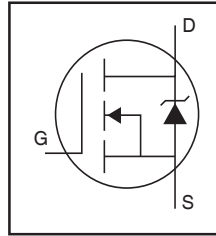


AUIRFR3504

HEXFET® Power MOSFET

Features

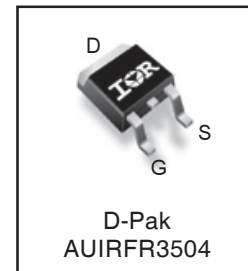
- Advanced Planar Technology
- Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified*



$V_{(BR)DSS}$	40V
$R_{DS(on)}$ typ.	7.8mΩ
max	9.2mΩ
I_D (Silicon Limited)	87A^⑧
I_D (Package Limited)	56A

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	87 ^⑧	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	61 ^⑧	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	56	
I_{DM}	Pulsed Drain Current ^①	350	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	140	W
	Linear Derating Factor	0.92	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ^②	240	mJ
$E_{AS} \text{ (tested)}$	Single Pulse Avalanche Energy Tested Value ^②	480	
I_{AR}	Avalanche Current ^①	See Fig. 12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ^①		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^⑩	—	1.09	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ^⑨	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.041	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.8	9.2	m Ω	$V_{GS} = 10V, I_D = 30A$ ④**
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	40	—	—	S	$V_{DS} = 10V, I_D = 30A$ ④**
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	48	71	nC	$I_D = 30A$ **
Q_{gs}	Gate-to-Source Charge	—	12	18		$V_{DS} = 32V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	13	20		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 20V$
t_r	Rise Time	—	53	—		$I_D = 30A$ **
$t_{d(off)}$	Turn-Off Delay Time	—	36	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	22	—		$V_{GS} = 10V$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2150	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	580	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	46	—		$f = 1.0MHz$, See Fig. 5
C_{oss}	Output Capacitance	—	2830	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	510	—		$V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	870	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V$

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	87⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	350		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 30A$ **, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	53	80	ns	$T_J = 25^\circ\text{C}, I_F = 30A$ **, $V_{DD} = 20V$
Q_{rr}	Reverse Recovery Charge	—	86	130	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.52mH$, $R_G = 25\Omega$, $I_{AS} = 30A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ $I_{SD} \leq 30A$, $di/dt \leq 170A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 1.0ms$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

- ⑥ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.
- ⑧ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 56A.
- ⑨ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑩ R_θ is measured at T_J of approximately 90°C .
- ** All AC and DC test conditions based on former package limited current of 30A.

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101) ^{††}	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D-Pak	MSL1
ESD	Machine Model	Class M4 (+/- 500V) ^{†††} AEC-Q101-002	
	Human Body Model	Class H1C (+/- 1500V) ^{†††} AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) ^{†††} AEC-Q101-005	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

†† Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

††† Highest passing voltage.

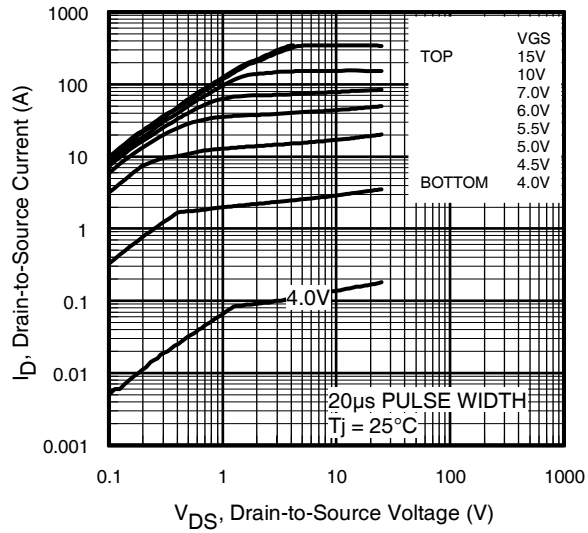


Fig 1. Typical Output Characteristics

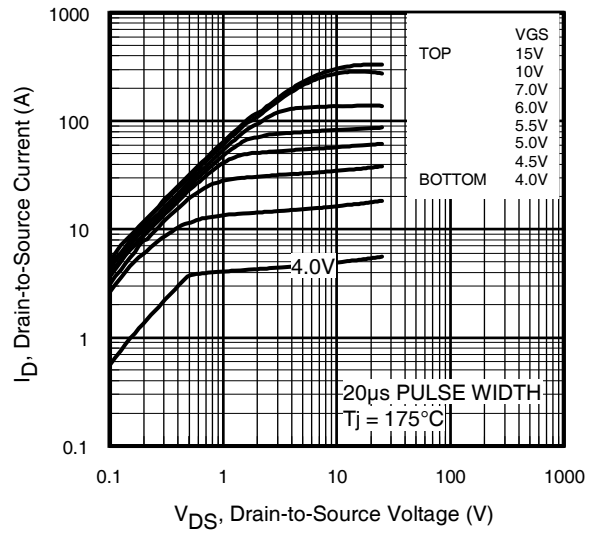


Fig 2. Typical Output Characteristics

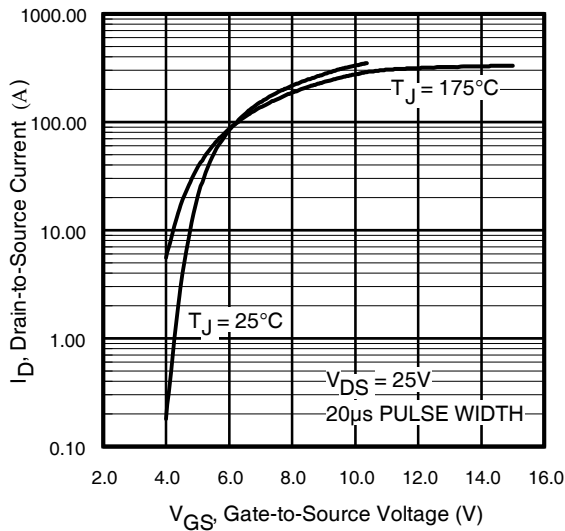


Fig 3. Typical Transfer Characteristics

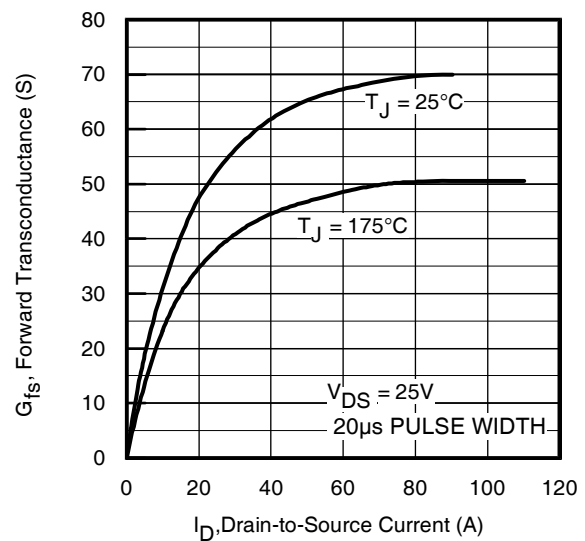


Fig 4. Typical Forward Transconductance Vs. Drain Current

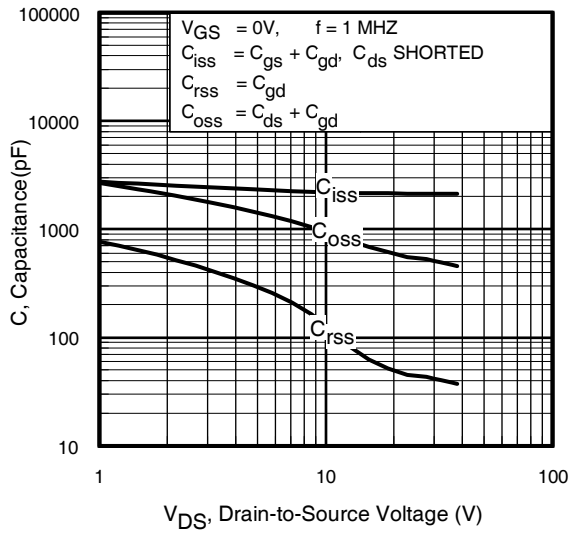


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

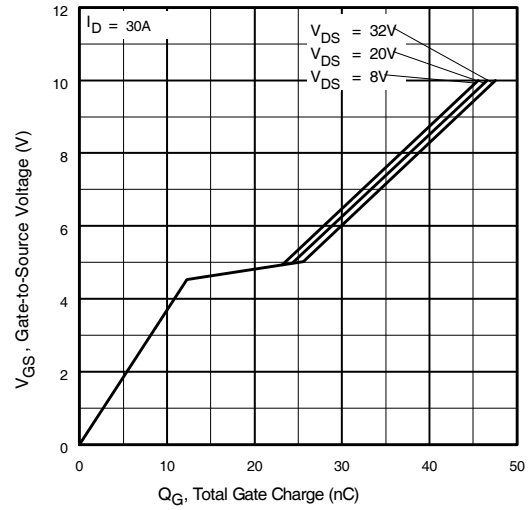


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

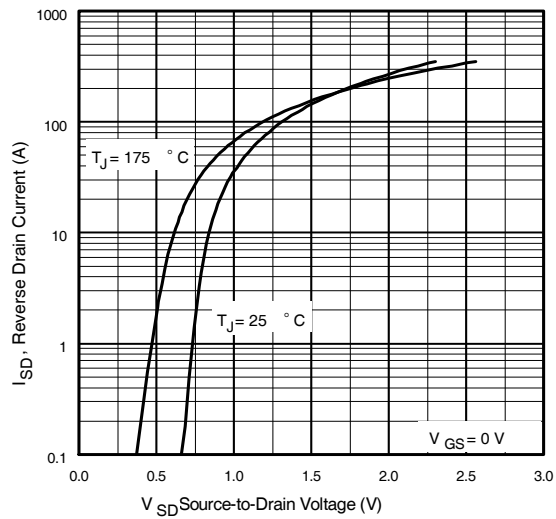


Fig 7. Typical Source-Drain Diode Forward Voltage

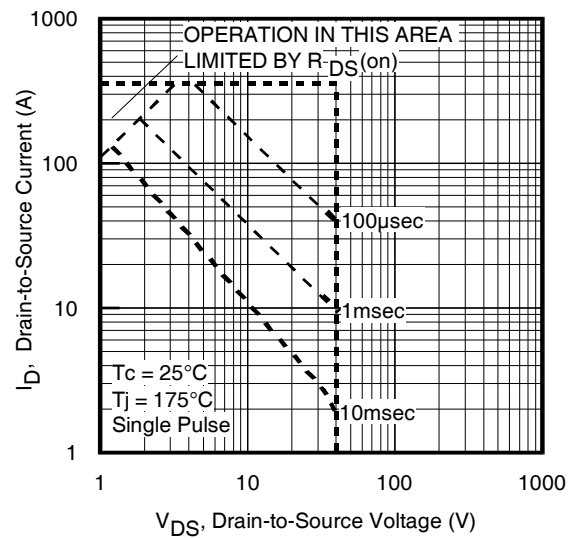


Fig 8. Maximum Safe Operating Area

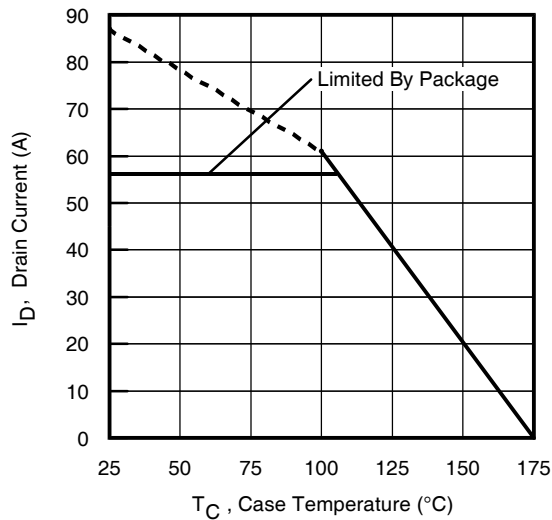


Fig 9. Maximum Drain Current Vs. Case Temperature

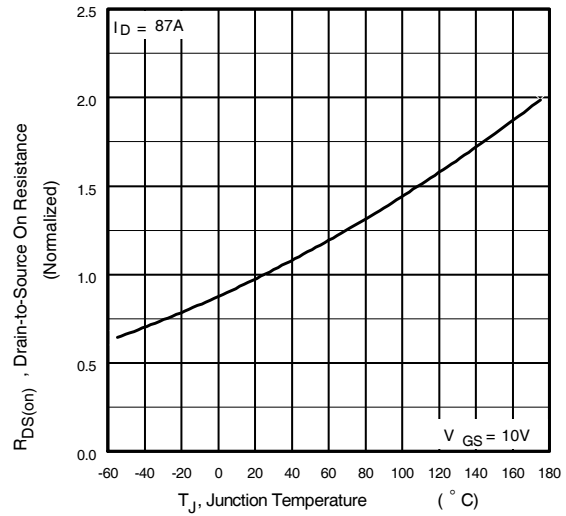


Fig 10. Normalized On-Resistance Vs. Temperature

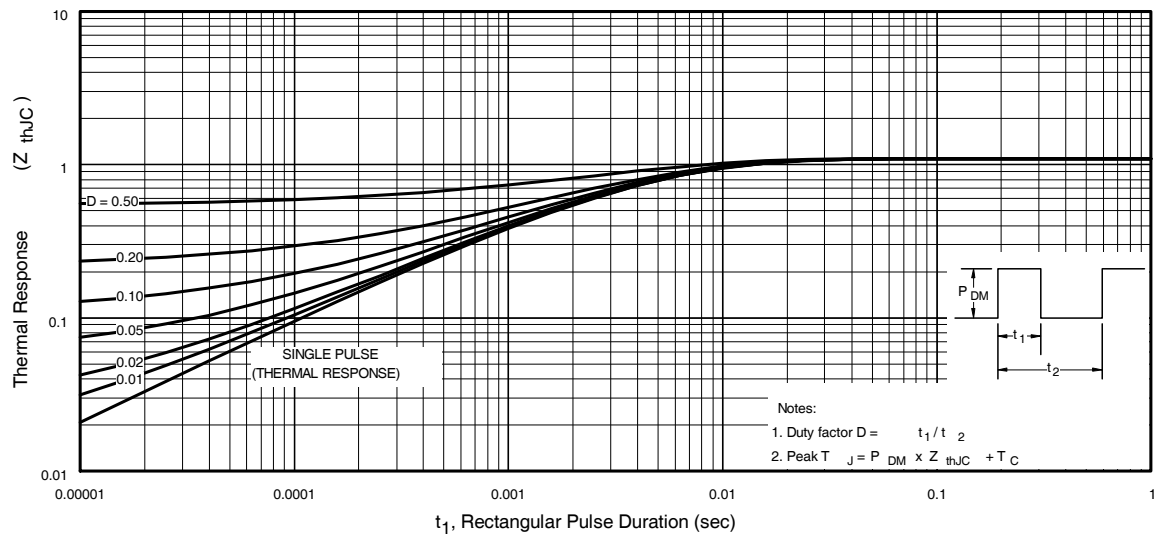


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

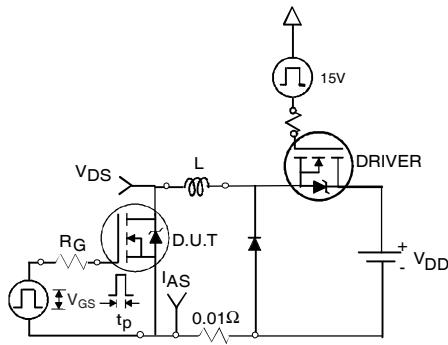


Fig 12a. Unclamped Inductive Test Circuit

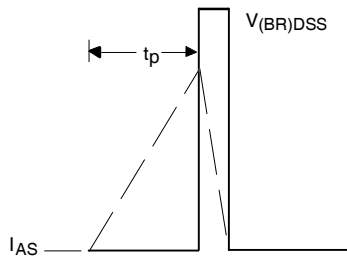


Fig 12b. Unclamped Inductive Waveforms

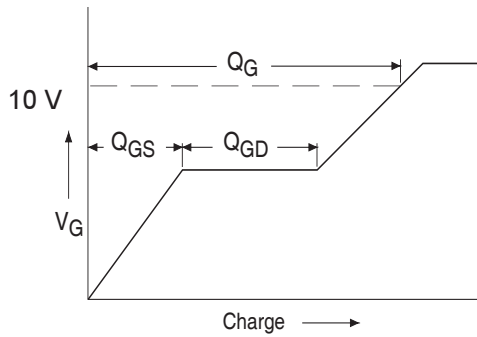


Fig 13a. Basic Gate Charge Waveform

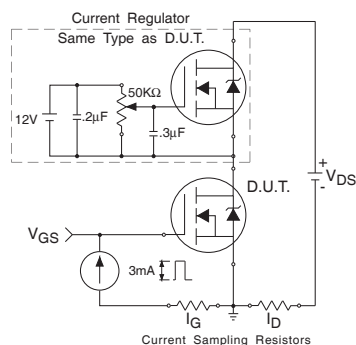


Fig 13b. Gate Charge Test Circuit
www.irf.com

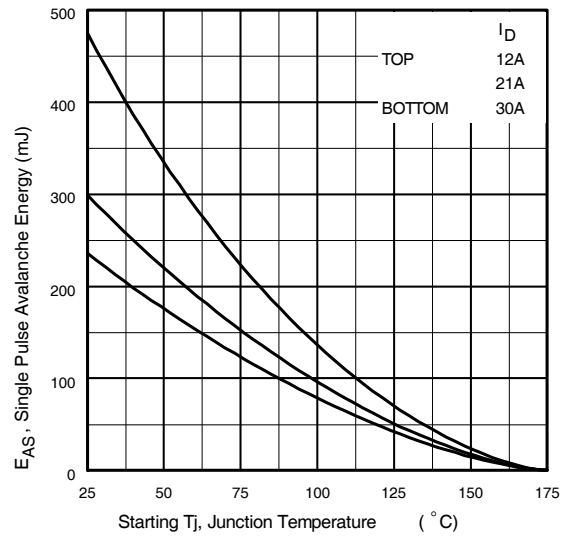


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

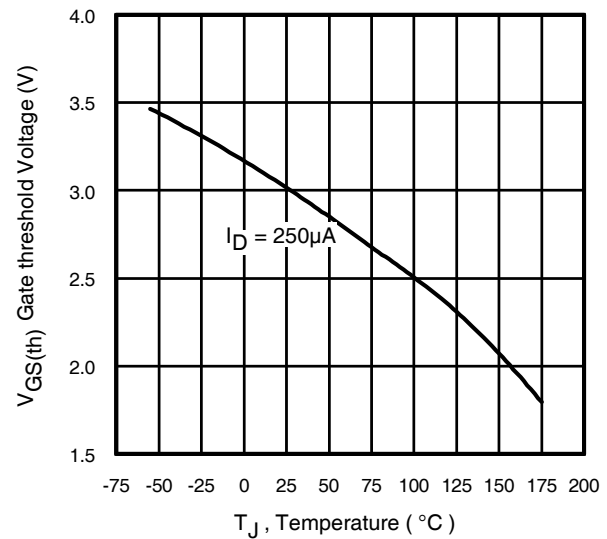


Fig 14. Threshold Voltage Vs. Temperature

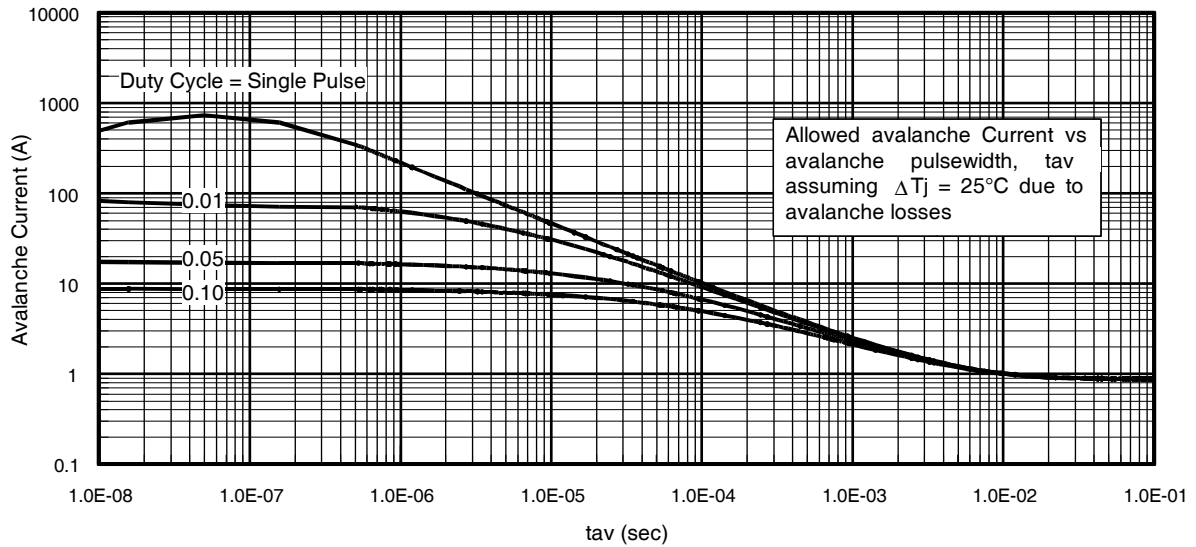
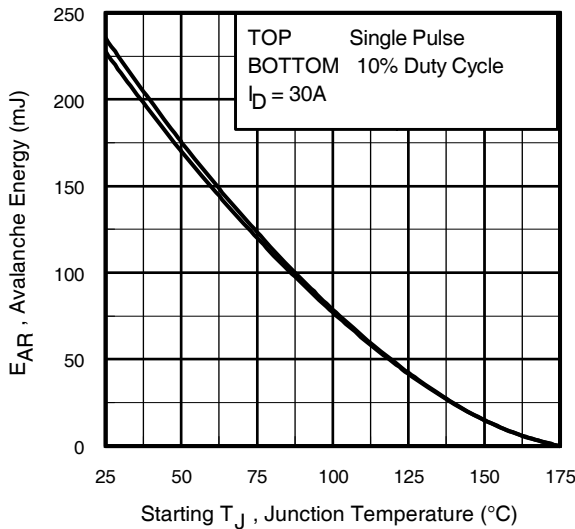


Fig 15. Typical Avalanche Current Vs. Pulsewidth



Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = \frac{1}{2} (1.3 \cdot BV \cdot I_{av}) = \frac{\Delta T}{Z_{thJC}}$$

$$I_{av} = \frac{2 \Delta T}{1.3 \cdot BV \cdot Z_{thJC}}$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 16. Maximum Avalanche Energy
Vs. Temperature

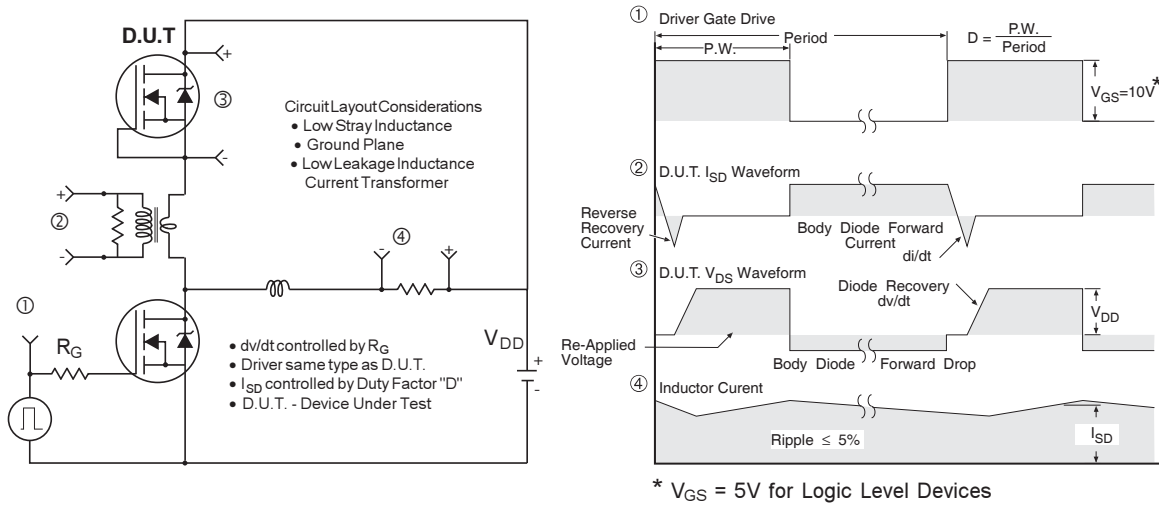


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

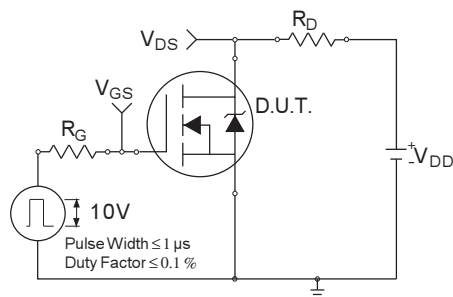


Fig 18a. Switching Time Test Circuit

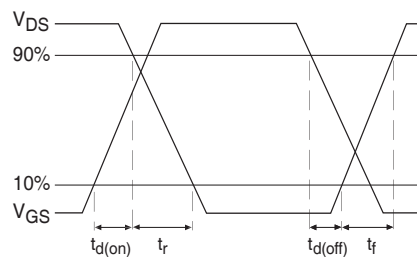
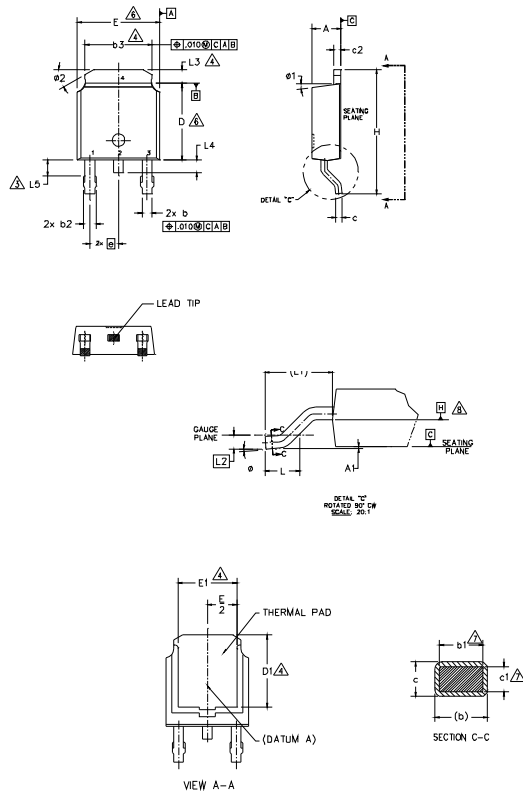


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
3. LEAD DIMENSION UNCONTROLLED IN L5.
4. DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5. SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10
[0.13 AND 0.25] FROM THE LEAD TIP.
6. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER
SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7. DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9. OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	—	.013	—	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	—	.205	—	
E	6.35	6.73	.250	.265	6
E1	4.32	—	.170	—	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 RF		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	—	1.02	—	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

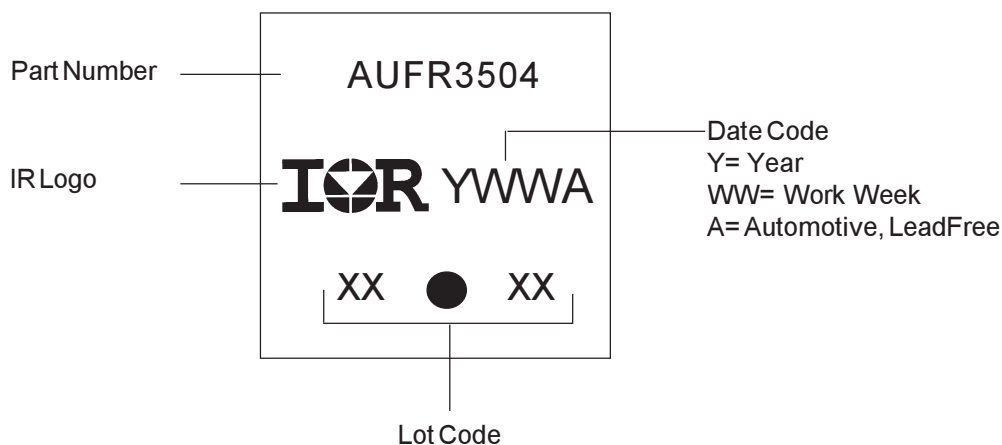
LEAD ASSIGNMENTS

- HEXFET
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
 - 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

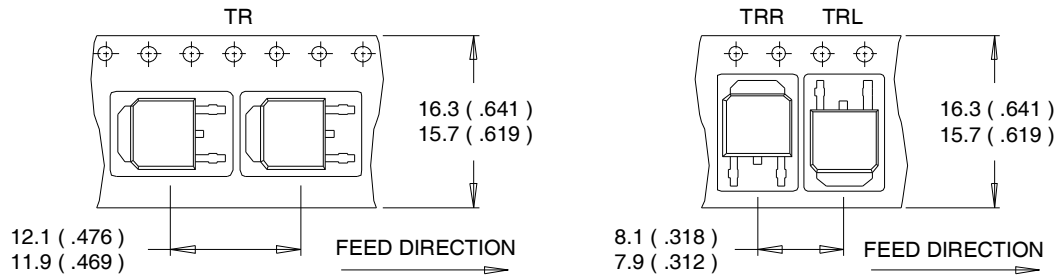
D-Pak Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

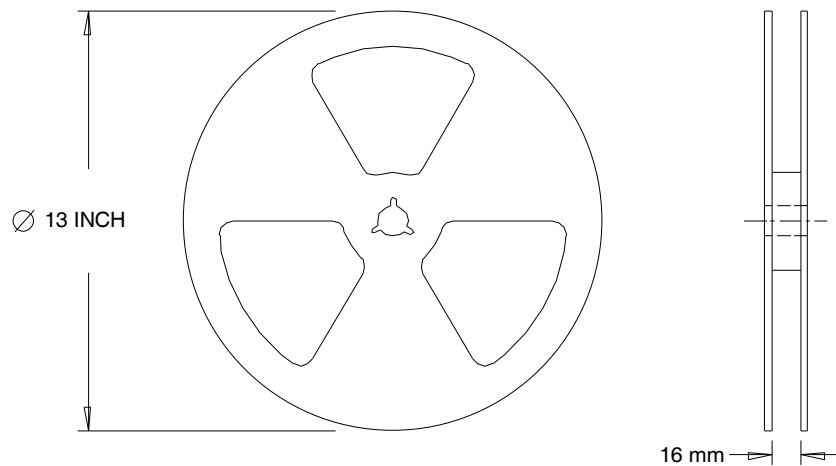
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRFR3504	Dpak	Tube	75	AUIRFR3504
		Tape and Reel	2000	AUIRFR3504TR
		Tape and Reel Left	3000	AUIRFR3504TRL
		Tape and Reel Right	3000	AUIRFR3504TRR

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<http://www.irf.com/technical-info/>

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