

## Stand-alone USB PD controller (with short-to-VBUS protection)



QFN24



QFN16

Product status link

[STUSB4710](#)

### Features

- USB power delivery (PD) controller
- Type-C attach and cable orientation detection
- Single role: provider
- Full hardware solution - no software
- I<sup>2</sup>C interface (optional connection to MCU)
- Support all USB PD profiles: up to 5 power data objects (PDO)
- Configurable start-up profiles
- Integrated V<sub>BUS</sub> voltage monitoring
- Internal and/or external V<sub>BUS</sub> discharge path
- Short -to-V<sub>BUS</sub> protections on CC pins (22 V) and V<sub>BUS</sub> pins (28 V)
- Wide power supply input:
  - V<sub>DD</sub> = [4.1 V; 22 V]
- Temperature range: -40 °C up to 105 °C
- Fully compatible with:
  - USB Type-C™ rev 1.2
  - USB PD rev 2.0
- Certification test ID: 1000125 (QFN24)

### Applications

- AC adapters and power supplies for: computer, consumer or portable consumer applications
- Smart plugs and wall adapters
- Power hubs and docking stations
- Displays
- Any Type-C source device

### Description

The **STUSB4710** is a new family of USB power delivery controllers communicating over Type-C™ configuration channel pins (CC) to negotiate a given amount of power to be sourced to an inquiring consumer device.

The **STUSB4710** addresses provider/DFP devices such as notebooks, tablets and AC adapters. The device can handle any connections to a UFP or DRP without any MCU attachment support, from the device attachment to power negotiation, including V<sub>BUS</sub> discharge and protections.

# 1 Functional description

The STUSB4710 is an autonomous USB power delivery controller optimized as a provider. It offers an open-drain GPIO interface to make direct interconnection with a power regulation stage.

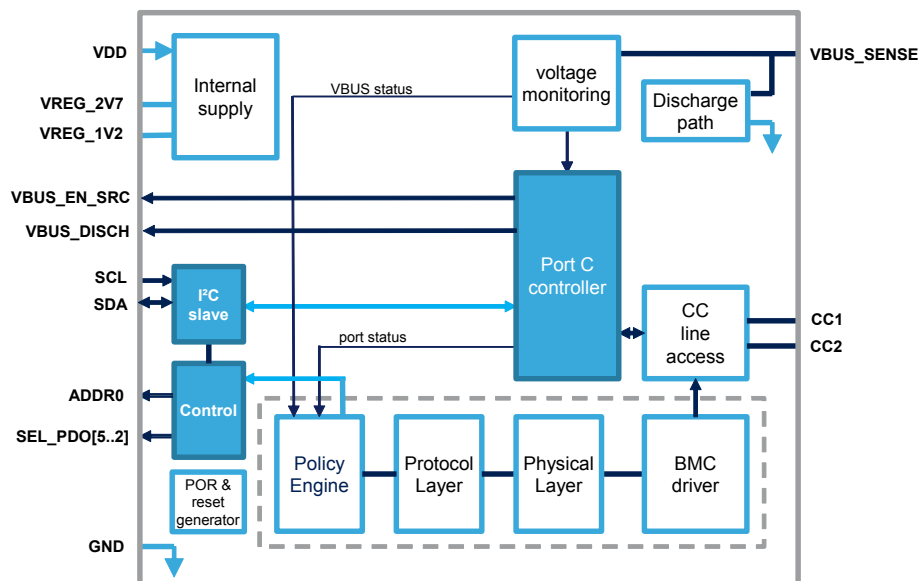
The STUSB4710 offers the benefits of a full hardware USB PD stack allowing robust and safe USB PD negotiation in line with USB PD standard. The STUSB4710 is ideal for provider applications in which digital or software intelligence is limited or missing.

The STUSB4710 main functions are:

- Detect the connection between two USB ports (attach detection)
- Establish a valid host to the device connection
- Discover and configure  $V_{BUS}$ : Type-C low, medium or high current mode
- Resolve cable orientation
- Negotiate a USB power delivery contract with a PD capable device
- Configure the power source accordingly
- Monitor  $V_{BUS}$ , manage transitions, handle protections and ensure user and device safety

Additionally, the STUSB4710 offers 5 customizable power data objects (PDOs), 5 general purpose I/Os, an integrated discharge path, and is natively robust to high voltage peaks.

**Figure 1. Functional block diagram**



## 2 Inputs/outputs

### 2.1 Pinout

Figure 2. STUSB4710AQTR pin connections (top view)

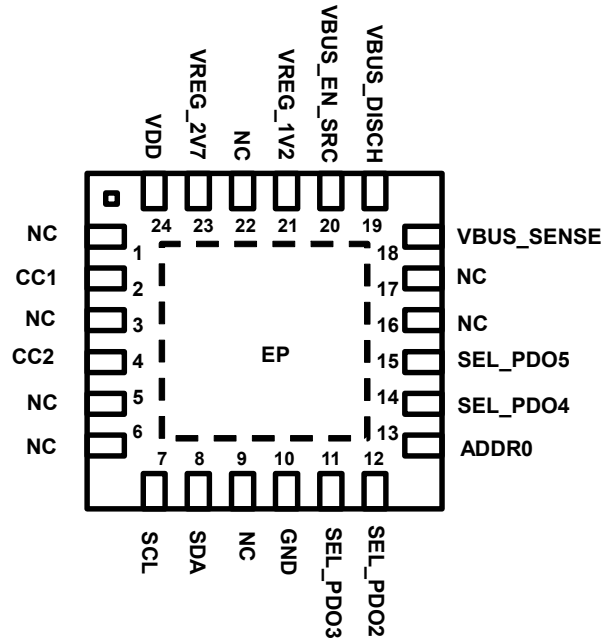
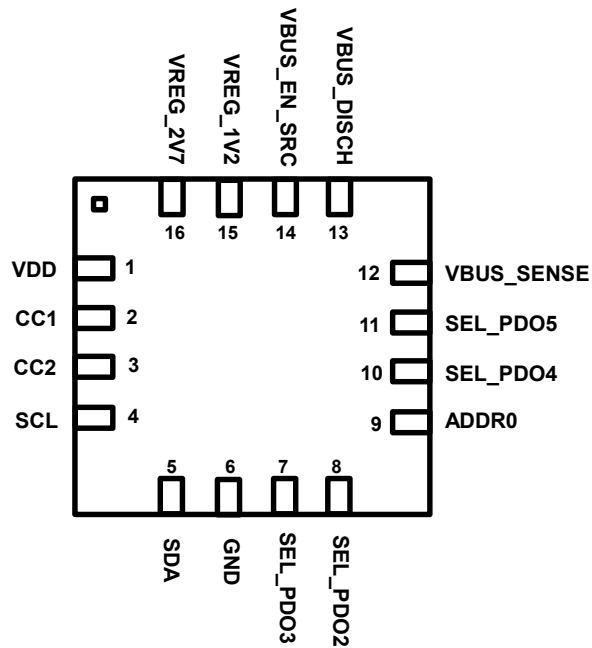


Figure 3. STUSB4710AQ1TR pin connections (top view)



## 2.2 Pin list

**Table 1. Pin function list**

Name	Type	Description	Connection
CC1	20 V analog IO	Configuration channel 1	Type-C receptacle A5
CC2	20 V analog IO	Configuration channel 2	Type-C receptacle B5
SCL	DI	I <sup>2</sup> C clock	To I <sup>2</sup> C master – ext. pull-up
SDA	DI/OD	I <sup>2</sup> C data input/output – active low open-drain	To I <sup>2</sup> C master – ext. pull-up
GND	Power	Ground	
SEL_PDO3	OD	PD03 select flag	
SEL_PDO2	OD	PD02 select flag	
ADDR0	Analog	I <sup>2</sup> C address 0 bit	
SEL_PDO4	OD	PD04 select flag	
SEL_PDO5	OD	PD05 select flag	
VBUS_SENSE	20 V AI	V <sub>BUS</sub> voltage monitoring and discharge path	From V <sub>BUS</sub>
VBUS_DISCH	Output	External discharge control signal	
VBUS_EN_SRC	20 V OD	V <sub>BUS</sub> source power path enable – active low open-drain	To switch or power system – ext. pull-up
VREG_1V2	Analog	1.2 V regulator output	1 μF typ. decoupling capacitor
VREG_2V7	Analog	2.7 V regulator output	1 μF typ. decoupling capacitor
VDD	20 V power	Main power supply (USB power line)	From V <sub>BUS</sub> (system side)
EP	Exposed pad	Exposed pad is connected to ground	To ground

**Table 2. Legend**

Type	Description
D	Digital
A	Analog
O	Output pad
I	Input pad
IO	Bidirectional pad
OD	Open drain output
PD	Pull-down
PU	Pull-up
PWR	Power supply
GND	Ground

## 2.3 Pin description

### 2.3.1 CC1 / CC2

CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable. CC1/CC2 are HiZ during reset.

### 2.3.2 I<sup>2</sup>C interface pins

**Table 3. I<sup>2</sup>C interface pin list**

Name	Description
SCL	I <sup>2</sup> C clock – needs external pull-up
SDA	I <sup>2</sup> C data – needs external pull-up

### 2.3.3 VBUS\_SENSE

This input pin is used to sense  $V_{BUS}$  presence, monitor  $V_{BUS}$  voltage and discharge  $V_{BUS}$  on USB Type-C receptacle side.

### 2.3.4 VBUS\_EN\_SRC

In source power role, this pin allows the outgoing  $V_{BUS}$  power to be enabled when the connection to a sink is established and  $V_{BUS}$  is in the valid operating range. The open-drain output allows a PMOS transistor to be driven directly. The logic value of the pin is also advertised in a dedicated I<sup>2</sup>C register bit.

### 2.3.5 VDD

$V_{DD}$  is the main power supply for applications powered by  $V_{BUS}$ .

This pin can be used to sense the voltage level of the main power supply providing  $V_{BUS}$ . It allows UVLO and OVLO voltage thresholds to be considered independently on VDD pin as additional conditions to enable the  $V_{BUS}$  power path through VBUS\_EN\_SRC pin.

### 2.3.6 GND

Ground.

### 2.3.7 ADDR0

At start-up, this pin is latched to set I<sup>2</sup>C device address 0 bit.

### 2.3.8 VREG2V7

This pin is used for external decoupling of 2.7 V internal regulator only .

Recommended decoupling capacitor: 1  $\mu$ F typ. (0.5  $\mu$ F min.; 10  $\mu$ F max.).

This pin must not be used to supply any external component.

### 2.3.9 VBUS\_DISCH

Control signal for external VBUS\_DISCH path.

### 2.3.10 SEL\_PDO [5:2]

These 4 output signals are asserted (active low) respectively when PDO2, PDO3, PDO4 and PDO5 are selected by the attached sink. These signals are used to pilot the power management unit.

## 3 Block descriptions

### 3.1 CC interface

The STUSB4710 controls the connection to the configuration channel (CC) pins, CC1 and CC2, through two main blocks, the CC line interface block and the CC control logic block.

The CC lines interface block is used to:

- Configure the termination mode on the CC pins relative to the power mode supported, i.e. pull-up for source power role
- Monitor the CC pin voltage values relative to the attachment detection thresholds
- Protect the CC pins against over voltage

The CC control logic block is used to:

- Execute the Type-C FSM relative to the Type-C power mode supported
- Determine the electrical state for each CC pins relative to the detected thresholds
- Evaluate the conditions relative to the CC pin states and  $V_{BUS}$  voltage value to transition from one state to another in the Type-C FSM
- Detect and establish a valid source-to-sink connection
- Determine the attached mode: source, accessory
- Determine cable orientation to allow external routing of the USB super speed data
- Manage  $V_{BUS}$  power capability: USB default, Type-C medium or Type-C high current mode
- Handle hardware faults

The CC control logic block implements the Type-C FSM's corresponding to source power role with accessory support.

### 3.2 BMC

This block is the physical link between USB PD protocol layer and CC pin. In TX mode, it converts the data into bi-phase mark coding (BMC), and drives the CC line to correct voltages. In RX mode, it recovers BMC data from the CC line, and converts to baseband signaling for the protocol layer.

### 3.3 Protocol layer

The protocol layer has the responsibility to manage the messages from/to the physical layer. It automatically manages the protocol receive timeouts, the message counter, the retry counter and the GoodCRC messages. It communicates with the internal policy engine.

### 3.4 Policy engine

The policy engine implements the power negotiation with the connected device according to its source role, it implements the state machine that controls protocol layer forming and scheduling the messages.

The policy engine uses the protocol layer to send/receive messages.

The policy engine interprets the device policy manager's input in order to implement policy for port and directs the protocol layer to send appropriate messages.

### 3.5 Device policy manager

The device policy manager manages the power resources.

## 3.6 VBUS power path control

### 3.6.1 VBUS monitoring

The  $V_{BUS}$  monitoring block supervises (from the  $VBUS\_SENSE$  input pin) the  $V_{BUS}$  voltage on the USB Type-C receptacle side.

This block is used to check that  $V_{BUS}$  is within a valid voltage range:

- To establish a valid source-to-sink connection according to USB Type-C standard specification
- To enable safely the  $V_{BUS}$  power path through  $VBUS\_EN\_SRC$  pin

It allows detection of unexpected  $V_{BUS}$  voltage conditions such as undervoltage or overvoltage relative to the valid  $V_{BUS}$  voltage range. When such conditions occur, the STUSB4710 reacts as follows:

- At attachment, it prevents the source-to-sink connection and the  $V_{BUS}$  power path assertion
- After attachment, it deactivates the source-to-sink connection and disables the  $V_{BUS}$  power path. The device goes into error recovery state.

The  $V_{BUS}$  voltage value is automatically adjusted at attachment and at each PDO transition. The monitoring is then disabled during  $T\_PDO\_transition$  (default 280 ms changed through NVM programming). Additionally, if a transition occurs to a lower voltage, the discharge path is activated during this time.

The valid  $V_{BUS}$  voltage range is defined from the  $V_{BUS}$  nominal voltage by a high threshold voltage and a low threshold voltage whose minimal values are respectively  $V_{BUS}+5\%$  and  $V_{BUS}-5\%$ . The nominal threshold limits can be shifted by a fraction of  $V_{BUS}$  from +1% to +15% for the high threshold voltage and from -1% to -15% for the low threshold voltage. This means the threshold limits can vary from  $V_{BUS}+5\%$  to  $V_{BUS}+20\%$  for the high limit and from  $V_{BUS}-5\%$  to  $V_{BUS}-20\%$  for the low limit.

The threshold limits are preset by default in the NVM with different shift coefficients (see [Section 8.3 Electrical and timing characteristics](#)). The threshold limits can be changed independently through NVM programming (see [Section 8.3 Electrical and timing characteristics](#)) and also by software during attachment through the I<sup>2</sup>C interface (see [Section 6 I<sup>2</sup>C register map](#)).

### 3.6.2 VBUS discharge

The monitoring block handles also the internal  $V_{BUS}$  discharge path connected to the  $VBUS\_SENSE$  input pin. The discharge path is activated at detachment, or when the device goes into the error recovery state (see [Section 3.8 Hardware fault management](#)).

The  $V_{BUS}$  discharge path is enabled by default in the NVM and can be disabled through NVM programming only (see [Section 4 User-defined startup configuration](#)). Discharge time duration ( $T\_PDO\_transition$  and  $T\_Transition$  to 0 V) are also preset by default in the NVM (see [Section 8.3 Electrical and timing characteristics](#)). The discharge time duration can be changed through NVM programming (see [Section 4 User-defined startup configuration](#)) and also by software through the I<sup>2</sup>C interface (see [Section 6 I<sup>2</sup>C register map](#)).

### 3.6.3 V<sub>BUS</sub> power path assertion

The STUSB4710 can control the assertion of the V<sub>BUS</sub> power path on USB Type-C port, directly or indirectly, through VBUS\_EN\_SRC pin.

The following table summarizes the configurations and the conditions that determine the logic value of VBUS\_EN\_SRC pin during system operation.

**Table 4. Conditions for VBUS power path assertion**

Pin	Electrical value	Operation conditions			Comment
		Attached state	V <sub>DD</sub> monitoring	V <sub>BUS</sub> monitoring	
VBUS_EN_SRC	0	Attached.SRC	VDD > UVLO if VDD_UVLO enabled and/or VDD < OVLO if VDD_OVLO enabled	V <sub>BUS</sub> within valid voltage range	The signal is asserted only if all the valid operation conditions are met.
		UnorientedDebug Accessory.SRC		if VBUS_VALID_RANGE enabled or V <sub>BUS</sub> > UVLO if VBUS_VALID_RANGE disabled	
		OrientedDebug Accessory.SRC			
HiZ		Any other state	VDD < UVLO if VDD_UVLO enabled and/or VDD > OVLO if VDD_OVLO enabled	V <sub>BUS</sub> is out of valid voltage range if VBUS_VALID_RANGE enabled or V <sub>BUS</sub> < UVLO if VBUS_VALID_RANGE disabled	The signal is de-asserted when at least one non-valid operation condition is met.

*Note:* Activation of the UVLO and OVLO threshold detections can be done through NVM programming (see Section 4 User-defined startup configuration) and also by software through the I<sup>2</sup>C interface (see Section 6 I<sup>2</sup>C register map). When the UVLO and/or OVLO threshold detection is activated, the VBUS\_EN\_SRC pin is asserted only if the device is attached and the valid threshold conditions on V<sub>DD</sub> are met. Once the VBUS\_EN\_SRC pin is asserted, the V<sub>BUS</sub> monitoring is done on VBUS\_SENSE pin instead of the V<sub>DD</sub> pin.

### 3.7 High voltage protection

The STUSB4710 can be safely used in systems or connected to systems that handle high voltage on the V<sub>BUS</sub> power path. The device integrates an internal circuitry on the CC pins that tolerates high voltage and ensures a protection up to 22 V in case of unexpected short circuit with V<sub>BUS</sub> or in case of connection to a device supplying high voltage on V<sub>BUS</sub>.



### 3.8 Hardware fault management

The STUSB4710 handles hardware fault conditions related to the device itself and the  $V_{BUS}$  power path during system operation.

When such conditions occur, the circuit goes into a transient error recovery state named ErrorRecovery in the Type-C FSM. When entering in this state, the device de-asserts the  $V_{BUS}$  power path by disabling the  $V_{BUS\_EN\_SRC}$  pin, and it removes the terminations from the CC pins during several tens of milliseconds. Then, it transitions to the unattached source state.

The STUSB4710 goes into error recovery state when at least one condition listed below is met:

- If an overtemperature is detected, the “THERMAL\_FAULT” flag is asserted.
- If an internal pull-up voltage on CC pins is below UVLO threshold, the “VPU\_VALID” flag is asserted.
- If an overvoltage is detected on the CC pins, the “VPU\_OVP\_FAULT” flag is asserted.
- If the  $V_{BUS}$  voltage is out of the valid voltage range during attachment, the “VBUS\_VALID” flag is asserted.
- If an undervoltage is detected on the  $V_{DD}$  pin during attachment when UVLO detection is enabled, the “VDD\_UVLO\_DISABLE” flag is asserted.
- If an overvoltage is detected on the  $V_{DD}$  pin during attachment when OVLO detection is enabled, the “VDD\_OVLO\_DISABLE” flag is asserted.

The I<sup>2</sup>C register bits mentioned above in quotes give either the state of the hardware fault when it occurs or the setting condition to detect the hardware fault.

### 3.9 Accessory mode detection

The STUSB4710 supports the detection of audio accessory mode and debug accessory mode as defined in the USB Type-C standard specification source power role with accessory support.

#### 3.9.1 Audio accessory mode detection

The STUSB4710 detects an audio accessory device when both the CC1 and CC2 pins are pulled down to ground by a  $R_a$  resistor from the connected device. The audio accessory detection is advertised through the CC\_ATTACHED\_MODE bits of the I<sup>2</sup>C register CC\_CONNECTION\_STATUS.

#### 3.9.2 Debug accessory mode detection

The STUSB4710 detects a connection to a debug and test system (DTS) when it operates either in sink power role or source power role. The debug accessory detection is advertised by the DEBUG1 and DEBUG2 pins as well as through the CC\_ATTACHED\_MODE bits of the I<sup>2</sup>C register CC\_CONNECTION\_STATUS.

In source power role, a debug accessory device is detected when both the CC1 and CC2 pins are pulled down to ground by a  $R_d$  resistor from the connected device. The orientation detection is performed in two steps as described in the table below. The DEBUG2 pin is asserted to advertise the DTS detection. The orientation detection is advertised through the TYPEC\_FSM\_STATE bits of the I<sup>2</sup>C register CC\_OPERATION\_STATUS.

## 4 User-defined startup configuration

### 4.1 Parameter overview

The STUSB4710 has a set of user-defined parameters that can be customized by NVM re-programming and/or by software through I<sup>2</sup>C interface. It allows changing the preset configuration of USB Type-C and PD interface and to define a new configuration to meet specific customer requirements addressing various applications, use cases or specific implementations.

The NVM re-programming overrides the initial default setting to define a new default setting that is used at power-up or after a reset. The default value is copied at power-up, or after a reset, from the embedded NVM into dedicated I<sup>2</sup>C register bits. The NVM re-programming is possible few times with a customer password.

**Table 5. PDO configurations in NVM**

Feature	Parameter	Value	Default
PDO1	Voltage	5 V	5 V
	Current	Configurable – defined by PDO1_I [3:0]	3 A
PDO2	Voltage	Configurable – defined by PDO2_V [1:0]	9 V
	Current	Configurable – defined by PDO2_I [3:0]	3 A
PDO3	Voltage	Configurable – defined by PDO3_V [1:0]	12 V
	Current	Configurable – defined by PDO3_I [3:0]	3 A
PDO4	Voltage	Configurable – defined by PDO4_V [1:0]	15 V
	Current	Configurable – defined by PDO4_I [3:0]	3 A
PDO5	Voltage	Configurable – defined by PDO5_V [1:0]	20 V
	Current	Configurable – defined by PDO5_I [3:0]	2.25 A

When a default value is changed during system boot by software, the new settings apply as long as the STUSB4710 is being run and until it is changed again. But after power-off and power-up, or after a hardware reset, the STUSB4710 takes back default values defined in the NVM.

### 4.2 PDO – voltage configuration in NVM

PDO2\_V [1:0], PDO3\_V [1:0], PDO4\_V [1:0] and PDO5\_V [1:0] can be configured with the following values:

**Table 6. PDO NVM voltage configuration**

Value	Configuration
2b00	9 V
2b01	15 V
2b10	PDO_FLEX_V1
2b11	PDO_FLEX_V2

PDO\_FLEX\_V1 and PDO\_FLEX\_V2 are defined in a specific 10-bit register, value being expressed in 50 mV units.

For instance:

- PDO\_FLEX\_V1 = 10b0100100010 → 14.5 V
- PDO\_FLEX\_V2 = 10b0110000110 → 19.5 V

### 4.3 PDO – current configuration in NVM

PDO1\_I [3:0], PDO2\_I [3:0], PDO3\_I [3:0], PDO4\_I [3:0] and PDO5\_I [3:0] can be configured with the following fixed values:

**Table 7. PDO NVM current configuration**

Value	Configuration
4b0000	PDO_FLEX_I
4b0001	1.50 A
4b0010	1.75 A
4b0011	2.00 A
4b0100	2.25 A
4b0101	2.50 A
4b0110	2.75 A
4b0111	3.00 A
4b1000	3.25 A
4b1001	3.50 A
4b1010	3.75 A
4b1011	4.00 A
4b1100	4.25 A
4b1101	4.50 A
4b1110	4.75 A
4b1111	5.00 A

PDO\_FLEX\_I is defined in a specific 10-bit register, value being expressed in 10 mA units. For instance:

- PDO\_FLEX\_I = 10b0011100001 → 2.25 A

### 4.4 Monitoring configuration in NVM

- T\_PDO\_Transition can be configured from 20 to 300 ms by increments of 20 ms (0 is not recommended). Default value is 240 ms.
- T\_Transition\_to\_0V can be configured from 84 to 1260 ms by increments of 84 ms (0 is not recommended). Default value is 168 ms.
- Vshift\_High can be configured from (5 to 20%). Default value ranges from 8% to 12%.
- Vshift\_Low can be configured from (5 to 20%). Default value is 10% for all PDO.

### 4.5 Discharge configuration in NVM

Both internal and external discharge paths are enabled by default. VBUS\_DISCH control pin is configured to drive a PMOS by default (active low).

## 5 I<sup>2</sup>C interface

### 5.1 Read and write operations

The I<sup>2</sup>C interface is used to configure, control and read the status of the device. It is compatible with the Philips I<sup>2</sup>C Bus® (version 2.1). The I<sup>2</sup>C is a slave serial interface based on two signals:

- SCL - serial clock line: input clock used to shift data
- SDA - serial data line: input/output bidirectional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity.

The bidirectional data line support transfers up to 400 Kbit/s (fast mode). The data are shifted to and from the chip on the SDA line, MSB first.

The first bit must be high (START) followed by the 7-bit device address and the read/write control bit.

Two 7-bit device addresses are available for the STUSB4710 thanks to external programming of DevADDR0, through ADDR0, pin setting. It allows two STUSB4710 devices to be connected on the same I<sup>2</sup>C bus.

ADDR is not available for all configurations.

The device address format:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DevADDR6	DevADDR5	DevADDR4	DevADDR3	DevADDR2	DevADDR1	DevADDR0	R/W
0	1	0	1	0	0	ADDR0	0/1

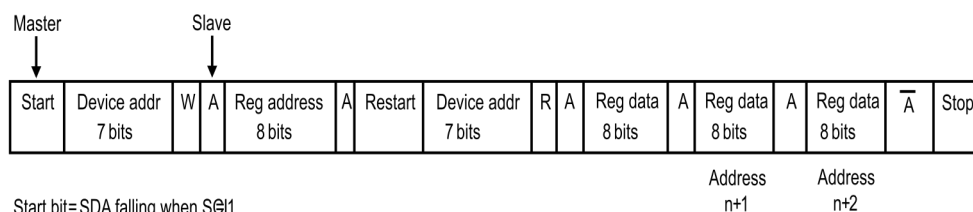
The register address format:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RegADDR7	RegADDR6	RegADDR5	RegADDR4	RegADDR3	RegADDR2	RegADDR1	RegADDR0

The register data format:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

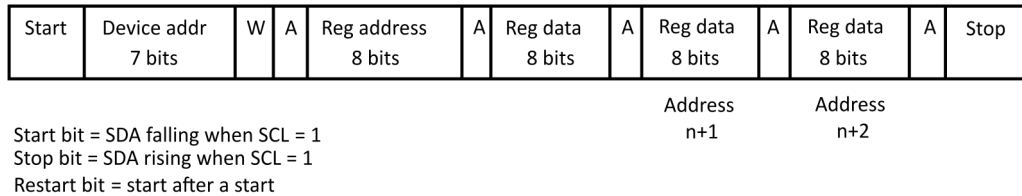
**Figure 4. Read operation**



Start bit=SDA falling when S<sub>0</sub>1  
 Stop bit=SDA rising when S<sub>0</sub>1  
 Restart bit= start after a start  
 Acknowledge=SDA forced low during a SCL clock

Address  
n+1      Address  
n+2

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**Figure 5. Write operation**


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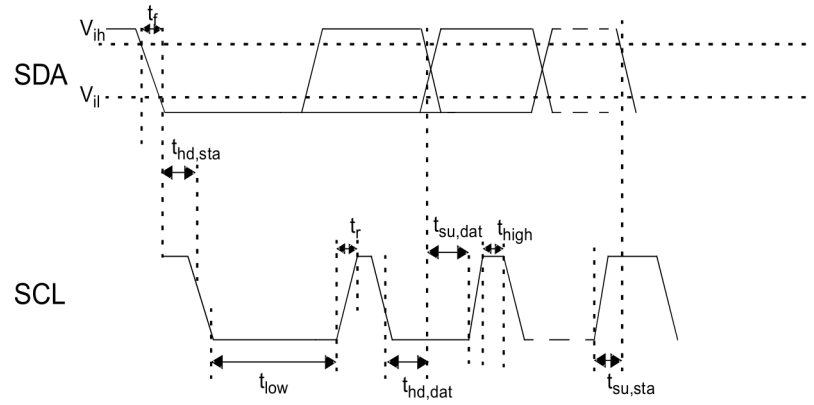
## 5.2 Timing specifications

 The device uses a standard slave I<sup>2</sup>C channel at speed up to 400 kHz.

**Table 8. I<sup>2</sup>C timing parameters - VDD = 5 V**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$F_{scl}$	SCL clock frequency	0	-	400	kHz
$t_{hd,sta}$	Hold time (repeated) START condition	0.6	-	-	$\mu$ s
$t_{low}$	LOW period of the SCL clock	1.3	-	-	$\mu$ s
$t_{high}$	HIGH period of the SCL clock	0.6	-	-	$\mu$ s
$t_{su,dat}$	Setup time for repeated START condition	0.6	-	-	$\mu$ s
$t_{hd,dat}$	Data hold time	0.04	-	0.9	$\mu$ s
$t_{su,dat}$	Data setup time	100	-	-	$\mu$ s
$t_r$	Rise time of both SDA and SCL signals	$20 + 0.1 C_b$	-	300	ns
$t_f$	Fall time of both SDA and SCL signals	$20 + 0.1 C_b$	-	300	ns
$t_{su,sto}$	Setup time for STOP condition	0.6	-	-	$\mu$ s
$t_{buf}$	Bus free time between a STOP and START condition	1.3	-	-	$\mu$ s
$C_b$	Capacitive load for each bus line	-	-	400	pF

**Figure 6. I<sup>2</sup>C timing diagram**



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## 6 I<sup>2</sup>C register map

**Table 9. STUSB4710 register map overview**

Address	Register name	Access	Description
00h to 0Ah	Reserved	RO	Do not use
0Bh	ALERT_STATUS	RC	Alert register linked to transition registers
0Ch	ALERT_STATUS_MASK_CTRL	R/W	Interrupt mask on ALERT_STATUS register
0Dh	CC_CONNECTION_STATUS_TRANS	RC	Alerts on transition in CC_CONNECTION_STATUS register
0Eh	CC_CONNECTION_STATUS	RO	CC connection status
0Fh	MONITORING_STATUS_TRANS	RC	Alerts on transition in MONITORING_STATUS register
10h	MONITORING_STATUS	RO	Gives status on V <sub>BUS</sub> voltage monitoring
11h	Reserved	RO	Do not use
12h	HW_FAULT_STATUS_TRANS	RC	Alerts on transition in HW_FAULT_STATUS register
13h	HW_FAULT_STATUS	RO	Hardware faults status
14h to 17h	Reserved	RO	Do not use
18h	CC_CAPABILITY_CTRL	R/W	Allows the CC capabilities to be changed
19h to 22h	Reserved	RO	Do not use
23h	RESET_CTRL	R/W	Controls the device reset by software
24h	Reserved	RO	Do not use
25h	VBUS_DISCHARGE_TIME_CTRL	R/W	Parameters defining V <sub>BUS</sub> discharge time
26h	VBUS_DISCHARGE_CTRL	R/W	Controls the V <sub>BUS</sub> discharge path
27h	VBUS_ENABLE_STATUS	RO	V <sub>BUS</sub> power path activation status
2Eh	VBUS_MONITORING_CTRL	R/W	Allows the monitoring conditions of V <sub>BUS</sub> voltage to be changed
19h to 1Eh	Reserved	RO	Do not use
71h	SRC_PDO1	R/W	PDO1 capabilities configuration
75h	SRC_PDO2	R/W	PDO2 capabilities configuration
79h	SRC_PDO3	R/W	PDO3 capabilities configuration
7Dh	SRC_PDO4	R/W	PDO4 capabilities configuration
81h	SRC_PDO5	R/W	PDO5 capabilities configuration
91h	SRC_RDO	RO	PDO request status

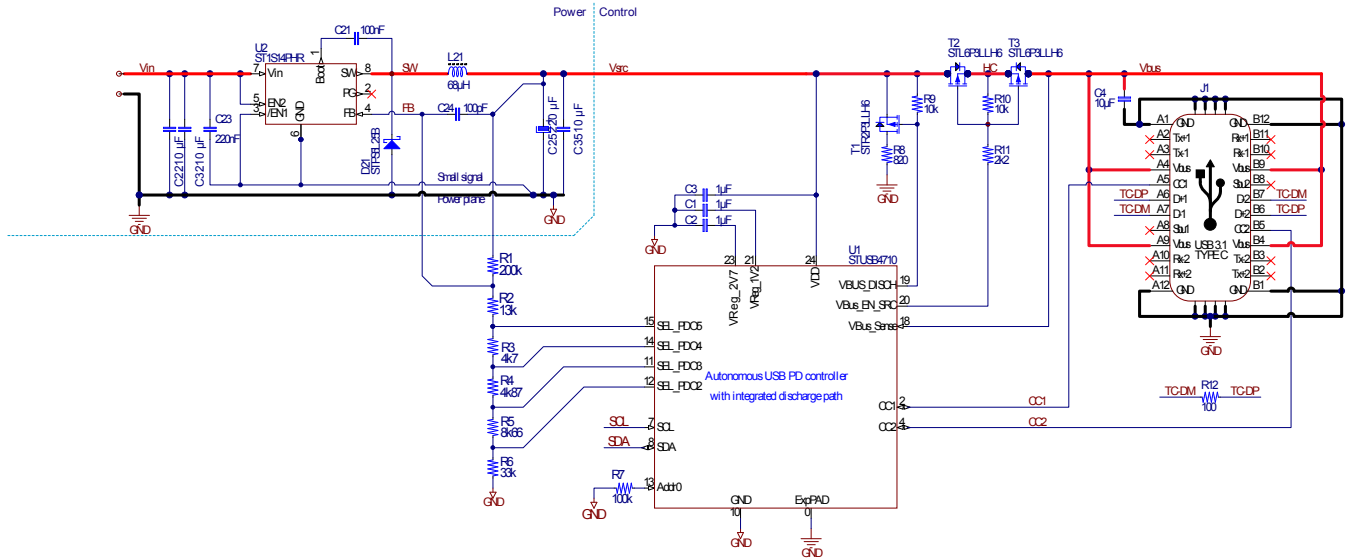
**Table 10. Register access legend**

Access code	Expanded name	Description
RO	Read only	Register can be read only
R/W	Read / write	Register can be read or written
RC	Read and clear	Register can be read and is cleared after read



## 7 Typical use cases

### 7.1 Power supply – buck topology

**Figure 7. Power supply - buck topology**


The STUSB4710 offers the possibility to have up to 5 PDOs using (GPIO0 to GPIO3).

For example PDO1:5V 3A (no GPIO grounded), PDO2:9V 3A (GPIO0 to GND), PDO3:12V 3A (GPIO1 to GND), PDO4:15 volt (GPIO2 to GND), PDO5: 20 volt GPIO3 to GND).

**Table 11. Resistor value**

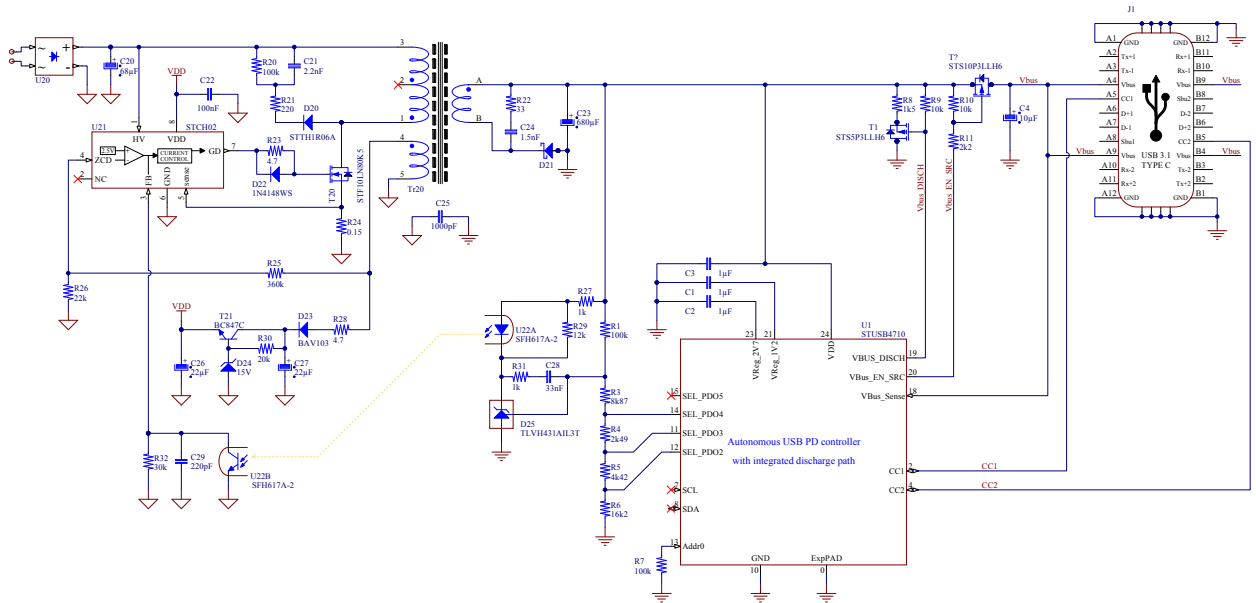
PDO	V <sub>OUT</sub>	Computation	Resistor value (Ω)
-	-	R1	200 k
5	20	$R_2 = \frac{R_1 \cdot 1.22}{V_{OUT} - 1.22}$ (1)	13 k
4	15	$R_3 = \frac{R_1 \cdot 1.22}{V_{OUT} - 1.22} - R_2$ (2)	4k7
3	12	$R_4 = \frac{R_1 \cdot 1.22}{V_{OUT} - 1.22} - R_2 - R_3$ (3)	4k87
2	9	$R_5 = \frac{R_1 \cdot 1.22}{V_{OUT} - 1.22} - R_3 - R_4$ (4)	8k66
1	5	$R_6 = \frac{R_1 \cdot 1.22}{V_{OUT} - 1.22} - R_2 - R_3 - R_4 - R_5$ (5)	33 k

## 7.2 Power supply – flyback topology

The STUSB4710 offers the possibility to have up to 5 PDOs using GPIO0 to GPIO3.

For example PDO1 (5 V; 3 A) (no Sel\_PDO grounded), PDO2 (9 V; 3 A) (GPIO0 to GND), PDO3 (15 V; 3 A) (GPIO1 to GND).

**Figure 8. Flyback topology**



**Table 12. Resistor value**

PDO	V <sub>OUT</sub>	Computation	Resistor value (Ω)
-	-	R1	100 k
4	15	$R_3 = \frac{R_1 \cdot 1.24}{V_{OUT} - 1.24}$ (6)	8k87
3	12	$R_4 = \frac{R_1 \cdot 1.24}{V_{OUT} - 1.24} - R_3$ (7)	2k49
2	9	$R_5 = \frac{R_1 \cdot 1.24}{V_{OUT} - 1.24} - R_3 - R_4$ (8)	4k42
1	5	$R_6 = \frac{R_1 \cdot 1.24}{V_{OUT} - 1.24} - R_3 - R_4 - R_5$ (9)	16k2

## 8 Electrical characteristics

### 8.1 Absolute maximum ratings

All voltages are referenced to GND.

**Table 13. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage	28	V
$V_{CC1}, V_{CC2}$	High voltage on CC pins	22	V
$V_{VBUS\_EN\_SRC}$ $V_{VBUS\_SENSE}$ $V_{VBUS\_DISCH}$	High voltage on $V_{BUS}$ pins	28	V
$V_{SCL}, V_{SDA}, V_{SEL\_PDO[5:2]}$	Operating voltage on I/O pins	-0.3 to 6	V
$T_{STG}$	Storage temperature	-55 to 150	°C
$T_J$	Maximum junction temperature	145	°C
ESD	HBM	4	kV
	CDM	1.5	

### 8.2 Operating conditions

**Table 14. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage	4.1 to 22	V
$V_{CC1}, V_{CC2}$	CC pins <sup>(1)</sup>	-0.3 to 5.5	V
$V_{VBUS\_SENSE}$ $V_{VBUS\_EN\_SRC}$ $V_{VBUS\_DISCH}$	High voltage pins	0 to 22	V
$V_{SCL}, V_{SDA}, V_{SEL\_PDO[5:2]}$	Operating voltage on I/O pins	0 to 4.5	V
$T_A$	Operating temperature	-40 to 105	°C

1. Transient voltage on CC1 and CC2 pins are allowed to go down to -0.3 during BMC communication from connected devices.

### 8.3 Electrical and timing characteristics

Unless otherwise specified:  $V_{DD} = 5\text{ V}$ ,  $T_A = +25\text{ }^\circ\text{C}$ , all voltages are referenced to GND.

**Table 15. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{DD(SRC)}$	Current consumption	Device Idle as SOURCE (not connected, no communication)				
		$V_{DD} @ 5.0\text{ V}$	–	188	–	$\mu\text{A}$
$I_{STDBY}$	Standby current consumption	Device standby (not connected, low power)				
		$V_{DD} @ 5.0\text{ V}$	–	53	–	$\mu\text{A}$
CC1 and CC2 pins						
$I_{P-USB}$	CC current sources	CC pin voltage	-20%	80	+20%	$\mu\text{A}$
$I_{P-1.5}$		$V_{CC} = -0.3\text{ to }2.6\text{ V}$	-8%	180	+8%	$\mu\text{A}$
$I_{P-3.0}$		$-40^\circ < T_A < +105^\circ$	-8%	330	+8%	$\mu\text{A}$
$V_{CCO}$	CC open pin voltage	CC unconnected, $V_{DD}=3.0\text{ to }5.5\text{ V}$	2.75	–	–	V
$R_d$	CC pull-down resistors	$-40^\circ < T_A < +105^\circ$	-10%	5.1	+10%	k $\Omega$
$V_{CCDB-1.5}$	CC pin voltage in dead battery condition	External $I_P=180\text{ }\mu\text{A}$ applied into CC	–	–	1.2	V
$V_{CCDB-3.0}$		External $I_P=330\text{ }\mu\text{A}$ applied into CC ( $V_{DD} = 0$ , dead battery function enabled)	–	–	2	V
$R_{INCC}$	CC input impedance	Pull-up and pull-down resistors off	200	–	–	k $\Omega$
$V_{TH0.2}$	Detection threshold 1	Max. $R_a$ detection by DFP at $I_P = I_{P-USB}$ , min. $I_{P-USB}$ detection by UFP on $R_d$ , min. CC voltage for connected UFP	0.15	0.2	0.25	V
$V_{TH0.4}$	Detection threshold 2	Max $R_a$ detection by DFP at $I_P = I_{P-1.5}$	0.35	0.4	0.45	V
$V_{TH0.66}$	Detection threshold 3	Min $I_{P-1.5}$ detection by UFP on $R_d$	0.61	0.66	0.7	V
$V_{TH0.8}$	Detection threshold 4	Max. $R_a$ detection by DFP at $I_P = I_{P-3.0}$	0.75	0.8	0.85	V
$V_{TH1.23}$	Detection threshold 5	Min. $I_{P-3.0}$ detection by UFP on $R_d$	1.16	1.23	1.31	V
$V_{TH1.6}$	Detection threshold 6	Max $R_d$ detection by DFP at $I_P = I_{P-USB}$ and $I_P = I_{P-1.5}$	1.5	1.6	1.65	V
$V_{TH2.6}$	Detection threshold 7	Max. $R_d$ detection by DFP at $I_{P-3.0}$ , max. CC voltage for connected UFP	2.45	2.6	2.75	V
V <sub>BUS</sub> monitoring and driving						
$V_{THUSB}$	V <sub>BUS</sub> presence threshold		3.8	3.9	4	V
$V_{TH0V}$	V <sub>BUS</sub> safe 0V threshold (vSafe0V)	Programmable threshold (from 0.6 to 1.8 V) Default $V_{TH0V} = 0.6\text{ V}$	0.5	0.6	0.7	V
			0.8	0.9	1	
			1.1	1.2	1.3	

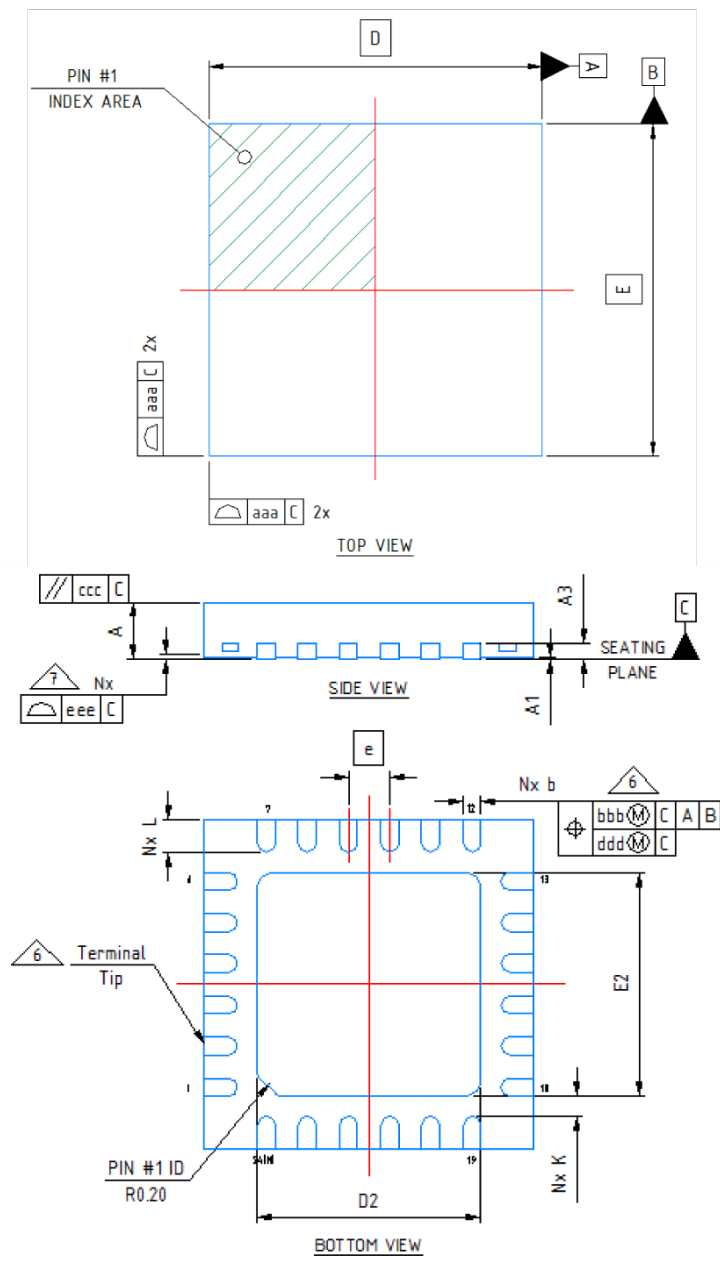
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{TH0V}$	$V_{BUS}$ safe 0V threshold (vSafe0V)	Programmable threshold (from 0.6 to 1.8 V) Default $V_{TH0V} = 0.6$ V	1.7	1.8	1.9	V
$R_{DISUSB}$	$V_{BUS}$ discharge resistor		600	700	800	$\Omega$
$T_{DISUSB}$	$V_{BUS}$ discharge time to 0 V	Default $T_{DISUSB} = 840$ ms. The coefficient $T_{DISPARAM}$ is programmable by NVM	$70 * T_{DISPARAM}$	$84 * T_{DISPARAM}$	$100 * T_{DISPARAM}$	ms
$T_{DISUSB}$	$V_{BUS}$ discharge time to PDO	Default $T_{DISUSB} = 200$ ms The coefficient $T_{DISPARAM}$ is programmable by NVM	$20 * T_{DISPARAM}$	$24 * T_{DISPARAM}$	$28 * T_{DISPARAM}$	ms
$V_{MONUSBH}$	$V_{BUS}$ monitoring high voltage threshold	$V_{BUS} =$ nominal target value Default $V_{MONUSBH} = V_{BUS} + 10\%$ The threshold limit is programmable by NVM from $V_{BUS} + 5\%$ to $V_{BUS} + 20\%$	–	$V_{BUS} + 10\%$	–	V
$V_{MONUSBL}$	$V_{BUS}$ monitoring low voltage threshold	$V_{BUS} =$ nominal target value Default $V_{MONUSBL} = V_{BUS} - 10\%$ The threshold limit is programmable by NVM from $V_{BUS} - 20\%$ to $V_{BUS} - 5\%$	–	$V_{BUS} - 10\%$	–	V
Digital input/output (SCL, SDA)						
$V_{IH}$	High level input voltage		1.2	–	–	V
$V_{IL}$	Low level input voltage		–	–	0.35	V
$V_{OL}$	Low level output voltage	$I_{oh} = 3$ mA	–	–	0.4	V
20 V open-drain outputs (VBUS_EN_SRC)						
$V_{OL}$	Low level output voltage	$I_{oh} = 3$ mA	–	–	0.4	V

## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 QFN24 EP 4x4 mm package information

Figure 9. QFN24 EP 4x4 mm package outline



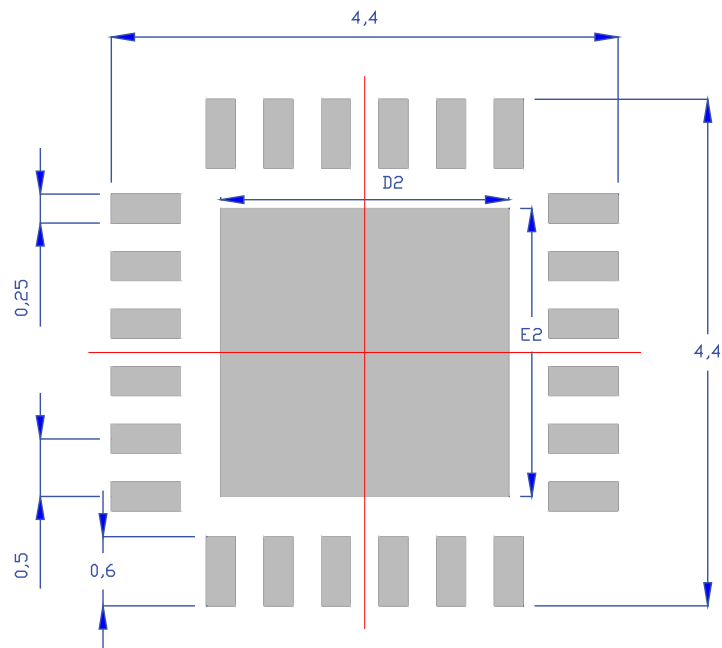
**Table 16. QFN24 EP 4x4 mm package mechanical data**

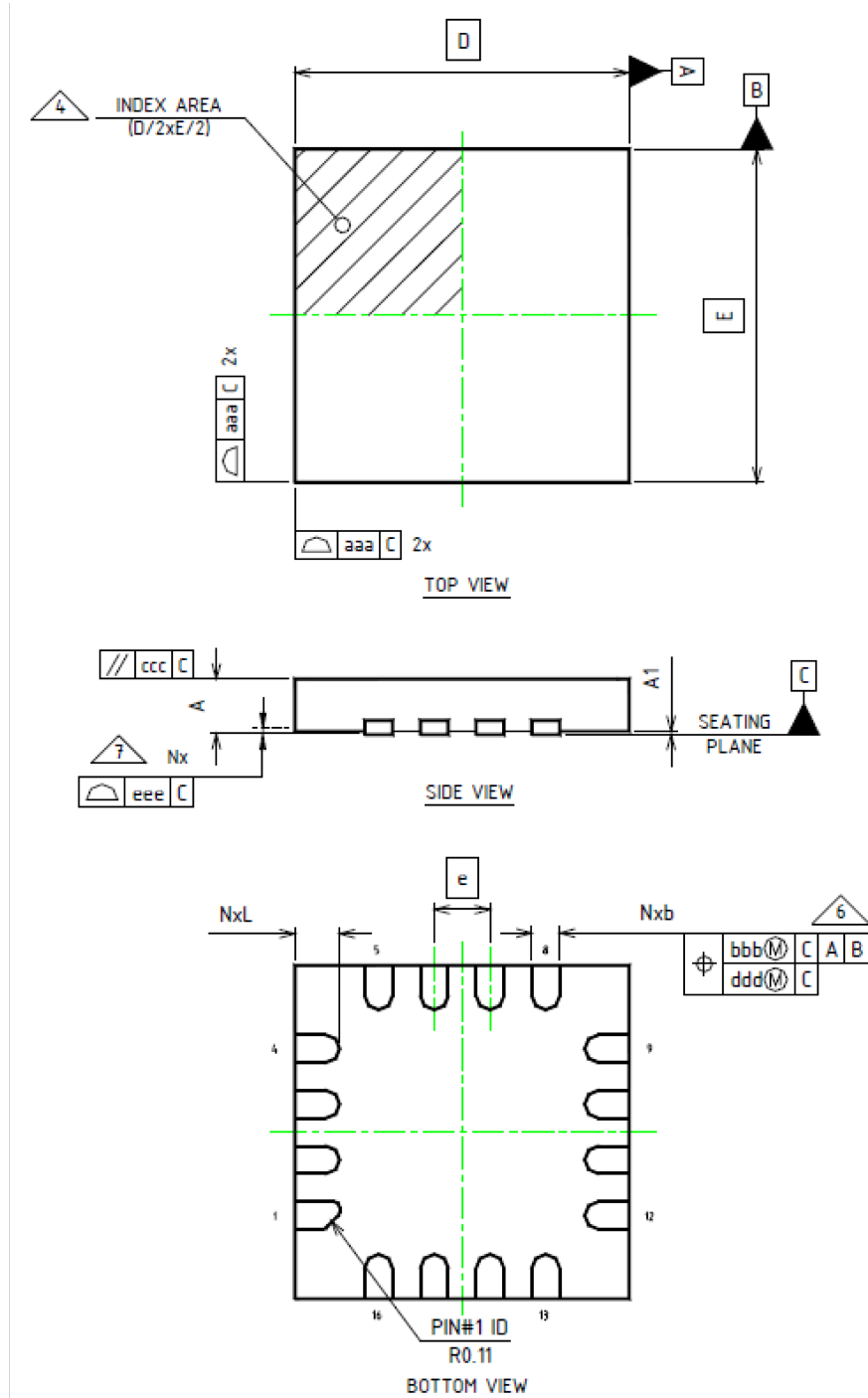
Symbol	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 Ref.	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.70	2.80
E	3.90	4.00	4.10
E2	2.55	2.70	2.80
e		0.50	
k	0.20	-	-
L	0.30	0.40	0.50

**Table 17. Tolerance of form and position**

Symbol	mm
aaa	0.05
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08

**Figure 10. QFN24 EP 4x4 mm recommended footprint**



**9.2 QFN 16 (3x3 mm), pitch 0.50 package information**
**Figure 11. QFN 16 (3x3 mm) package outline**


- Note:
- *Nxb* means *N* pads with *b* width
  - *NxL* means *N* pads with *L* length



**Table 18. QFN 16 (3x3 mm) mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	0.5		0.65
A1	0		0.05
b	0.18	0.25	0.30
D	3.00 bsc		
E	3.00 bsc		
e		0.50	
L	0.40	0.50	0.60
aaa			0.15
bbb			0.10
ccc			0.10
ddd			0.05
eee			0.08
n		16	
nD		4	
nE		4	

**Note:**

1. *N is the total number of terminals*
2. *nD and nE refer to the number of terminals on D and E side respectively*
3. *Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured on that radius area*

### 9.3 Thermal information

**Table 19. Thermal information**

Package	Symbol	Parameter	Value	Unit
QFN24 EP	$R_{\theta JA}$	Junction-to-ambient thermal resistance	37	°C/W
	$R_{\theta JC}$	Junction-to-case thermal resistance	5	
QFN16	$R_{\theta JA}$	Junction-to-ambient thermal resistance	78	
	$R_{\theta JC}$	Junction-to-case thermal resistance	30	

## 9.4 Packing information

Figure 12. Reel information

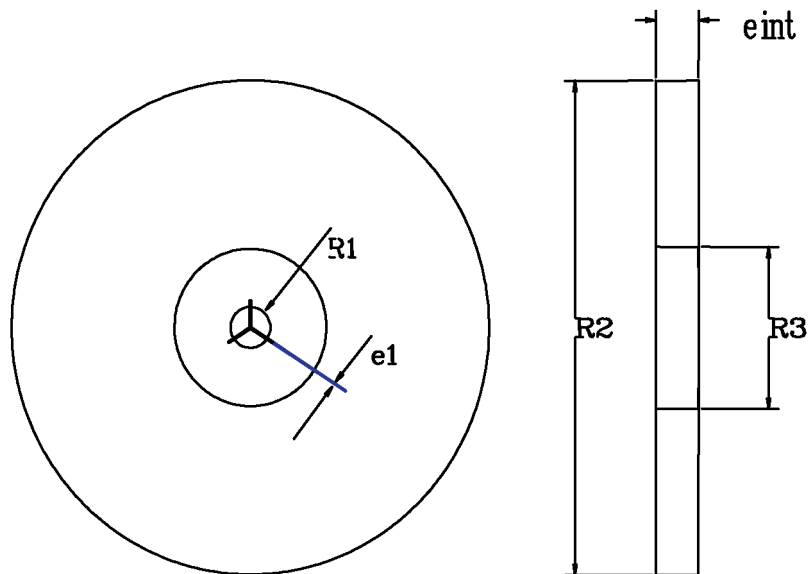


Table 20. Tape dimensions

Package	Pitch	Carrier width	Reel
QFN 4x4 - 24L	8 mm	12 mm	13"

## 10 Terms and abbreviations

**Table 21. List of terms and abbreviations**

Term	Description
Accessory modes	Audio adapter accessory mode. It is defined by the presence of Ra/Ra on the CC1/CC2 pins.
	Debug accessory mode. It is defined by the presence of Rd/Rd on CC1/CC2 pins in source power role or Rp/Rp on CC1/CC2 pins in sink power role.
DFP	Downstream facing port, associated with the flow of data in a USB connection. Typically, the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources $V_{BUS}$ and $V_{CONN}$ and supports data.
DRP	Dual-role port. A port that can operate as either a source or a sink. The port role may be changed dynamically.
Sink	Port asserting Rd on the CC pins and consuming power from the $V_{BUS}$ ; most commonly a device.
Source	Port asserting Rp on the CC pins and providing power over the $V_{BUS}$ ; usually a host or hub DFP.
UFP	Upstream facing port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks the $V_{BUS}$ and supports data.

## 11 Ordering information

**Table 22. Ordering information**

Order code	Description	Package	Marking
STUSB4710AQ1TR	Autonomous USB PD controller (provider)	QFN16 (3x3 mm)	471A
STUSB4710AQTR		QFN24 EP (4x4 mm)	4710A

## Revision history

**Table 23. Document revision history**

Date	Version	Changes
05-Apr-2017	1	Initial release.
12-Jul-2017	2	Updated Features, Table 2: "Pin functions list", Section 2.3.10: "SEL_PDO [5:2]", Section 4.4: "Monitoring configuration in NVM", Section 4.5: "Discharge configuration in NVM", Section 5.1: "Read and write operations", Table 15: "Operating conditions ", Table 20: "Thermal information", and Section 7.2: "Power supply – flyback topology".
23-Aug-2017	3	Updated Table 1: "Device summary table"
13-Nov-2017	4	Updated the features and the device summary table in cover page. Minor text changes throughout the document.
24-Mar-2021	5	Added Section 11 Ordering information. Updated QFN16 (3x3x0.55) package information and Section 9.1 QFN24 EP 4x4 mm package information.
22-Jul-2021	6	Updated the title of figure 2 and figure 3.
20-Oct-2022	7	Updated Section 9.2 QFN 16 (3x3 mm), pitch 0.50 package information.
15-Dec-2022	8	Updated <a href="#">Section 3.9.2 Debug accessory mode detection</a> .

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