Precision Digital Power Monitor

ISL28022

The ISL28022 is a bi-directional high-side and low-side digital current sense and voltage monitor with serial interface. The device monitors current and voltage and provides the results digitally along with calculated power. The ISL28022 provides tight accuracy of less than 0.3% for both voltage and current monitoring over the entire input range. The digital power monitor has configurable fault thresholds and measurable ADC gain ranges.

The ISL28022 handles common-mode input voltage ranging from 0V to 60V. The wide range permits the device to handle telecom, automotive and industrial applications with minimal external circuitry. Both high and low-side ground sensing applications are easily handled with the flexible architecture.

The ISL28022 consumes an average current of just 700µA and is available in the 10 Ld MSOP package. The ISL28022 is also offered in a space saving 16 Ld QFN package. The part operates over the extended temperature range from -40°C to +125°C.

Features

- Bus voltage sense range . . . . . 0V to 60V
- 16-bit ∑ΔADC monitors current and voltage
- Voltage measuring error . . . . . <0.3%
- Current measuring error . . . . . <0.3%
- Handles negative system voltage
- Over/undervoltage and current fault monitoring
- I^2C/SMBus interface
- Wide V_{CC} range . . . . . 3V to 5.5V
- ESD (HBM). 8kV
- Supports high speed I^2C 3.4MHz

Applications

- Routers and servers
- DC/DC, AC/DC converters
- Battery management/charging
- Automotive power
- Power distribution
- Medical and test equipment

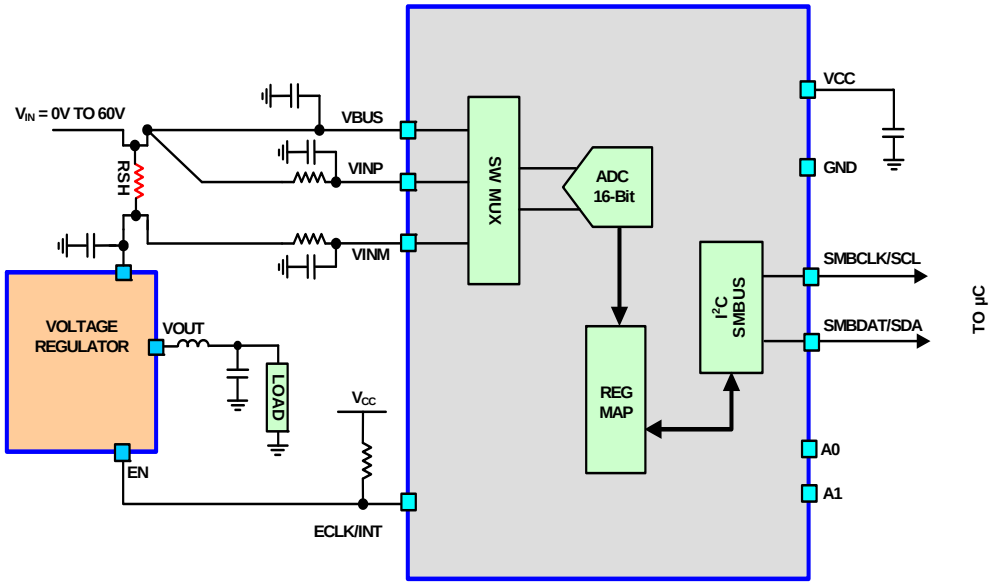

FIGURE 1. TYPICAL APPLICATION

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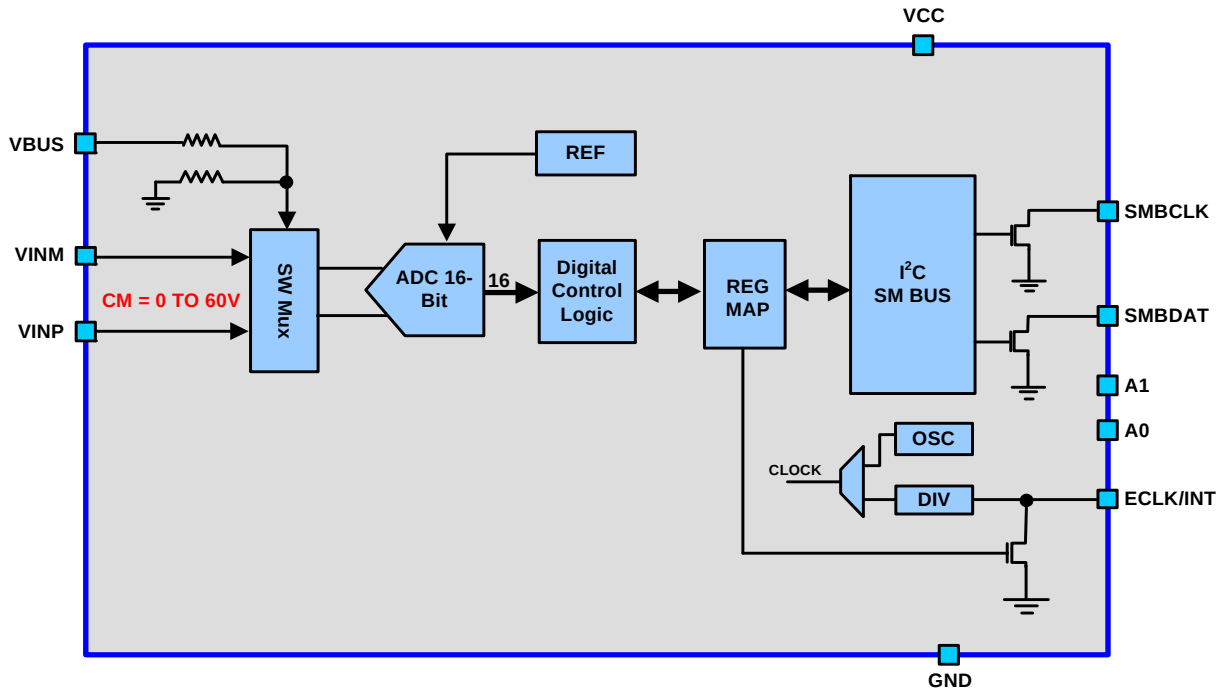
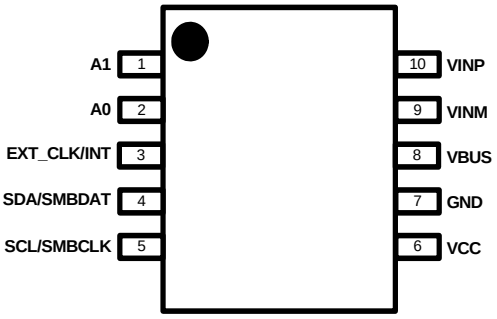
Block Diagram

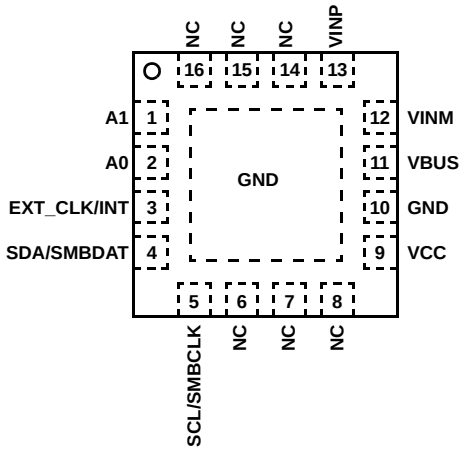


Pin Configurations

ISL28022
(10 LD MSOP)
TOP VIEW



ISL28022
(16 LD QFN)
TOP VIEW



Pin Descriptions

MSOP PIN NUMBER	QFN PIN NUMBER	PIN NAME	DESCRIPTION
1	1	A1	I^2C address, bit 1
2	2	A0	I^2C address, bit 0
3	3	EXT_CLK/INT	External ADC clock input or CPU interrupt output signal. When the pin is configured as an interrupt, the output is an open drain.
4	4	SDA/SMBDAT	I^2C serial data input/output.
5	5	SCL/SMBCLK	I^2C clock input
6	9	VCC	Positive power pin. The positive power supply to the part
7	10	GND	Negative power pin. Can be connected to ground or a negative voltage.
8	11	VBUS	VBUS power voltage sense.
9	12	VINM	Current sense minus input.
10	13	VINP	Current sense plus input.
	6, 7, 8, 14, 15, 16	NC	No connect. No internal connection.
	Epad	GND	Negative power pin. Can be connected to ground or a negative voltage.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28022FUZ	8022F	-40 to +125	10 Ld MSOP	M10.118
ISL28022FRZ	022F	-40 to +125	16 Ld QFN	L16.3x3B
ISL28022EVKIT1Z	ISL28022 Evaluation Kit (Includes Dongle Board, Generic Evaluation Board, R_{Load} Board)			
ISL28022MBEV1Z	ISL28022 Generic Evaluation Board			
ISL28022EV1Z	ISL28022 8-site Evaluation Board.			

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28022. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

VCC 6.0V
VBUS Voltage. 63V
Common Mode Input Voltage (V_{INP}, V_{INM}) 63V
Differential Input Voltage (V_{INP}, V_{INM}) . . . . . ±63V
Input Voltage (Digital Pins) . . . . . GND - 0.3V to 5.5V
Output Voltage (Digital Pins) . . . . . GND - 0.3 to VCC + 0.3V
Open Drain Output Current 10mA
Open Drain Voltage (Interrupt) 24V
ESD Rating
Human Body Model (Tested per JESD22-A114) 8kV
Machine Model (Tested per JESD22-A115). 300V
Charged Device Model (Tested per JESD22-C101 . . . . . 2kV
Latch-up (Tested per JESD-78B) . . . . . 60V at +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN (Notes 4, 5)	52	6.5
10 Ld MSOP (Notes 6, 7)	150	55

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. For θJ_C, the "case temp" location is taken at the package top center.

Electrical Specifications

T_A = +25°C, V_{CC} = 3.3, V_{INP} = V_{bus} = 12V, V_{SENSE} = V_{INP}-V_{INM} = 32mV, unless otherwise specified. All voltages with respect to GND pin.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
INPUTS						
$V_{SENSEDIFF}$	Useful Full Scale Current Sense Differential Voltage Range (V_{INP}-V_{INM})	PGA Gain = /1	0		±40	mV
		PGA Gain = /2	0		±80	mV
		PGA Gain = /4	0		±160	mV
		PGA Gain = /8	0		±300	mV
V_{SHUNT_step}	LSB Step Size, Shunt Voltage			10		µV
$V_{CMSENSE}$	Current Sense Common Mode (VINP, VINM)		0		60	V
V_{OS}	V_{SENSE} Offset Voltage	PGA Gain = /1, /2, /4, /8; ADC Setting = 1111		±10	±75	µV
V_{OSTC}	V_{SENSE} Offset Voltage Temperature Coefficient			0.15		µV/°C
CMRR	V_{SENSE} V_{OS} vs Common Mode	V_{bus} = 0V to 60V; BRNG = 2, 3	110	130		dB
PSRR	V_{SENSE} V_{OS} vs Power Supply	V_{CC} = 3V to 5V		105		dB
A_{CS}	Current Sense Gain Error			±40		m%
A_{CSTC}	Current Sense Gain Error Temperature Coefficient			±1		m%/°C
I_{VINACT}	Input Leakage, VIN Pins	Active Mode (for both V_{INP} and V_{INM} pins)		±20		µA
I_{VINACT}	Input Leakage, VIN Pins	Power-Down Mode (for both V_{INP} and V_{INM} pins)		±0.1	±0.5	µA

Electrical Specifications T_A = +25°C, V_{CC} = 3.3, V_{INP} = V_{bus} = 12V, V_{SENSE} = V_{INP}-V_{INM} = 32mV, unless otherwise specified. All voltages with respect to GND pin. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{BUS}	Useful Bus Voltage Range	BRNG = 0	0		16	V
		BRNG = 1	0		32	V
		BRNG = 2, 3	0		60	V
V_{BUS}_Step	LSB Step Size, Bus Voltage	BRNG = 0		4		mV
V_{BUS}_VCO	V_{bus} Voltage Coefficient			50		ppm/V
R_{VBACT}	Input Impedance, VBUS Pin	Active Mode		600		kΩ
DC ACCURACY						
	ADC Resolution (Native)	PGA gain = /1, V_{SENSE} = ±300mV		16		Bits
	Current Measurement Error	T_A = +25°C		±0.2	±0.3	%
	Current Measurement Error Over Temperature	T_A = -40°C to +85°C			±0.5%	%
		T_A = -40°C to +125°C			±1%	%
	Bus Voltage Measurement Error	T_A = +25°C		±0.2	±0.3	%
	Bus Voltage Measurement Error Over Temperature	T_A = -40°C to +85°C			±0.5%	%
		T_A = -40°C to +125°C			±1%	%
ADC TIMING SPECS						
t_s	ADC Conversion Time Mode = 5 or 6	ADC setting = 0000		72	79.2	µs
		ADC setting = 0001		132	145.2	µs
		ADC setting = 0010		258	283.8	µs
		ADC setting = 0011		508	558.8	µs
		ADC setting = 1001		1.01	1.11	ms
		ADC setting = 1010		2.01	2.21	ms
		ADC setting = 1011		4.01	4.41	ms
		ADC setting = 1100		8.01	8.81	ms
		ADC setting = 1101		16.01	17.61	ms
		ADC setting = 1110		32.01	35.21	ms
		ADC setting = 1111		64.01	70.41	ms
I^2C INTERFACE SPECIFICATIONS						
V_{IL}	SDA and SCL Input Buffer LOW Voltage		-0.3		0.3 x VCC	V
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		0.7 x V_{CC}		V_{CC} + 0.3	V
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.05 x V_{CC}		V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{CC} = 5V, I_{OL} = 3mA	0	0.02	0.4	V
C_{PIN}	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{CC} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns

Electrical Specifications T_A = +25°C, V_{CC} = 3.3, V_{INP} = V_{bus} = 12V, V_{SENSE} = V_{INP}-V_{INM} = 32mV, unless otherwise specified. All voltages with respect to GND pin. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing.	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing.	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}.	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.	20		900	ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.	600			ns
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.	0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 x Cb		300	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 x Cb		300	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip		75		pF
R_{PU}	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ~2.5kΩ. For Cb = 40pF, max is about 15kΩ~20kΩ	1			k

Electrical Specifications

T_A = +25°C, V_{CC} = 3.3, V_{INP} = V_{bus} = 12V, V_{SENSE} = V_{INP}-V_{INM} = 32mV, unless otherwise specified. All voltages with respect to GND pin. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
POWER SUPPLY						
	Operating Supply Voltage Range		3		5.5	V
I_{CCEXT}	Power Supply Current On V_{CC} Pin, Active Mode	External power supply mode, V_{CC} = 5V		0.7	1.0	mA
I_{CCPD}	Power Supply Current On V_{CC} Pin, Power-Down Mode	External power supply mode, V_{CC} = 5V		5	15	µA

NOTE:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{bus} = 12V, S(B)ADC = 15; unless otherwise specified.

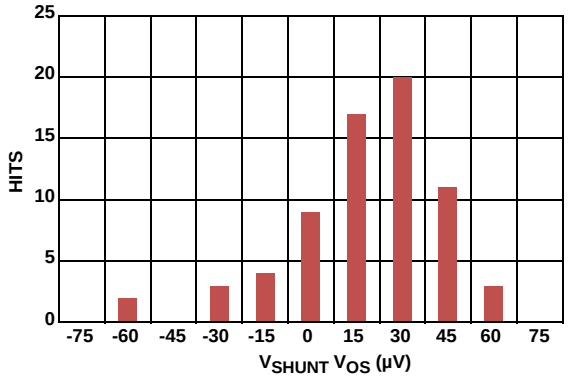


FIGURE 2. V_{SHUNT} V_{OS}

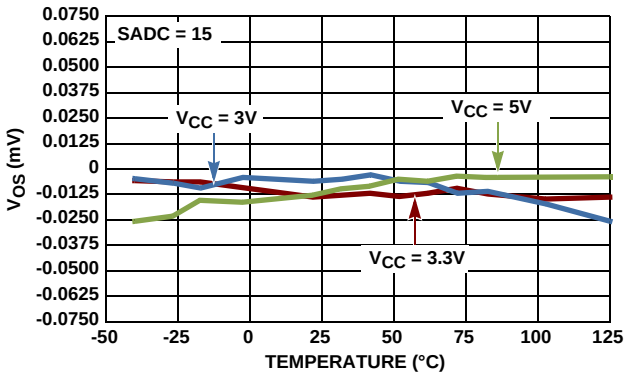


FIGURE 3. V_{SHUNT} V_{OS} vs TEMPERATURE

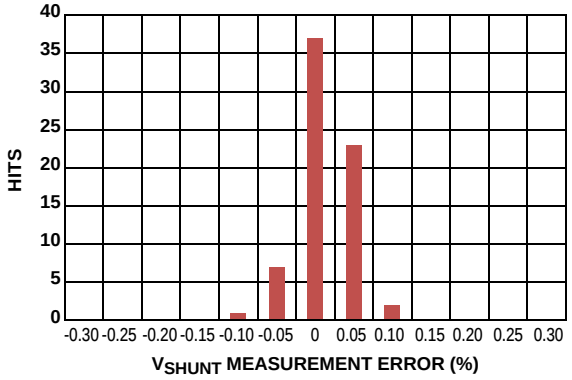


FIGURE 4. V_{SHUNT} MEASUREMENT ERROR

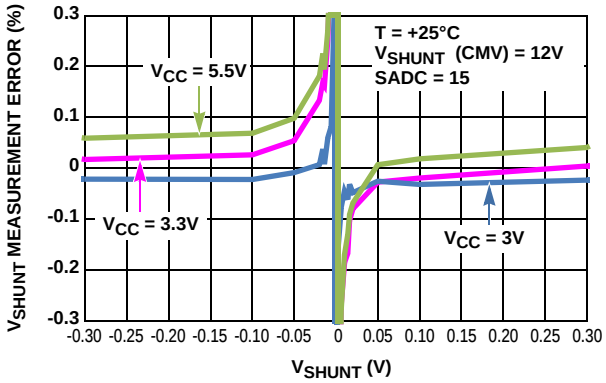


FIGURE 5. V_{SHUNT} MEASUREMENT ERROR vs V_{SHUNT} INPUT

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{bus} = 12V, S(B)ADC = 15; unless otherwise specified.

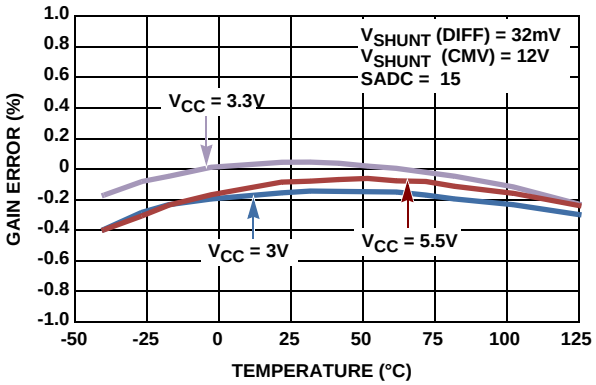


FIGURE 6. V_{SHUNT} GAIN vs TEMPERATURE

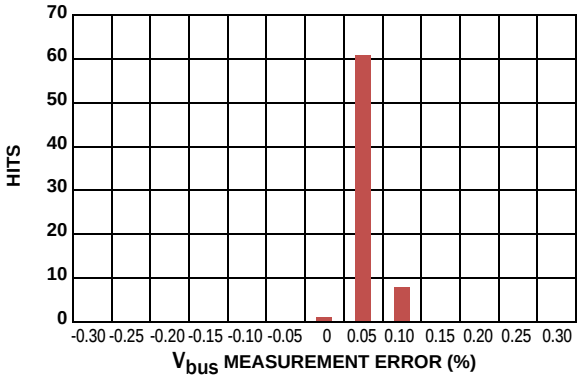


FIGURE 7. V_{bus} MEASUREMENT ERROR DISTRIBUTION

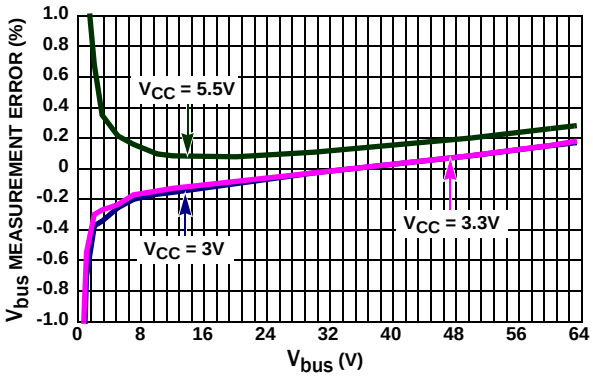


FIGURE 8. V_{bus} MEASUREMENT ERROR vs V_{bus} (T_A = +25°C)

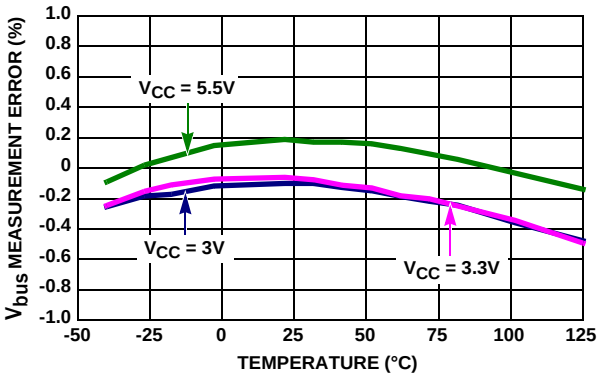


FIGURE 9. V_{bus} MEASUREMENT ERROR vs TEMPERATURE

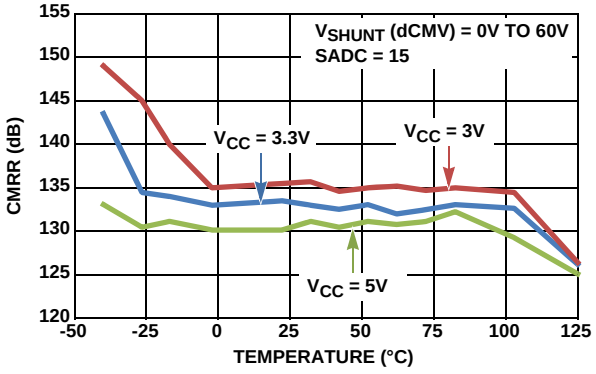


FIGURE 10. CMRR vs TEMPERATURE

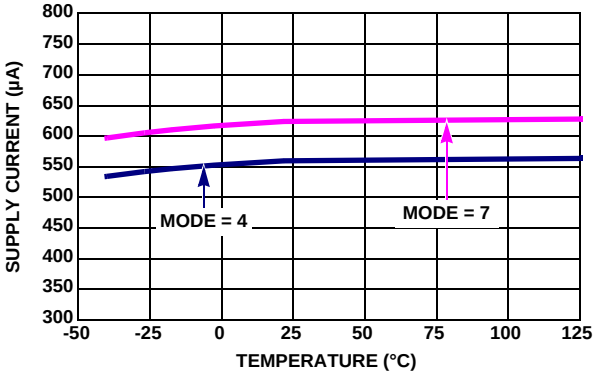


FIGURE 11. SUPPLY CURRENT vs MODE vs TEMPERATURE

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{bus} = 12V, S(B)ADC = 15; unless otherwise specified.

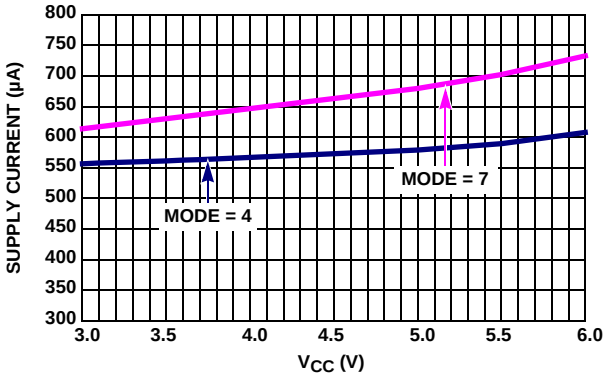


FIGURE 12. SUPPLY CURRENT vs MODE vs VCC

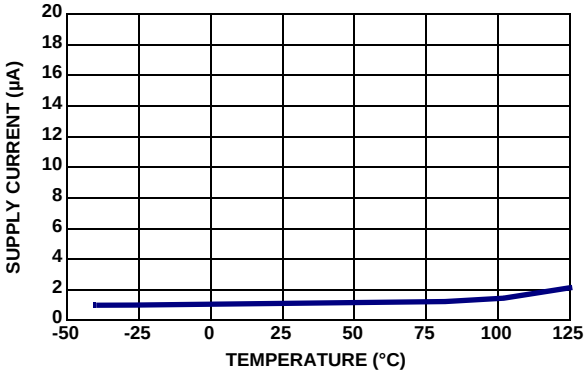


FIGURE 13. SUPPLY CURRENT vs MODE 0 vs TEMPERATURE

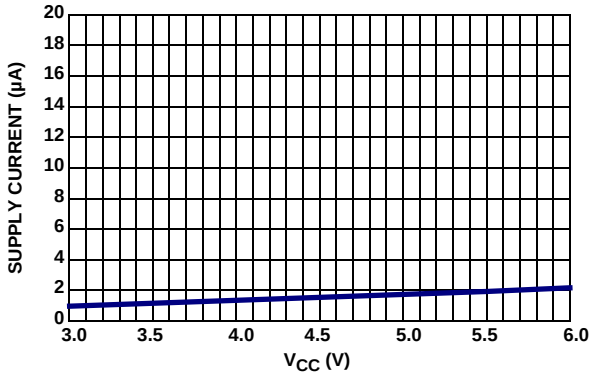


FIGURE 14. SUPPLY CURRENT vs MODE 0 vs V_{CC}

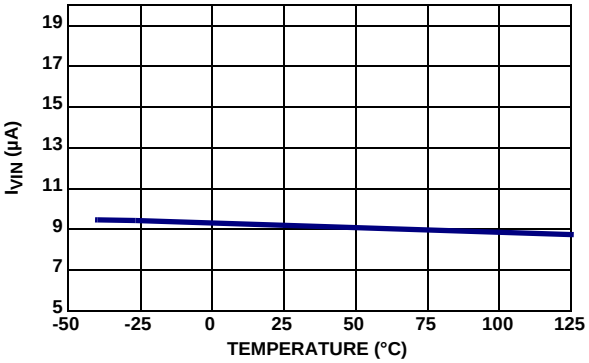


FIGURE 15. SHUNT I_{VIN} vs TEMPERATURE (MODE 5)

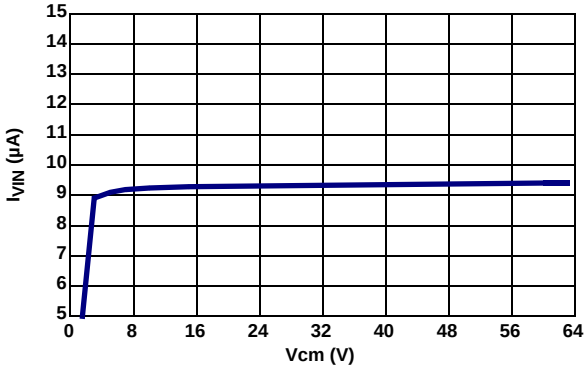


FIGURE 16. SHUNT I_{VIN} vs COMMON MODE VOLTAGE (MODE 5)

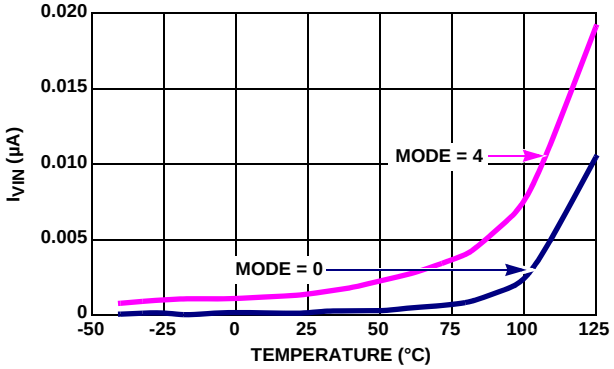


FIGURE 17. SHUNT I_{VIN} vs TEMPERATURE (MODE 0, 4)

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{bus} = 12V, S(B)ADC = 15; unless otherwise specified.

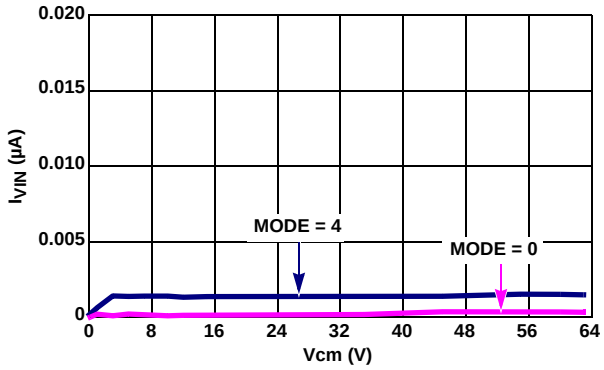


FIGURE 18. SHUNT I_{VIN} vs COMMON MODE VOLTAGE (MODE 0, 4)

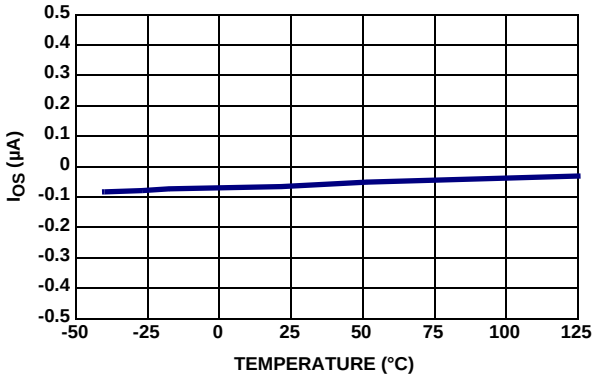


FIGURE 19. SHUNT I_{OS} vs TEMPERATURE (MODE 5)

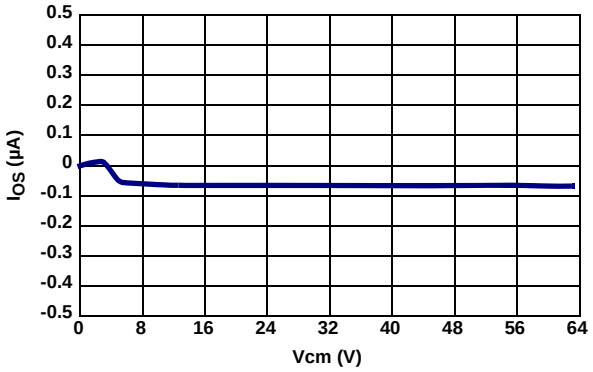


FIGURE 20. SHUNT I_{OS} vs COMMON MODE VOLTAGE (MODE 5)

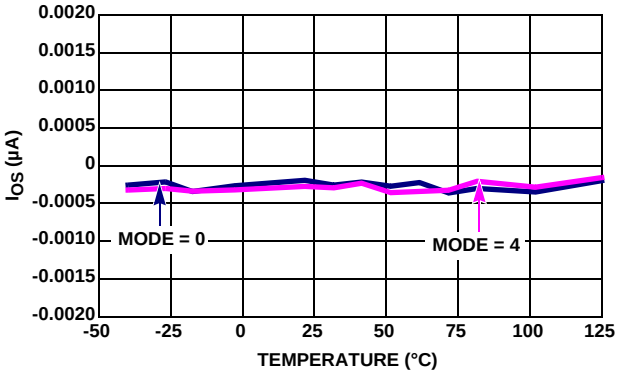


FIGURE 21. SHUNT I_{OS} vs TEMPERATURE (MODE 0, 4)

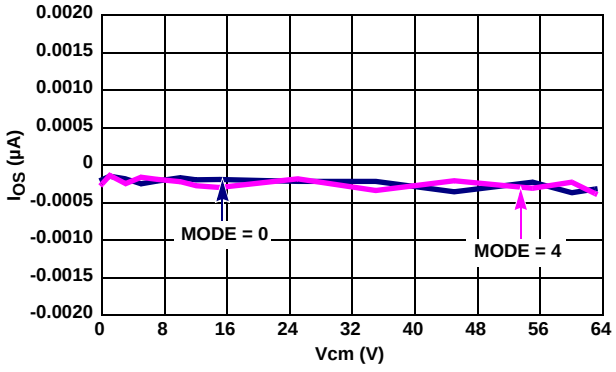


FIGURE 22. SHUNT I_{OS} vs COMMON MODE VOLTAGE (MODE 0, 4)

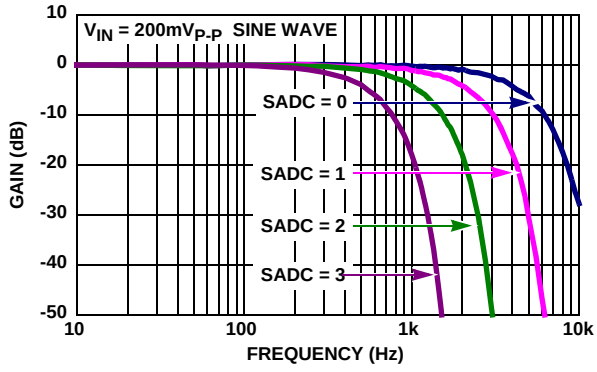


FIGURE 23. V_{SHUNT} BANDWIDTH vs SADC MODE

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{bus} = 12V, S(B)ADC = 15; unless otherwise specified.

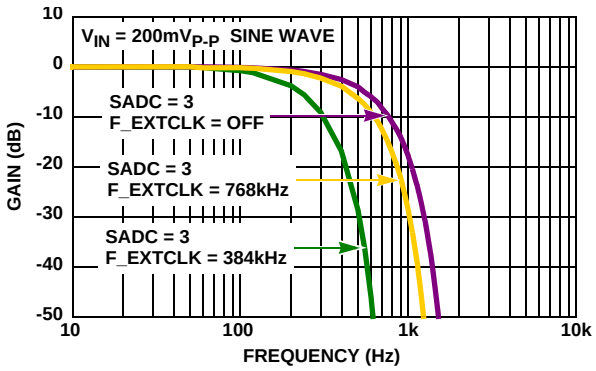


FIGURE 24. V_{SHUNT} BANDWIDTH vs EXTERNAL CLOCK FREQUENCY

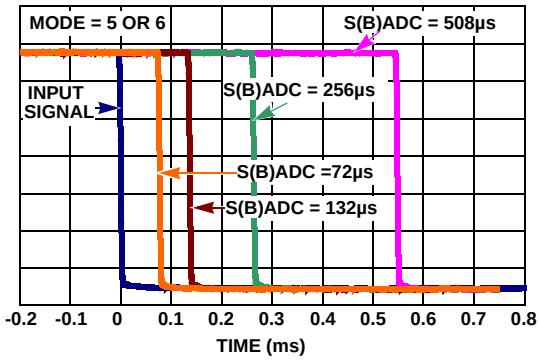


FIGURE 25. INTERRUPT TIMING

Functional Description

Overview

The ISL28022 is a digital power monitor (DPM) device that is capable of measuring bi-directional currents while monitoring the bus voltage.

The DPM requires an external shunt resistor to enable current measurements. The shunt resistor translates the bus current to a voltage. The DPM measures the voltage across the shunt resistors and reports the measured value out digitally via an I^2C interface. A register within the DPM is reserved to store the value of the shunt resistor. The stored current sense resistor value allows the DPM to output the current value to an external digital device.

The ISL28022 measures bus voltage and current sequentially. The device has a power measurement functionality that multiplies current and voltage measured values. The power calculation is stored in a unique register. The power measurement allows the user to monitor power to or from the load in addition to current and voltage.

The ISL28022 can monitor supplies from 0V to 60V while operating on a chip supply ranging from 3V to 5.5V.

The ISL28022 ADC sample rate can be configured to an internal oscillator (500kHz) or a user can provide a synchronized clock.

Detailed Description

The ISL28022 consists of a two channel analog front end multiplexer, a 16-bit sigma delta ADC and digital signal processing/serial communication circuitry.

The main block within the device is a 3rd order Sigma Delta ADC. The input signal bandwidth is 1kHz, wide enough for power monitoring applications. The main block includes an internal 1.2V band gap voltage reference that is used to drive the ADC.

The analog front end multiplexer selects the input to the ADC. The selection to the input of the ADC is either a single-ended V_{bus} measurement or a fully differential measurement across a shunt resistor.

The digital block contains controllable registers, I^2C serial communication circuitry and a state machine. The state machine controls the behavior of the ADC acquisition, whether the acquisition is triggered or continuous. A more detailed description of the state machine states can be found in “MODE: Operating Mode” on page 14.

Pin Descriptions

A1

A1 is the address select pin. A1 is one of two I^2C/SMBus slave address select pins that are multi-logic programmable for a total of 16 different address combinations.

There are four selectable levels for A1, VCC, GND, SCL/SMBCLK, and SDA/SMBDAT. See Table 21 for more details in setting the slave address of the device.

A0

A0 is the address select pin. A0 is one of two I^2C/SMBus slave address select pins that are multi-logic programmable for a total of 16 different address combinations.

There are four selectable levels for A0, VCC, GND, SCL/SMBCLK, and SDA/SMBDAT. See Table 21 for more details in setting the slave address of the device.

EXT_CLK/INT

EXT_CLK/INT is the External/Interrupt clock pin. EXT_CLK/INT is a bi-directional pin. The pin provides a connection to the system clock. The system clock is connected to the ADC. The acquisitions rate of the ADC can be varied through the EXT_CLK/INT pin. The pin functionality is set through a control register bit.

When the EXT_CLK/INT pin is configured as an output, the pin functionality becomes an interrupt flag to connecting devices. EXT_CLK/INT pin as an output requires a pull-up resistor to a power supply, up to 20V, for proper operation. The internal threshold detectors (OV_{sh}/UV_{sh}/OV_b/UV_b) signal level relative to the measured value determines the state of the INT pin.

SDA/SMBDAT

SDA/SMBDAT is the serial data input/output pin. SDA/SMBDAT is a bi-directional pin used to transfer data to and from the device. The pin is an open drain output and may be wired with other open drain/collector outputs. The open drain output

requires a pull-up resistor for proper functionality. The pull-up resistor should be connected to VCC of the device.

SCL/SMBCLK

SCL/SMBCLK is the serial clock input pin. The SCL/SMBCLK input is responsible for clocking in all data to and from the device.

VCC

VCC is the positive supply voltage pin. VCC is an analog power pin. VCC supplies power to the device.

GND

GND is the ground pin. All voltages internal to the chip are referenced to ground. GND should be tied to 0V for single supply applications. For dual supply applications, the pin should be connected to the most negative voltage in the application.

VBUS

VBUS is the power bus voltage input pin. The pin should be connected to the desired power supply bus to be monitored.

VINP

VINP is the shunt voltage monitor positive input pin. The pin connects to the most positive voltage of the current shunt resistor.

VINM

VINM is the shunt voltage monitor negative input pin. The pin connects to the most negative voltage of the current shunt resistor.

Register Descriptions

Table 1 is the register map for the device. The table describes the function of each register and its respective value. The addresses are sequential and the register size is 16 bits (2 bytes) per address.

CONFIGURATION REGISTER

The configuration register (Table 2) controls the functionality of the chip. ADC measurable range, converter acquisition times, converter resolution and state machine modes are configurable bits within this register.

RST: Reset Bit

Configuring the reset bit (Bit 15) to a 1 generates a system reset that initializes all registers to their default values and performs a system calibration.

BRNG: Bus Voltage Range

Bits 13 and 14 of the configuration register sets the bus measurable voltage range. Table 3 shows the BRNG bit configurations versus the allowable full scale measurement range. The shaded row is the power-up default.

TABLE 1. ISL28022 REGISTER DESCRIPTIONS

REGISTER ADDRESS (HEX)	REGISTER NAME	FUNCTION	POWER-ON RESET VALUE (HEX)	ACCESS
00	Configuration	Power On Reset, Bus and Shunt ranges, ADC acquisition times, Mode configuration	799F	R/W
01	Shunt Voltage	Shunt voltage measurement value	0000	R
02	Bus Voltage	Bus voltage measurement value	0000	R
03	Power	Power measurement value	0000	R
04	Current	Current measurement value	0000	R
05	Calibration Register	Register used to enable current and power measurements.	0000	R/W
06	Shunt Voltage Threshold	Min/Max Shunt thresholds	7F81	R/W
07	Bus Voltage Threshold	Min/Max V_{bus} thresholds	FF00	R/W
08	DCS Interrupt Status	Threshold interrupts	0000	R/W
09	Aux Control Register	Register to control the interrupts and external clock functionality	0000	R/W

TABLE 2. CONFIGURATION REGISTER

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	RST	BRNG1	BRNG0	PG1	PG0	BADC3	BADC2	BADC1	BADC0	SADC3	SADC2	SADC1	SADC0	MODE2	MODE1	MODE0

TABLE 3. BRNG BIT SETTINGS

BRNG1	BRNG0	USABLE FULL SCALE RANGE (V)
0	0	16
0	1	32
1	0	60
1	1	60

PG: PGA (Shunt Voltage Only)

Bits 11 and 12 of the configuration register determines the shunt voltage measurement range. Table 4 shows the PGA bit configurations versus the allowable full scale measurement range. The shaded row is the power-up default.

TABLE 4. PGA BIT SETTINGS

PG1	PG0	GAIN	RANGE (mV)
0	0	1	±40
0	1	÷2	±80
1	0	÷4	±160
1	1	÷8	±300

BADC: Bus ADC Resolution/Averaging

Bits [10:7] of the configuration register sets the ADC resolution/averaging when the ADC is configured in the V_{bus} mode. The ADC can be configured versus bit accuracy. The bit accuracy selections range from 12 to 15-bits. The ADC is configurable versus the number of averages. The selection ranges from 2 to 128 samples. Table 5 shows the breakdown of each BADC setting. The shaded row is the default setting upon power-up.

SADC: Shunt ADC Resolution/Averaging

Bits [10:7] of the configuration register sets the ADC resolution/averaging when the ADC is configured in the V_{SHUNT} mode. The ADC can be configured versus bit accuracy. The bit accuracy selections range from 12 to 15-bits. The ADC is configurable versus number of averages. The selection ranges from 2 to 128 samples. Table 5 shows the break down of each SADC setting. The shaded row is the default setting upon power-up.

MODE: Operating Mode

Bits [2:0] of the configuration register controls the state machine within the chip. The state machine globally controls the overall functionality of the chip. Table 6 shows the various states the chip can be configured to, as well as the mode bit definitions to achieve a desired state. The shaded row is the default setting upon power-up.

TABLE 5. ADC SETTINGS, APPLIES TO BOTH SADC AND BADC CONTROL

ADC3	ADC2	ADC1	ADC0	MODE/SAMPLES	CONVERSION TIME
0	X	0	0	12-Bit	72µs
0	X	0	1	13-Bit	132µs
0	X	1	0	14-Bit	258µs
0	X	1	1	15-Bit	508µs
1	0	0	0	15-Bit	508µs
1	0	0	1	2	1.01ms
1	0	1	0	4	2.01ms
1	0	1	1	8	4.01ms
1	1	0	0	16	8.01ms
1	1	0	1	32	16.01ms
1	1	1	0	64	32.01ms
1	1	1	1	128	64.01ms

TABLE 6. OPERATING MODE SETTINGS

MODE2	MODE1	MODE0	MODE
0	0	0	Power-Down
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	ADC Off (disabled)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

SHUNT VOLTAGE REGISTER 01H (READ-ONLY)

The Shunt Voltage Register reports the measured value across the shunt pins (VINP and VINM) into the register. The shunt register LSB is independent of PGA range settings. The PGA setting for the shunt register masks the unused most significant bit with a sign bit. For lower range of PGA settings, multiple sign bits are returned by the DPM. Only one sign bit should be used to calculate the measured value.

Tables 7 through 10 show the weights of each bit for various PGA ranges. The tables should be used to calculate the measured value across the shunt pins from the binary to decimal domains.

To calculate the measured decimal value across the shunt, first read the shunt voltage register. Assume the PGA setting is set to the 80mV range. For this example, the reading output by the chip is 1111 1010 0000 0101. The 80mV range has three sign bits.

Only one sign bit needs to be used to calculate the measured decimal value. Bits 14 and 15 are omitted from the calculation. This leaves a binary reading of 11 1010 0000 0101.

Next, multiply each bit by its respective weight. Bit0 value would be multiplied by bit0 weight (1), Bit1 value * Bit1 weight (2), etc....

Add all the multiplied values to equate to a single number. For the binary reading 11 1010 0000 0101 this equates to -1531.

The LSB for a shunt register is 10µV. Multiplying the decimal value by the LSB weight yields the measured voltage across the shunt. A 1111 1010 0000 0101 reading equals -15.31mV measured across the shunt pins.

TABLE 7. SHUNT VOLTAGE REGISTER, PG GAIN = /8 (RANGE = 11), FULL SCALE = ±300mV, 15 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT	-32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 8. SHUNT VOLTAGE REGISTER, PG GAIN = /4 (RANGE = 10), FULL SCALE = ±160mV, 14 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Sign	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT		-16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 9. SHUNT VOLTAGE REGISTER, PG GAIN = /2 (RANGE = 01), FULL SCALE = ±80mV, 13 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Sign	Sign	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT			-8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 10. SHUNT VOLTAGE REGISTER, PG GAIN = /1 (RANGE = 00), FULL SCALE = ±40mV, 12 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Sign	Sign	Sign	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT				-4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 11. BUS VOLTAGE REGISTER, BRNG = 10 OR 11, FULL SCALE = 60V, 14 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CNVR	OVF
WEIGHT	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1		

TABLE 12. BUS VOLTAGE REGISTER, BRNG = 01, FULL SCALE = 32V, 13 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		CNVR	OVF
WEIGHT	4096	2048	1024	512	256	128	64	32	16	8	4	2	1			

TABLE 13. BUS VOLTAGE REGISTER, BRNG = 00, FULL SCALE = 16V, 12 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME		Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		CNVR	OVF
WEIGHT		2048	1024	512	256	128	64	32	16	8	4	2	1			

TABLE 14. CALIBRATION REGISTER, 05h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

BUS VOLTAGE REGISTER 02H (READ-ONLY)

The Bus Voltage Register is where the DPM reports the measured value of the V_{bus}. There are three scale ranges possible depending on the BRNG setting controlled from the configuration register(00H).

Tables 11 through 13 are the weight bits for each BRNG setting. The binary value recorded in the Bus Voltage Register is translated to a decimal value in the same way as the shunt voltage register is converted to a decimal value.

$$V_{bus} = \left[\sum_{n=0}^{15}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot Vbus_{LSB} \quad \text{(EQ. 1)}$$

Equation 1 is the mathematical equation for converting the binary V_{bus} value to a decimal value. N is the bit number. The LSB value for the V_{bus} measurement equals 4mV across all bus range (BRNG) settings.

CNVR: Conversion Ready (Bit 1)

The Conversion Ready Bit indicates when the ADC has finished a conversion and transferred the reading(s) to the appropriate register(s). The CNVR is only operable when the DPM is set to one of three trigger modes. The CNVR is at a high state when the conversion is in progress. The CNVR transitions and remains at a low state when the conversion is complete.

The CNVR bit is initialized or re-initialized in the following ways:

1. Writing to the configuration register.
2. Reading from Power Register.

OVF: Math Overflow Flag (Bit 0)

The Math Overflow Flag (OVF) is a bit that is set to indicate the current or power data being read from the DPM is over ranged and meaningless.

CALIBRATION REGISTER 05H (READ/WRITE)

To accurately read the current and power measurements from the chip, the calibration register needs to be programmed.

The calibration register value is calculated as follows:

1. Calculate the full scale current range that is desired. This is calculated using Equation 2. R_{shunt} is the value of the shunt resistor. V_{SHUNT} is the full scale setting that is desired. In most cases, it is the PGA full scale range (300mV, 160mV, 80mV and 40mV) that the DPM is programmed to.

$$Current_{FS} = \frac{Vshunt_{FS}}{R_{shunt}} \quad \text{(EQ. 2)}$$

2. From the current full scale range, the current LSB is calculated using Equation 3. Current full scale is the outcome from Equation 2. ADC_{res} is the resolution of shunt voltage reading. The value is determined by the SADC setting in configuration register. SADC setting equal to 3 and greater will have a 15-bit resolution. The ADC_{res} value equals 2^{15} or 32768.

$$Current_{LSB} = \frac{Current_{FS}}{ADC_{res}} \quad \text{(EQ. 3)}$$

3. From Equation 3, the calibration resister value is calculated using Equation 4. The resolution of the math that is processed internally in the DPM is 4096 or 12 bits of resolution. The V_{SHUNT} LSB is set to 10µV. Equation 4 yields a 16-bit binary number that can be written to the calibration register. The calibration register format is represented in Table 14.

$$CalReg_{val} = integer\left[\frac{Math_{res} \cdot Vshunt_{LSB}}{\left(Current_{LSB} \cdot R_{shunt}\right)}\right]$$

$$CalReg_{val} = integer\left[\frac{0.04096}{\left(Current_{LSB} \cdot R_{shunt}\right)}\right] \quad \text{(EQ. 4)}$$

CURRENT REGISTER 04H (READ-ONLY)

Once the calibration register (05h) is programmed, the output current is calculated using Equation 5:

$$\text{Current} = \left[\sum_{n=0}^{15}\left(\text{Bit}_n \cdot \text{Bit\_Weight}_n\right)\right] \cdot \text{Current}_{LSB} \quad \text{(EQ. 5)}$$

Bit is the returned value of each bit from the current register either 1 or a 0. The weight of each bit is represented in Table 15. n is the bit number. The current LSB is the value calculated from Equation 3.

POWER REGISTER 03H (READ-ONLY)

The Power register only has meaning if the calibration register (05H) is programmed. The units for the power register are in watts. The power is calculated using Equation 6:

$$\text{Power} = \left[\sum_{n=0}^{15}\left(\text{Bit}_n \cdot \text{Bit\_Weight}_n\right)\right] \cdot \text{Power}_{LSB} \cdot 5000 \quad \text{(EQ. 6)}$$

Bit is the returned value of each bit from the power register either 1 or a 0. The weight of each bit is represented in Table 16. n is the bit number. The power LSB is calculated from Equation 7:

$$\text{Power}_{LSB} = \text{Current}_{LSB} \cdot \text{Vbus}_{LSB} \quad \text{(EQ. 7)}$$

If V_{bus} range, BRNG, is set to 60V, the power equation in Equation 6 is multiplied by 2.

THRESHOLD REGISTERS

The Shunt Voltage or V_{bus} threshold registers are used to set the Min/Max threshold limits that will be tested versus V_{SHUNT} or V_{bus} readings. Measurement readings exceeding the respective V_{SHUNT} or V_{bus} limits, either above or below, will set a register flag and perhaps an external interrupt depending on the configuration of the interrupt enable bit (INTREN) in register 09h. The testing of the ADC reading versus the respective threshold limits occurs once per ADC conversion.

SHUNT VOLTAGE THRESHOLD REGISTER 06H (READ/WRITE)

The V_{SHUNT} minimum and maximum threshold limits are set using one register. The shunt value readings are either positive or negative. D15 and D7 bits of Table 17 are given to represent the sign of the limit. SMX bits represent the upper limit threshold. SMN represents the lower threshold limit. Equation 8 is the calculation used to convert the V_{SHUNT} threshold binary value to decimal. Bit is the value of each bit set in the shunt threshold register. The value is either 1 or a 0. The weight of each bit is represented in Table 17. n is the bit number. The shunt voltage threshold LSB is 2.56mV.

$$\text{Vs}_{\text{thresh}} = \left[\sum_{n=0}^{7}\left(\text{Bit}_n \cdot \text{Bit\_Weight}_n\right)\right] \cdot \text{VsThresh}_{LSB} \quad \text{(EQ. 8)}$$

TABLE 15. CURRENT REGISTER, 04h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Bit 15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT	-32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 16. POWER REGISTER, 03h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
WEIGHT	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 17. SHUNT VOLTAGE THRESHOLD REGISTER, 06h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	SMX6	SMX5	SMX4	SMX3	SMX2	SMX1	SMX0	Sign	SMN6	SMN5	SMN4	SMN3	SMN2	SMN1	SMN0
WEIGHT	-128	64	32	16	8	4	2	1	-128	64	32	16	8	4	2	1

TABLE 18. BUS VOLTAGE THRESHOLD REGISTER, 07h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	BMX7	BMX6	BMX5	BMX4	BMX3	BMX2	BMX1	BMX0	BMN7	BMN6	BMN5	BMN4	BMN3	BMN2	BMN1	BMN0
WEIGHT	128	64	32	16	8	4	2	1	128	64	32	16	8	4	2	1

TABLE 19. INTERRUPT STATUS REGISTER, 08h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	SMXW	SMNW	BMXW	BMNW
WEIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TABLE 20. AUX CONTROL REGISTER, 09h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	NA	NA	NA	NA	NA	NA	NA	FORCEINTR	INTREN	ExtClkEn	ExtCLKDiv[5:0]					
WEIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUS VOLTAGE THRESHOLD REGISTER 07H (READ/WRITE)

The V_{bus} minimum and maximum threshold limits are set using one register. The V_{bus} value readings range from 0V to 60V. Table 18 shows the register configuration and bit weights for the V_{bus} threshold register. BMX bits represent the upper limit threshold. BMN represents the lower threshold limit. Equation 9 is the calculation used to convert the V_{bus} threshold binary value to decimal. Bit is the value of each bit set in the V_{bus} threshold register. The value is either 1 or a 0. The weight of each bit is represented in Table 18. n is the bit number. The V_{bus} voltage threshold LSB is 256mV.

$$Vb_{thresh} = \left[\sum_{n=0}^{7}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot VbThresh_{LSB} \quad \text{(EQ. 9)}$$

INTERRUPT STATUS REGISTER 08H (READ/WRITE)

The interrupt status register consists of a series of bit flags that indicate if an ADC reading has exceeded the readings respective limit. A 1 or high reading from a warning bit indicates the reading has exceeded the limit. To clear a warning, write a 1 or high to the set warning bit. Table 19 shows the definition of the interrupt status register.

BMNW is the bus voltage minimum warning. A 1 reading for this bit indicates the bus reading is below the bus voltage minimum threshold limit.

BMXW is the bus voltage maximum warning. A 1 reading for this bit indicates the bus reading is above the bus voltage maximum threshold limit.

SMNW is the shunt voltage minimum warning. A 1 reading for this bit indicates the shunt reading is below the shunt voltage minimum threshold limit.

SMXW is the shunt voltage maximum warning. A 1 reading for this bit indicates the shunt reading is above the shunt voltage maximum threshold limit.

AUX CONTROL REGISTER 09H (READ/WRITE)

The aux control register controls the functionality of the EXTCLK/INT pin of the ISL28022. Table 20 shows the definition of the register.

FORCEINTR is the force interrupt bit. Programming a 1 to the bit will force a 0 or a low at the EXTCLK/INT pin.

INTREN is the interrupt enable bit. Programming a 1 to the bit will allow for a threshold measurement violation to set the state of the EXTCLK/INT pin. With the INTREN set, any flag set from the interrupt status register will change the state of the EXTCLK/INT pin from 1 to a 0.

EXCLKEN is the external clock enable bit. Setting the bit enables the external clock. This also changes the EXTCLK/INT pin from an output to an input. The internal oscillator will shut down when the bit is enabled.

EXTCLKDIV are the external clock divider bits. The bits control an internal clock divider that are useful for fast system clocks. The internal clock frequency from pin to chip is represented in Equation 10:

$$freq_{internal} = \frac{f_{EXTCLK}}{(EXTCLKDIV + 1)\cdot 2} \quad \text{(EQ. 10)}$$

f_{EXTCLK} is the frequency of the signal driven to the EXTCLK/INT pin. EXTCLKDIV is the decimal value of the clock divide bits.

I²C Serial Interface

The ISL28022 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL28022 operates as a slave device in all applications.

The ISL28022 uses two bytes to transfer all reads and writes. All communication over the I²C interface is conducted by sending the MSByte of each byte of data first, followed by the LSByte.

Protocol Conventions

For normal operation, data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 26). On power-up of the ISL28022, the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL28022 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 26). A START condition is ignored during the power-up sequence.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 26). A STOP condition at the end of a read operation or at the end of a write operation places the device in its standby mode.

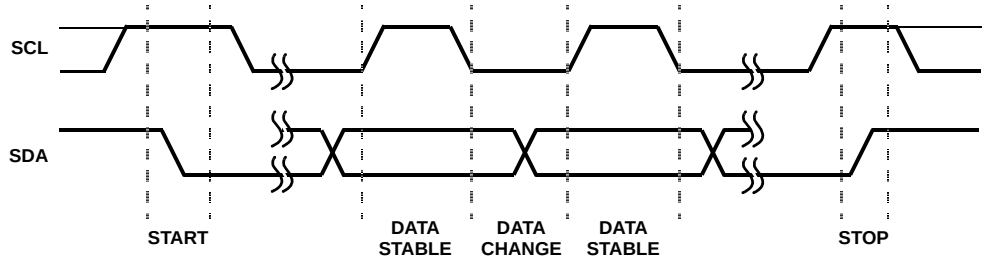


FIGURE 26. VALID DATA CHANGES, START AND STOP CONDITIONS

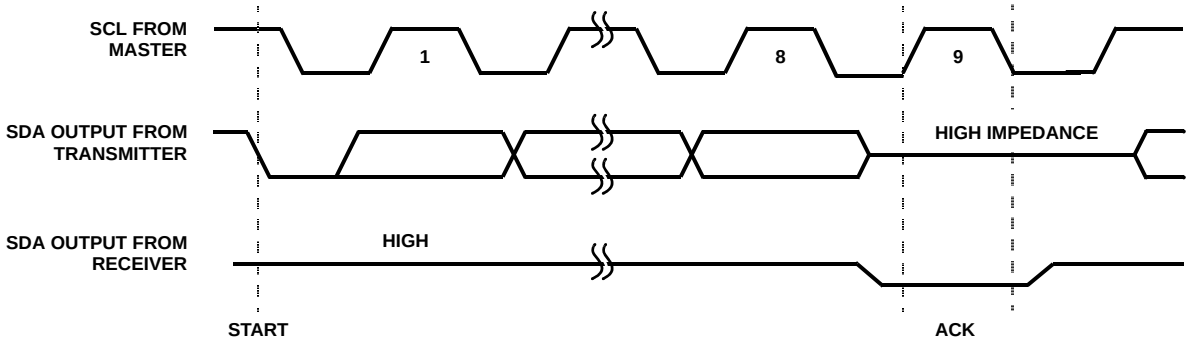


FIGURE 27. ACKNOWLEDGE RESPONSE FROM RECEIVER

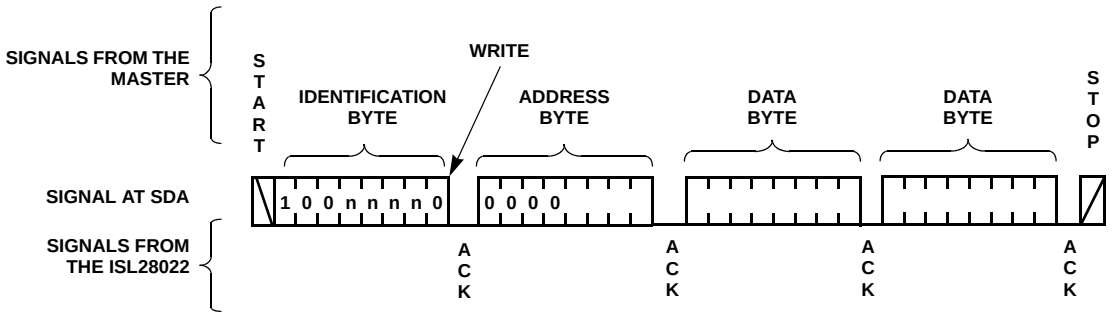


FIGURE 28. BYTE WRITE SEQUENCE (SLAVE ADDRESS INDICATED BY nnnn)

SMBus Support

The ISL28022 supports SMBus protocol, which is a subset of the global I^2C protocol. SMBCLK and SMBDAT have the same pin functionality as the SCL and SDA pins, respectively. The SMBus operates at 100kHz.

Device Addressing

Following a start condition, the master must output a slave address byte. The 7 MSB's are the device identifiers. The A0 and A1 pins control the bus address. These bits are shown in Table 21, there are 16 possible combinations depending on the A0/A1 connections.The last bit of the slave address byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a "1", a read operation is selected. A "0" selects a write operation (refer to Figure 28).

After loading the entire slave address byte from the SDA bus, the ISL28022 compares the loaded value to the internal slave address. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the slave byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the one word address byte, as shown in Figure 29.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the registers, the slave byte must be "100nnnnx" in both places.

TABLE 21. I^2C SLAVE ADDRESSES

A1	A0	SLAVE ADDRESS
GND	GND	1000 000
GND	VCC	1000 001
GND	SDA	1000 010
GND	SCL	1000 011
VCC	GND	1000 100
VCC	VCC	1000 101
VCC	SDA	1000 110
VCC	SCL	1000 111
SDA	GND	1001 000
SDA	VCC	1001 001
SDA	SDA	1001 010
SDA	SCL	1001 011
SCL	GND	1001 100
SCL	VCC	1001 101
SCL	SDA	1001 110
SCL	SCL	1001 111
Broadcast Address		0111 111

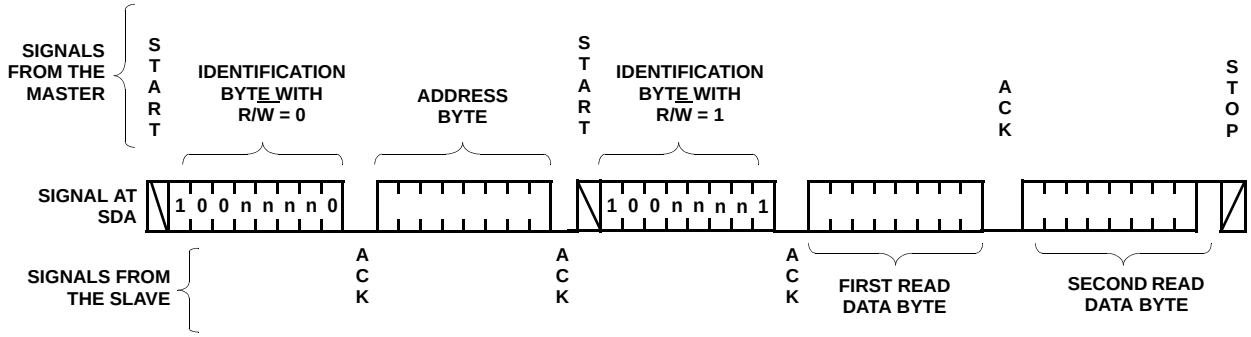


FIGURE 29. READ SEQUENCE (SLAVE ADDRESS SHOWN AS nnnn)

Write Operation

A write operation requires a START condition, followed by a valid identification byte, a valid address byte, two data bytes, and a STOP condition. The first data byte contains the LSB of the data, the second contains the MSB. After each of the four bytes, the ISL28022 responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A read operation consists of a three byte instruction, followed by two data bytes (see Figure 29). The master initiates the operation issuing the following sequence: A START, the identification byte with the R/$\overline{W}$ bit set to “0”, an address byte, a second START, and a second identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL28022 responds with an ACK. Then the ISL28022 transmits two data bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of the first byte. The master terminates the read operation (issuing no ACK then a STOP condition) following the last bit of the second data byte (see Figure 29).

The data bytes are from the memory location indicated by an internal pointer. This pointer’s initial value is determined by the address byte in the read operation instruction, and increments by one during transmission of each pair of data bytes. The highest valid memory location is 09h, reads of addresses higher than that will not return useful data.

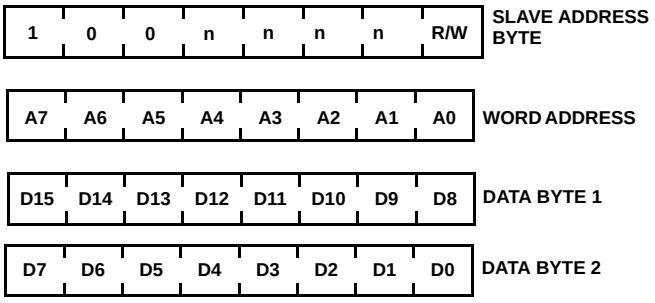


FIGURE 30. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Broadcast Addressing

The DPM has a feature that allows the user to configure the settings of all DPM chips at once. For example, a system has 16 DPM chips connected to an I^2C bus. A user can set the range or initiate a data acquisition in one I^2C data transaction by using a slave address of 0111 111. The broadcast feature saves time in configuring the DPM as well as measuring signal parameters in time synchronization. The broadcast should not be used for DPM read backs. This will cause all devices connected to the I^2C bus to talk to the master simultaneously.

I^2C Clock Speed

The device supports high-speed digital transactions up to 3.4Mbs. To access the high speed I^2C feature, a master byte code of 0000 1xxx is attached to the beginning of a standard frequency read/write I^2C protocol. The x in the master byte signifies a do not care state. X can either equal a 0 or a 1. The master byte code should be clocked into the chip at frequencies equal or less than 400kHz. The master code command configures the internal filters of the ISL28022 to permit data bit frequencies greater than 400kHz. Once the master code has been clocked into the device, the protocol for a standard read/write transaction is followed. The frequency at which the standard protocol is clocked in at can be as great as 3.4MHz. A stop bit at the end of a standard protocol will terminate the high speed transaction mode. Appending another standard protocol serial transaction to the data string without a stop bit, will resume the high speed digital transaction mode. Figure 31 illustrates the data sequence for the high speed mode.

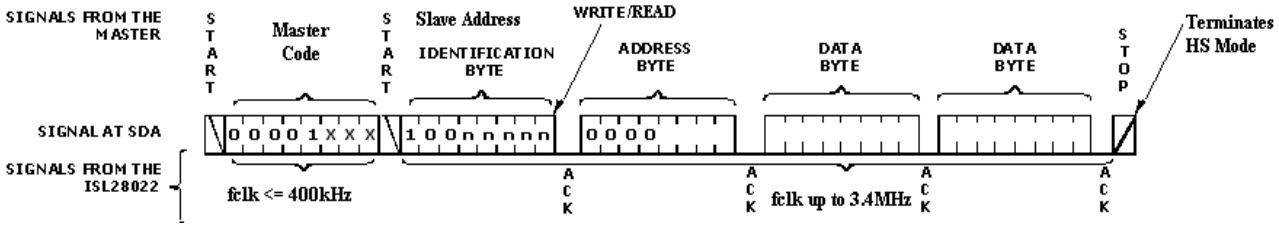


FIGURE 31. BYTE TRANSACTION SEQUENCE FOR INITIATING DATA RATES ABOVE 400kbs

Signal Integrity

The purity of the signal being measured by the ISL28022 is not always ideal. Environmental noise or noise generated from a regulator can degrade the measurement accuracy. The ISL28022 maintains a high CMRR ratio from DC to approximately 10kHz, as shown in Figure 32.

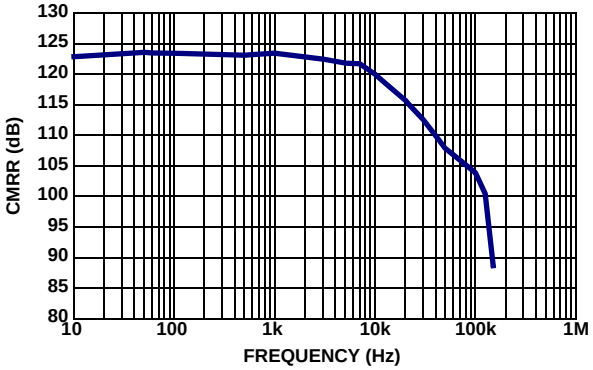


FIGURE 32. CMRR vs FREQUENCY

The CMRR vs Frequency graph best represents the response of the ISL28022 when an aberrant signal is applied to the circuit.

The graph was generated by shorting the ISL28022 input without any filtering and applying a 0V to 10V triangle wave to the Shunt inputs, VINP and VINM. The voltage shunt measurement was recorded for each frequency applied to the Shunt input.

The CMRR can be improved by designing a filter stage before the ISL28022. The purpose of the filter stage is to attenuate the amplitude of the unwanted signal to the noise level of the ISL28022. Figure 33 is a simple filter example to attenuate unwanted signals.

CSH and RSH are single pole RC filters that differentially attenuate unwanted signals to the ISL28022. Most power monitoring applications require a shunt resistor to be low in value to measure large currents. For small shunt resistors, a large value capacitor is required to attenuate low frequency signals. Most large value capacitors are not offered in space saving packages. The corner frequency of the differential filter, CSH and RSH, should be designed for higher value frequency filtering.

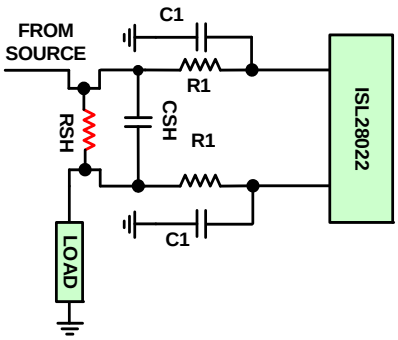


FIGURE 33. SIMPLIFIED FILTER DESIGN TO IMPROVE NOISE PERFORMANCE TO THE ISL28022

R_1 and C_1 for both inputs are single ended low pass filters. The value of the series resistor to the ISL28022 can be a larger value than the Shunt resistor, RSH. A larger series resistor to the input allows for a lower cutoff frequency filter design to the ISL28022. The ISL28022 can source up to 20µA of transient current in the measurement mode. The transient or switching offset current can be as large as 10µA. The switching offset current combined with the series resistance, R_1, creates an error offset voltage. A balance of the value of R_1 and the shunt measurement error should be achieved for this filter design.

The common mode voltage of the shunt input stage ranges from 0V to 60V. The capacitor voltage rating for C1 and CSH should comply with the nominal voltage being applied to the input.

Measurement Stability vs Acquisition Time

The BADC and SADC bits within the Configuration register configures the conversion time and accuracy for the bus and shunt inputs respectively. The faster the conversion time the less accuracy and more noise introduced into the measurement. Figure 34 is a graph that illustrates the shunt measurement variability versus a set SADC mode. The standard deviation of 2048 shunt V_{OS} measurements is used to quantify the measurement variability of each mode.

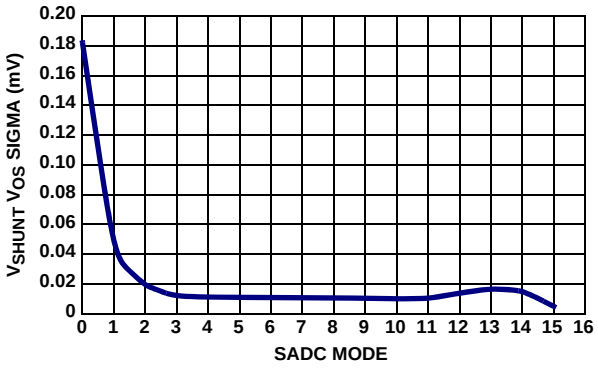


FIGURE 34. MEASUREMENT STABILITY vs SADC MODE

Fast Transients

A small isolation resistor placed between ISL28022 inputs and the source is recommended. In hot swap or other fast transient events, the amplitude of a signal can exceed the recommended operating voltage of the part due to the line inductance. The isolation resistor creates a low pass filter between the device and the source. The value of the isolation resistor should not be too large. A large value isolation resistor can effect the measurement accuracy. The offset current for shunt input can be as large as 10µA. The value of the isolation resistor combined with the offset current creates an error offset voltage at the shunt input. The input of the Bus channel is connected to the top of a precision resistor divider. The accuracy of the resistor divider determines the gain error of the Bus channel. The input resistance of the Bus channel is 600kΩ. Placing an isolation resistor of the 10Ω will change the gain error of the Bus channel by 0.0016%.

External Clock

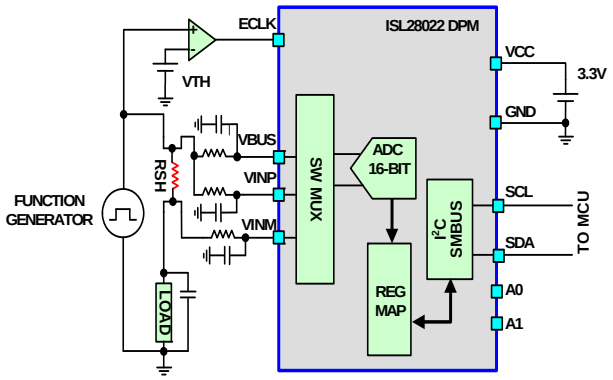


FIGURE 35. SIMPLIFIED SCHEMATIC OF THE ISL28022 SYNCHRONIZED TO A PWM SOURCE

An externally controlled clock allows measurements to be synchronized to an event that is time dependent. The event could be application generated, such as timing a current measurement to a charging capacitor in a switch regulator application or the event could be environmental. A voltage or current measurement may be suspectable to crosstalk from a controlled source. Instead of filtering the environmental noise from the measurement, another approach would be to synchronize the measurement to the source. The variability and accuracy of the measurement will improve.

The ISL28022 has the functionality to allow for synchronization to an external clock. The speed of the external clock combined with the choice of the internal chip frequency division value determines the acquisition times of the ADC. The internal system clock frequency is 500kHz. The internal system clock is also the ADC sampling clock. The acquisition times scale linearly from 500kHz. For example, an external clock frequency of 1.0MHz with a frequency divide setting of 2 results in acquisition times that equals the internal oscillator frequency when enabled. The internal clock frequency of the ISL28022 should not exceed 500kHz. The ADC modulator is optimized for frequencies of 500kHz and below. Operating internal clock frequencies above 500kHz result in measurement accuracy errors due to the modulator not having enough time to settle.

Suppose an external clock frequency of 1.0MHz is applied with a divide by 8 internal frequency setting, the system clock speed is 125kHz or 4x slower than internal system clock. The acquisition times for this example will increase by 4. For a S(B)ADC setting of 3, the ISL28022 will have an acquisition time of 2.032ms instead of 508µs.

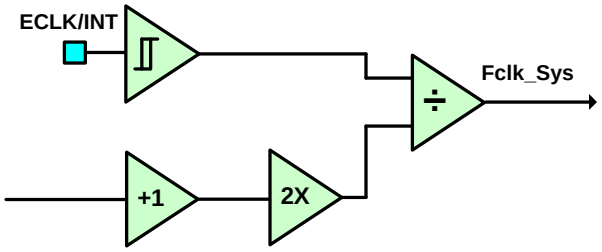


FIGURE 36. SIMPLIFIED INTERNAL BLOCK CONNECTION OF THE ECLK/INT PIN

The ECLK/INT pin connects to a buffer that drives a D-flip flop. Figure 36 illustrates a simple schematic of the ECLK/INT pin internal connection. The series of divide by 2 configured D-flip flops are controlled by the CLKDIV bits from the Aux Control Register. The buffer is a Schmitt triggered buffer. The bandwidth of the buffer is 4MHz. Figure 37 shows the bandwidth of the ECLK/INT pin.

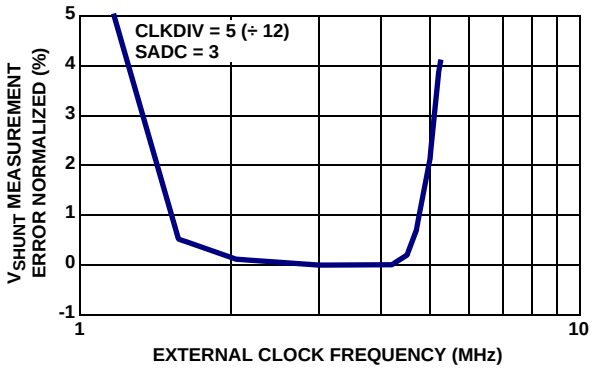


FIGURE 37. EXTERNAL CLOCK BANDWIDTH vs MEASUREMENT ACCURACY

The V_{SHUNT} measurement error degrades at ECLK frequencies above 4MHz. It is recommended that the ECLK does not exceed 4MHz. At ECLK frequencies below 2.5MHz or internal clock frequencies of 208kHz, the clock frequency to modulator is too slow allowing the charged capacitors to discharge due to parasitic leakages. The capacitor discharge results in a measurement error.

Over-ranging

It is not recommended to operate the ISL28022 outside the set voltage range. In the event of measuring a shunt voltage beyond the maximum set range (300mV) and lower than the clamp voltage of the protection diode (1V), the measured output reading may be within the accepted range but will be incorrect.

Shunt Resistor Selection

In choosing a sense resistor, the following resistor parameters needs to be considered; the resistor value, the resistor temperature coefficient and the resistor power rating.

The sense resistor value is a function of the full scale voltage drop across the shunt resistor and the maximum current measured for the application. The ISL28022 has 4 voltage ranges that are controlled by programming the PGA bits within the configuration register. The PGA bits control the voltage range for the V_{SHUNT} input (VINP-VINM) of the ISL28022. Once the voltage range for the input is chosen and the maximum measurable current is known, the sense resistor value is calculated using Equation 11:

$$R_{sense} = \frac{V_{shunt\_range}}{Imeas_{Max}} \quad \text{(EQ. 11)}$$

In choosing a sense resistor, the sense resistor power rating should be taken into consideration. The physical size of a sense resistor is proportional to the power rating of the resistor. The maximum power rating for the measurement system is calculated as the V_{shunt_range} multiplied by the maximum measurable current expected. The power rating equation is represented by Equation 12:

$$P_{res\_rating} = V_{shunt\_range} \cdot Imeas_{Max} \quad \text{(EQ. 12)}$$

A general rule of thumb is to multiply the power rating calculated in Equation 12 by 2. This allows the sense resistor to survive an event when the current passing through the shunt resistor is greater than the measurable maximum current. The higher the ratio between the power rating of the chosen sense resistor and the calculated power rating of the system (Equation 12), the less the resistor will heat up in high-current applications.

The temperature coefficient (TC) of the sense resistor directly degrades the current measurement accuracy. The surrounding temperature of the sense resistor and the power dissipated by the resistor will cause the sense resistor value to change. The change in resistor temperature with respect to the amount of current that flows through the resistor, is directly proportional to the ratio of the power rating of the resistor versus the power being dissipated. A change in sense resistor temperature results in a change in sense resistor value. Overall, the change in sense resistor value contributes to the measurement accuracy for the system. The change in a resistor value due to a temperature rise can be calculated using Equation 13:

$$\Delta R_{sense} = R_{sense} \cdot Rsense_{TC} \cdot \Delta Temperature \quad \text{(EQ. 13)}$$

ΔTemperature is the change in temperature in Celsius. $Rsense_{TC}$ is the temperature coefficient rating for a sense resistor. R_{sense} is the resistance value of the sense resistor at the initial temperature.

Table 22 is a shunt resistor reference table for select full scale current measurement ranges ($Imeas_{Max}$). The table also provides the minimum rating for each shunt resistor.

TABLE 22. SHUNT RESISTOR VALUES AND POWER RATINGS FOR SELECT MEASURABLE CURRENT RANGES

R_{sense}/ P_{rating}	V_{SHUNT} RANGE (PGA SETTING)			
$Imeas_{Max}$	(PGA 00) 40mV	(PGA 01) 80mV	(PGA 10) 160mV	(PGA 11) 300mV
100µA	400Ω/4µW	800Ω/8µW	1.6kΩ/16µW	3kΩ/ 30µW
1mA	40Ω/40µW	80Ω/80µW	160Ω/160µW	300Ω/ 300µW
10mA	4Ω/400µW	8Ω/800µW	16Ω/1.6mW	30Ω/ 3mW
100mA	400mΩ/ 4mW	800mΩ/8mW	1.6Ω/16mW	3Ω/ 30mW
500mA	80mΩ/ 20mW	160mΩ/40mW	320mΩ/ 80mW	600mΩ/ 150mW
1A	40mΩ/ 40mW	80mΩ/80mW	160mΩ/ 160mW	300mΩ/ 300mW
5A	8mΩ/ 200mW	16mΩ/400mW	32mΩ/ 800mW	60mΩ/ 1.5W
10A	4mΩ/ 400mW	8mΩ/800mW	16mΩ/1.6W	30mΩ/ 3W
50A	0.8mΩ/2W	1.6mΩ/4W	3.2mΩ/8W	6.0mΩ/ 15W
100A	0.4mΩ/4W	0.8mΩ/8W	1.6mΩ/16W	3mΩ/ 30W
500A	0.08mΩ/20W	0.16mΩ/40W	0.32mΩ/80W	0.6mΩ/ 150W

It is often hard to readily purchase shunt resistor values for a desired measurable current range. Either the value of the shunt resistor does not exist or the power rating of the shunt resistor is too low. A means of circumventing the problem is to use two or more shunt resistors in parallel to set the desired current measurement range. For example, an application requires a full scale current of 50A with a maximum voltage drop across the shunt resistor of 40mV. Table 22 shows this requires a sense resistor of 0.8mΩ, 2W resistor. Assume the power ratings and the shunt resistor values to choose from are 1mΩ/ 1W, 2mΩ /1W, and 4mΩ /1W.

Let's use a 1mΩ and a 4mΩ resistor in parallel to create the shunt resistor value of 0.8mΩ. Figure 38 shows an illustration of the shunt resistors in parallel.

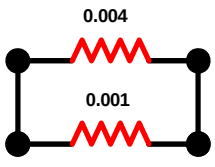


FIGURE 38. A SIMPLIFIED SCHEMATIC ILLUSTRATING THE USE OF TWO SHUNT RESISTORS TO CREATE A DESIRED SHUNT VALUE

The power to each shunt resistor should be calculated before calling a solution complete. The power to each shunt resistor is calculated using Equation 14:

$$P_{shuntRes} = \frac{V_{shunt\_range}^{2}}{R_{sense}} \quad \text{(EQ. 14)}$$

The power dissipated by the 1mΩ resistor is 1.6W. 400mW is dissipated by the 4mΩ resistor. 1.6W exceeds the rating limit of 1W for the 1mΩ sense resistor. Another approach would be to use three shunt resistors in parallel as illustrated in Figure 39.

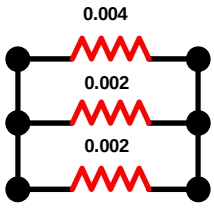


FIGURE 39. INCREASING THE NUMBER OF SHUNT RESISTORS IN PARALLEL TO CREATE A SHUNT RESISTOR VALUE REDUCES THE POWER DISSIPATED BY EACH SHUNT RESISTOR

Using Equation 14, the power dissipated to each shunt resistor yields 0.8W for the 2mΩ shunt resistors and 0.4W for the 4mΩ shunt resistor. All shunt resistors are within the specified power ratings.

Lossless Current Sensing (DCR)

A DCR sense circuit is an alternative to a sense resistor. The DCR circuit utilizes the parasitic resistance of an inductor to measure the current to the load. A DCR circuit remotely measures the current through an inductor. The lack of components in series with the regulator to the load makes the circuit lossless.

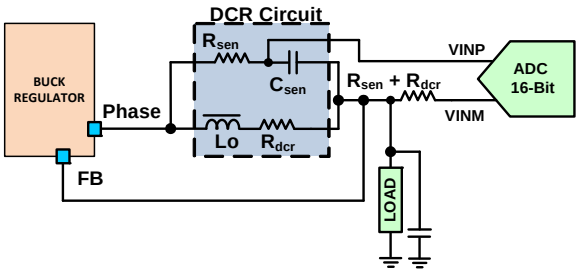


FIGURE 40. A SIMPLIFIED CIRCUIT EXAMPLE OF A DCR

A properly matched DCR circuit has an equivalent circuit seen by the ADC equals to R_{dcr} in Figure 40. Before deriving the transfer function between the inductor current and voltage seen by the ISL28022, let's review the definition of an inductor and capacitor in the Laplacian domain.

$$X_C(f) = \frac{1}{j\cdot\omega(f)\cdot C} \qquad X_L(f) = j\cdot\omega(f)\cdot L \quad \text{(EQ. 15)}$$

X_C is the impedance of a capacitor related to the frequency and X_L is the impedance of an inductor related to frequency. ω equals to 2*π*f. f is the chop frequency dictated by the regulator. Using Ohms law, the voltage across the DCR circuit in terms of the current flowing through the inductor is defined in Equation 16.

$$V_{dcr}(f) = \left(R_{dcr} + j\cdot\omega(f)\cdot L\right)\cdot i_L \quad \text{(EQ. 16)}$$

In Equation 16, R_{dcr} is the parasitic resistance of the inductor. The voltage drop across the inductor (Lo) and the resistor (R_{dcr}) circuit is the same as the voltage drop across the resistor (R_{sen}) and the capacitor (C_{sen}) circuit. Equation 17 defines the voltage across the capacitor (V_{csen}) in terms of the inductor current (I_L).

$$V_C(F) = \left[\frac{\left(j\cdot\omega(f)\cdot L + R_{dcr}\right)}{1 + j\cdot\omega(f)\cdot C_{sen}\cdot R_{sen}}\right]\cdot I_L = R_{dcr}\cdot\left[\frac{\left[1 + \frac{(j\cdot w(f)\cdot L)}{R_{dcr}}\right]}{1 + j\cdot\omega(f)\cdot C_{sen}\cdot R_{sen}}\right]\cdot I_L \quad \text{(EQ. 17)}$$

The relationship between the inductor load current (I_L) and the voltage across capacitor simplifies if the following component selection holds true:

$$\frac{L}{R_{dcr}} = C_{sen}\cdot R_{sen} \quad \text{(EQ. 18)}$$

If Equation 18 hold true, the numerator and denominator of the fraction in Equation 17 cancels reducing the voltage across the capacitor to the equation represented in Equation 19.

$$V_C = R_{dcr}\cdot i_L \quad \text{(EQ. 19)}$$

Most inductor datasheets will specify the average value of the R_{dcr} for the inductor. R_{dcr} values are usually sub 1mΩ with a tolerance averaging 8%. Common chip capacitor tolerances average to 10%.

Inductors are constructed out of metal. Metal has a high temperature coefficient. The temperature drift of the inductor value could cause the DCR circuit to be un-tuned. An un-tuned circuit results in inaccurate current measurements along with a chop signal bleeding into the measurement. To counter the temperature variance, a temperature sensor may be incorporated into the design to track the change in component values.

A DCR circuit is good for gross current measurements. As discussed, inductors and capacitors have high tolerances and are temperature dependent which will result in less than accurate current measurements.

In Figure 40, there is a resistor in series with the ISL28022 negative shunt terminal, VINM, with the value of R_{sen} + R_{dcr}. The resistor's purpose is to counter the effects of the bias current from creating a voltage offset at the input of the ADC.

Layout

The layout of a current measuring system is equally important as choosing the correct sense resistor and the correct analog converter. Poor layout techniques can result in severed traces, signal path oscillations, magnetic contamination, which all contribute to poor system performance.

TRACE WIDTH

Matching the current carrying density of a copper trace with the maximum current that will pass through is critical in the performance of the system. Neglecting the current carrying capability of a trace will result in a large temperature rise in the trace, and the loss in system efficiency due to the increase in resistance of the copper trace. In extreme cases, the copper trace could be severed because the trace could not pass the current. The current carrying capability of a trace is calculated using Equation 20:

$$\text{Trace}_{\text{width}} = \frac{\left(\frac{\text{Imax}}{k \cdot \Delta T^{0.44}}\right)^{\frac{1}{0.725}}}{\text{Trace}_{\text{Thickness}}} \quad \text{(EQ. 20)}$$

I_{max} is the largest current expected to pass through the trace. ΔT is the allowable temperature rise in Celsius when the maximum current passes through the trace. $\text{Trace}_{\text{Thickness}}$ is the thickness of the trace specified to the PCB fabricator in mils. A typical thickness for general current carrying applications (<100mA) is 0.5oz copper or 0.7mils. For larger currents, the trace thickness should be greater than 1.0oz or 1.4mils. A balance between thickness, width and cost needs to be achieved for each design. The coefficient k in Equation 20 changes depending on the trace location. For external traces, the value of k equals 0.048 while for internal traces the value of k reduces to 0.024. The k values and Equation 20 are stated per the ANSI IPC-2221(A) standards.

TRACE ROUTING

It is always advised to make the distance between voltage source, sense resistor and load as close as possible. The longer the trace length between components will result in voltage drops between components. The additional resistance will reduce the efficiency of a system.

The bulk resistance, ρ, of copper is 0.67µΩ/in or 1.7µΩ/cm at +25°C. The resistance of trace can be calculated from Equation 21:

$$R_{\text{trace}} = \rho \cdot \frac{\text{Trace}_{\text{length}}}{\text{Trace}_{\text{width}} \cdot \text{Trace}_{\text{thickness}}} \quad \text{(EQ. 21)}$$

Figure 41 illustrates each dimension of a trace.

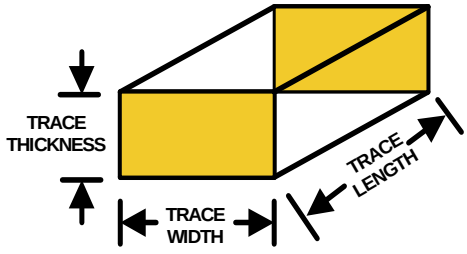


FIGURE 41. ILLUSTRATION OF THE TRACE DIMENSIONS FOR A STRIP LINE TRACE

For example, assume a trace has 2oz of copper or 2.8mil thickness, a width of 100mil and a length of 0.5in. Using Equation 21, the resistance of the trace is approximately 2mΩ.

Assume 1A of current is passing through the trace. A 2mV voltage drop would result from trace routing.

Current flowing through a conductor will take the path of least resistance. When routing a trace, avoid orthogonal connections for current bearing traces.

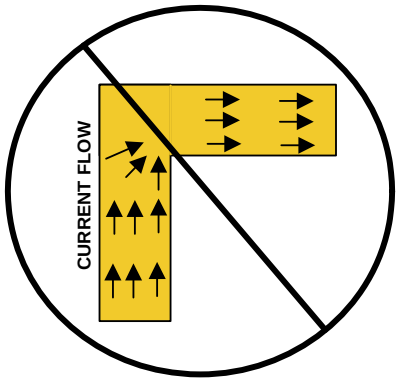


FIGURE 42. AVOID ROUTING ORTHOGONAL CONNECTIONS FOR TRACES THAT HAVE HIGH CURRENT FLOWS

Orthogonal routing for high current flow traces will result in current crowding, localized heating of the trace and a change in trace resistance (see Figure 42).

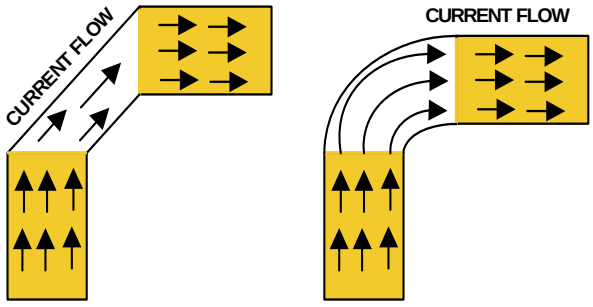


FIGURE 43. AVOID ROUTING ORTHOGONAL CONNECTIONS FOR TRACES THAT HAVE HIGH CURRENT FLOWS

The utilization of arcs and 45° traces in routing large current flow traces will maintain uniform current flow throughout the trace. Figure 43 illustrates the routing technique.

CONNECTING SENSE TRACES TO THE CURRENT SENSE RESISTOR

Ideally, a 4 terminal current sense resistor would be used as the sensing element. Four terminal sensor resistors can be hard to find in specific values and in sizes. Often a two terminal sense resistor is designed into the application.

Sense lines are high impedance by definition. The connection point of a high impedance line reflects the voltage at the intersection of a current bearing trace and a high impedance trace. The high impedance trace should connect at the intersection where the sense resistor meets the landing pad on the PCB. The best place to make current sense line connection is on the inner side of the sense resistor footprint. The illustration of the connection is shown in Figure 44. Most of the current flow is at the outer edge of the footprint. The current ceases at the point the sense resistor connects to the landing pad. Assume the sense resistor connects at the middle of the each landing pad, this leaves the inner half of the each landing pad with little current flow. With little current flow, the inner half of each landing pad is classified as high impedance and perfect for a sense connection.

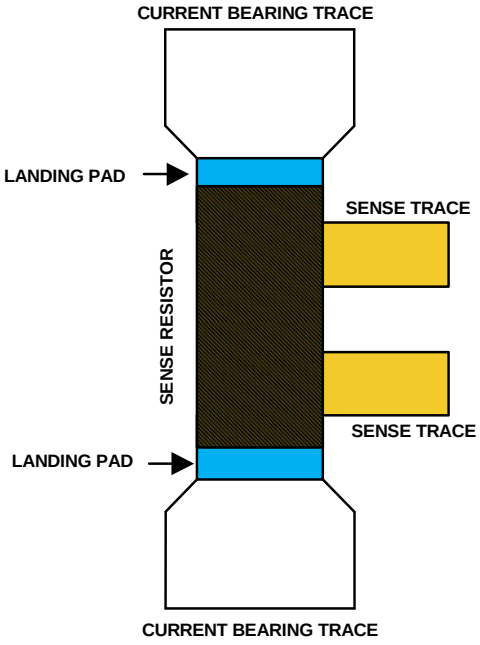
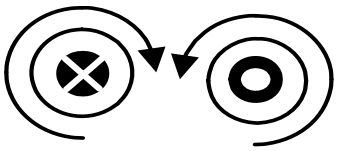


FIGURE 44. CONNECTING THE SENSE LINES TO A CURRENT SENSE RESISTOR

Current sense resistors are often smaller than the width of the traces that connect to the footprint. The trace connecting to the footprint is tapered at a 45° angle to control the uniformity of the current flow.

MAGNETIC INTERFERENCE

The magnetic field generated from a trace is directly proportional to the current passing through the trace and the distance from the trace the field is being measured at. Figure 45 illustrates the direction the magnetic field flows versus current flow.



$$B = \frac{\mu_o \cdot I}{2 \cdot \pi \cdot r}$$

FIGURE 45. THE CONDUCTOR ON THE LEFT SHOWS THE MAGNETIC FIELD FLOWING IN A CLOCKWISE DIRECTION FOR CURRENTS FLOWING INTO THE PAGE. A CURRENT FLOW OUT OF THE PAGE HAS A COUNTER CLOCKWISE MAGNETIC FLOW

The Equation in Figure 45 determines the magnetic field, B, the trace generates in relation to the current passing through the trace, I, and the distance the magnetic field is being measured from the conductor, r. The permeability of air, μ_o, is $4\pi*10^{-7}$ H/m.

When routing high-current traces, avoid routing high impedance traces in parallel with high-current bearing traces. A means of limiting the magnetic interference from high-current traces is to closely route the paths connected to and from the sense resistor. The magnetic fields will cancel outside the two traces and add between the two traces. Figure 46 illustrates a layout that is less sensitive to magnetic field interference.

If possible, do not cross traces with high-current. If a trace crossing cannot be avoided, cross the trace in an orthogonal manor and the furthest layer from the current bearing trace. The interference from the current bearing trace will be limited.

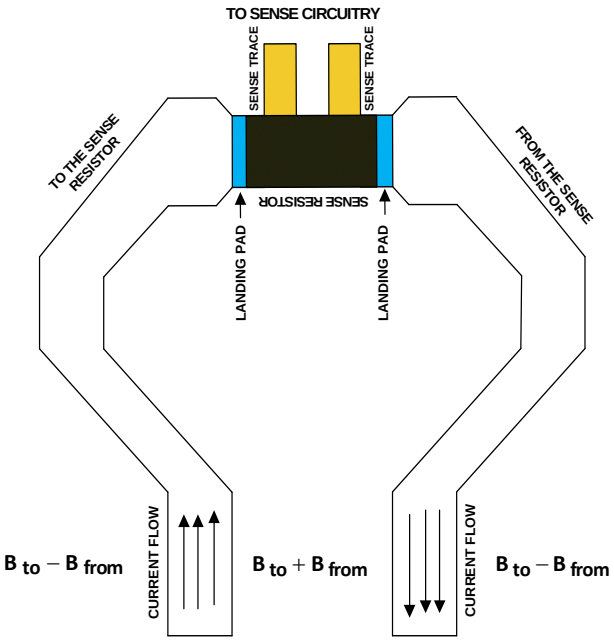


FIGURE 46. CLOSELY ROUTED TRACES THAT CONNECT TO THE SENSE RESISTOR REDUCES THE MAGNETIC INTERFERENCE SOURCED FROM THE CURRENT FLOWING THROUGH THE TRACES

A Trace as a Sense Resistor

In previous sections, the resistance and the current carrying capabilities of a trace were discussed. In high current sense applications, a design may utilize the resistivity of a current sense trace as the sense resistor. This section will discuss how to design a sense resistor from a copper trace.

Suppose an application needs to measure current up to 200A. The design requires the least amount of voltage drop for maximum efficiency. The full scale voltage range of 40mV (PGA 00) is chosen. From Ohms law, the sense resistor is calculated to be 200µΩ. The power rating of the resistor is calculated to be 8W. Assume the PCB trace thickness of the board equals 2oz/2.8mils and the maximum temperature rise of the trace is 20°C. Using Equation 20, the calculated trace width is 2.192in. The trace width, thickness and the desired sense resistor value is known. Utilizing Equation 21, the trace length is calculated to be 1.832in.

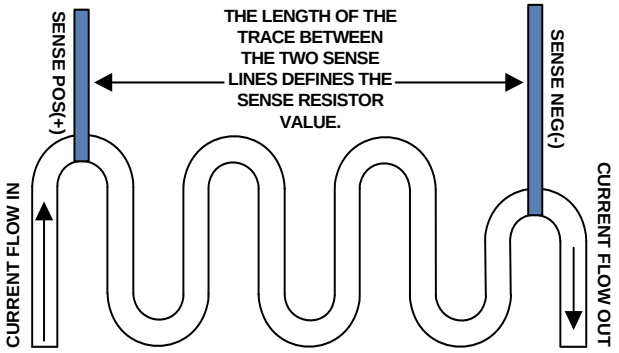


FIGURE 47. ILLUSTRATES A LAYOUT EXAMPLE OF A CURRENT SENSE RESISTOR MADE FROM A PCB TRACE

Figure 47 illustrates a layout example of a current sense resistor defined by a PCB trace. The serpentine pattern of the resistor reduces current crowding as well as limiting the magnetic interference caused by the current flowing through the trace.

The width of the trace in Figure 47 illustration would equal 2.192in and the length between the sense lines equals 1.832in.

The width of the resistor is long for some applications. A means of shortening the trace width is to connect two traces in parallel. For calculation ease, assume the resistive traces are routed on the outside layers of a PCB. Using Equations 20 and 21, the width of the trace is reduced from 2.192in to 1.096in.

When using multiple layers to create a trace resistor, use multiple vias to keep the trace potentials between the two conductors the same. Vias are highly resistive compared to a copper trace. Multiple vias should be employed to lower the voltage drop due to current flowing through resistive vias. Figure 48 illustrates a layout technique for a multiple layered trace sense resistor.

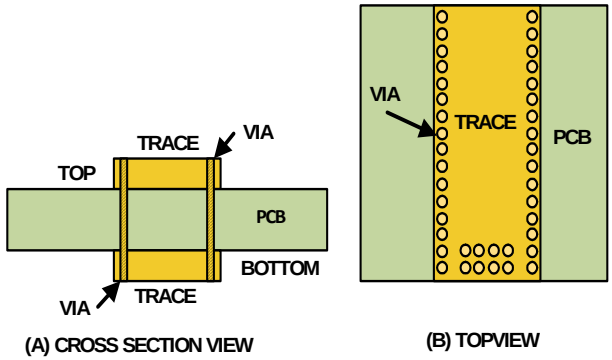


FIGURE 48. ILLUSTRATES A LAYOUT EXAMPLE OF A MULTIPLE LAYER TRACE RESISTOR

Typical Applications

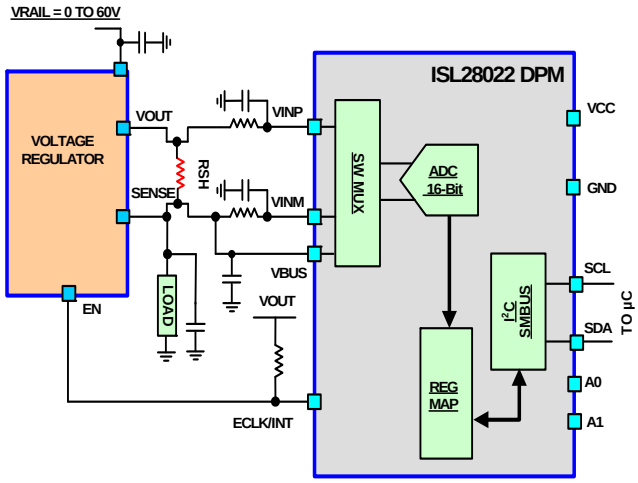


FIGURE 49. POINT OF LOAD MONITORING DESIGN IDEA

Point Of Load Power Monitor

The circuit illustrated in Figure 49 is a solution that can be used to monitor a load's performance. The voltage regulator regulates to a point of load (POL) voltage. 5V, 3.3V, 2.5V and 1.8V are examples of POL voltages.

The main bus voltage applied to the voltage regulator regulates the voltage to the load at the VINM, VBUS and Sense node for the configuration shown in Figure 49. The shunt resistor in the circuit allows the current to be monitored while regulating the voltage to the load. The maximum shunt voltage the ISL28022 is able to measure is ±300mV. The shunt resistor value is determined by the Equation 22:

$$R_{shunt} = RSH = \frac{0.30}{Current_{FS}} \quad \text{(EQ. 22)}$$

$Current_{FS}$ is the maximum current to be measured through the load. This is chosen by the user.

The ISL28022 has over/undervoltage (OV/UV) sensing circuitry for the Bus and Shunt inputs. The levels of the error detection

circuitry are controlled digitally via an I^2C/SMBus interface. The status of each inputs' error detection can be read digitally via a register. The ISL28022 allows for the summation of error detection bits to be routed to an interrupt pin. For the Point Of Load Monitoring circuit shown in Figure 49, the interrupt pin is connected to the enable pin of the regulator. In a fault condition, the ISL28022 will trigger an interrupt causing the voltage regulator to shut down. When a fault exists, the ISL28022 interrupt pin output state can be digitally programmed.

The ISL28022 calculates the power and current internally and stores the results in an internal register. The V_{bus} connected directly to the load, enables a measurement system that monitors power to the load.

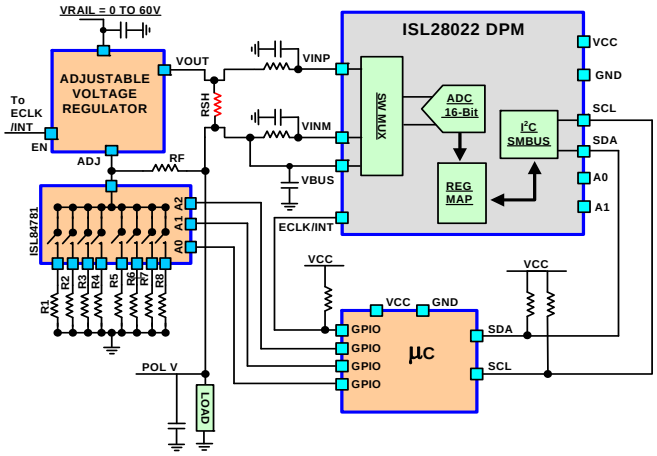


FIGURE 50. ADJUSTABLE POINT OF LOAD MONITORING DESIGN IDEA

Adjustable Point Of Load Monitor

Many applications require unique voltages to optimize a circuit's potential. Figure 50 is a microcontroller selectable point of load (POL) circuit. The circuit is very similar to the POL monitor discussed previously. The general purpose input output bits (GPIO) of the microcontroller controls a multiplexer which connects a gain setting resistor to the adjust (ADJ) pin of the regulator. The feedback resistance (RF), the multiplexer switch resistance and the value of the gain setting resistor (R_1 to R_8) determine the regulated output voltage (POL V) to the load. Equation 23 is a generic formula to determine the regulated POLV.

$$POL\_V = \alpha \cdot \left(\frac{R_F}{R_x + R_{mux}} + 1 \right) \quad \text{(EQ. 23)}$$

The coefficient alpha, α, is dependent on the designed in regulator. For the ISL80101-ADJ, α equals 0.5. R_x is the value of the gain resistor (R1 to R8) selected by the microcontroller. R_{mux} is multiplexer switch resistor value. The multiplexer switch resistance is a function of the current flowing through the switch. A general practice is to choose resistor values such that current flowing through the multiplexer is small. The ISL84781 has an on-resistance of 0.4Ω.

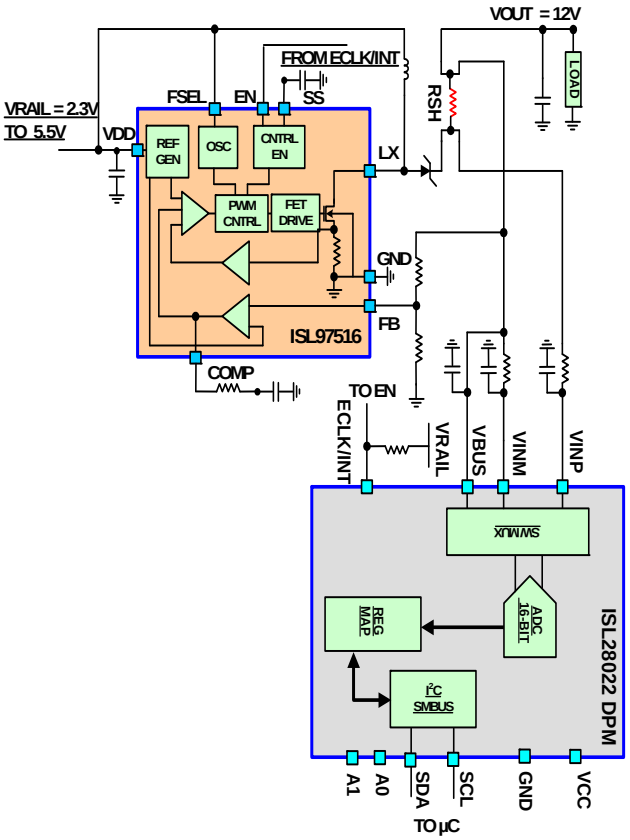


FIGURE 51. POWER MONITOR BOOST REGULATOR DESIGN IDEA

Power Monitor Boost Regulation

The Power Monitor Boost Regular application is an example of the ISL28022 used as a digital helper (Figure 51). With minimal circuitry, the ISL28022 enables smart designs that digitally monitor the electrical parameters to a load. Alternative designs require a current amplifier paired with an ADC. The ADC chosen is often not compliant to common communication standards, such as I^2C. The ISL28022 solves this problem and allows for 16 devices on a single I^2C bus.

The ISL97516 chip is a high efficiency step-up voltage regulator. The maximum peak inductor current the regulator can deliver is 2.0A. If more output current is needed, the ISL97656 is rated for 4.0A maximum peak inductor current. For this particular application, the ISL97516 is configured to step up the voltage at the VDD pin to 12V. The voltage at VDD can range from 2.3V to 5.5V for normal 12V regulated operation. A USB power pin could be used to drive the ISL97516.

The regulation node of the circuit, shown in Figure 51 is at V_{OUT}. The ISL97516 has feedback circuitry that removes the current sense resistor, RSH, from impacting the regulation voltage. The current sense resistor is calculated using Equation 22. Equation 22 on page 28 shows the formula used to calculate R_{shunt}.

The ISL28022 interrupt pin is connected to the Enable pin of the regulator. The ISL28022 has OV/UV alerts for both the Bus and Shunt channels. A fault condition from either channel powers down the voltage regulator.

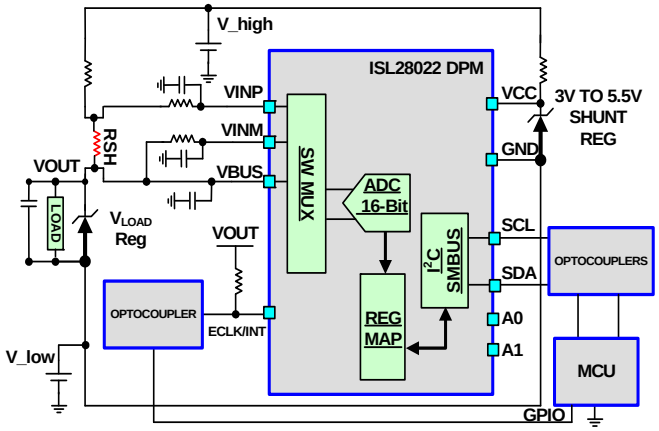


FIGURE 52. FLOATING SUPPLY DESIGN IDEA

Floating Supply DPM (>60V or <0V Operation)

The ISL28022 is operational when the potential of the measured circuitry is greater than the potential at the ground pin. In most applications the ground pin potential equals 0V. A zero potential ground reference limits the operating range of the ISL28022 to 0V to 60V. This application illustrates the connectivity of the DPM to measure and operate at potentials greater than 60V or less than 0V.

Assume an application that measures a -48V supply. The ground reference voltage of the system, V_low, equals -48V. V_high equals 0V for the example. The power supply voltage to the system is -48V. The load supply voltage is set by the voltage regulator, V_{LOAD} Reg. The regulator can be either a shunt or a linear regulator.

The voltage levels for I^2C communication lines are determined by V_low and the ISL28022 shunt regulator. A low voltage equals the V_low potential. A high level equals the summation of V_low and the Shunt Regulator voltage. For a -48V system with a 3.3V shunt regulator, a low voltage equals -48V and a high voltage level equals -44.7V. The voltage from the I^2C communication pins can not be directly connected to a ground referenced micro-controller. The optocouplers are used to translate the voltage level from the -48V referenced system to the ground referenced microcontroller system.

The ISL28022 measures voltage between two nodes. For the shunt input, the ISL28022 measures the voltage between VINP and VINM nodes. For the Bus input, the ISL28022 measures the difference between V_{bus} and GND nodes. The V_{bus} voltage for a floating system is calculated using Equation 24:

$$V_{bus} = V_{low} + \left(Vbus_{LSB} \cdot Vbus_{Reg}\right) \quad \text{(EQ. 24)}$$

V_{LOW} is the ground reference voltage of the system. In this instance, the value is -48V. $Vbus_{LSB}$ is the step size of the V_{bus} measurement, which equals 4mV. $Vbus_{Reg}$ is the integer value of the V_{bus} measurement reported by the ISL28022.

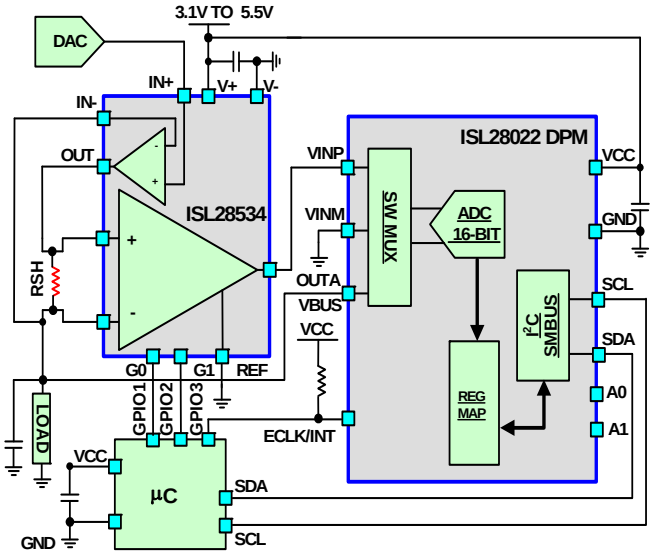


FIGURE 53. A SIMPLIFIED SCHEMATIC OF A FORCE VOLTAGE MEASURE VOLTAGE AND CURRENT CIRCUIT WITH LOW CURRENT DRIVE CAPABILITY

Force Voltage Measure Current and Voltage

Many applications require testing of components or validating a system's performance by utilizing circuits that force voltage and measure current and voltage to a specific connection point. The circuit in Figure 53 is a force voltage measure current and voltage circuit.

The digital-to-analog converter, DAC, is configured by the microcontroller. The DAC is either integrated into the microcontroller or a standalone discrete device depending on the level of precision needed. The output of the DAC is fed into the non-inverting input of the ISL28534. The ISL28534 is a chopper-stabilized single output instrumentation amplifier with an additional operational amplifier (op amp) integrated into the die. The allowable voltages that can be fed to the op amp are 0.1V to V+ - 0.1V. The allowable supply voltages to the circuit ranges from 3.1V to 5.5V. The integrated op amp regulates the voltage to the load while delivering current. The op amp can successfully regulate the programmed voltage up to 1mA. For greater than 1mA drive currents, an external operational amplifier with higher current may be needed. Another approach is to add a push-pull output stage between the output of the integrated op amp and the sense resistor. The push-pull output stage that enables higher drive capability for the circuit is shown in Figure 54.

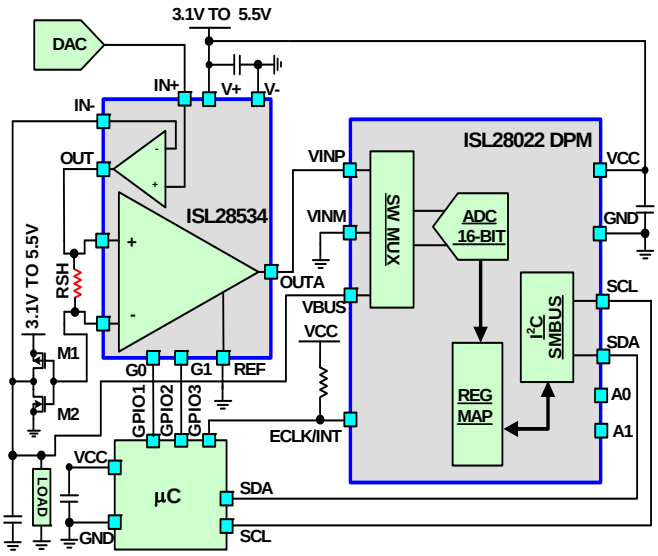


FIGURE 54. A SIMPLIFIED SCHEMATIC OF A FORCE VOLTAGE MEASURE VOLTAGE AND CURRENT CIRCUIT WITH A PUSH PULL OUTPUT STAGE

The addition of the power MOSFETs between the shunt resistor, RSH, and the load increases the drive current to the load. The MOSFETs are labeled M1 and M2 in Figure 54.

The feedback loop of the shunt resistor, RSH, and the power MOSFETs, M1 and M2, between the IN- terminal and Out terminal of the op amp, enhances the drive capability to the load. The IN- terminal regulates the voltage to the load, while the current is steered from 3.1V to 5V supply through the MOSFET, M1, to the load. The additional power stage limits the voltage delivered to the load.

Integrated into the ISL28534 is an instrumentation amplifier, IA, that can be configured to 1 of 9 gain ranges. The ISL28534 is one product of a family of six products. The products are differentiated by gain values and the number of outputs. The purpose of the instrumentation amplifier, IA, is to extend the measurable current range by using one sense resistor.

The ISL28534 gain selection spans from 1 to 1000. The voltage noise floor of the IA is 0.5µV at a high gain. The lowest voltage the IA can resolve is 1µV as a conservative value. The ISL28534 has an input offset current of 300pA at room temperature. The lowest current that can be measured is 500pA. The current value is dependent on the operational temperature range of the circuit.

The output of the IA connects to the shunt input (VINP, VINM) of the ISL28022. The full scale measurable range of the shunt input is ±300mV. Voltage readings that exceed 300mV in magnitude, require a reduction of gain in the IA setting. The ISL28022 digital comparators can be set to fire an interrupt for readings above 300mV. The interrupt can be routed to either the interrupt or a GPIO pin of the microcontroller. The connection allows the ISL28022 to notify the microcontroller to decrement the gain of the IA when the output reading of the IA exceeds 300mV.

If the minimum current to be measured is 500pA, what is the shunt resistor value, RSH, and the full scale current that the circuit can measure? The lowest measured current reading should occur at the IA's highest gain while the voltage drop across the shunt resistor equals the IA resolution voltage. The bounded criterion discussed determines the shunt resistor value. The shunt resistor value can be calculated using Equation 25:

$$R_{sense} = RSH = \frac{V_{IA\_Res}}{I_{min}} \quad \text{(EQ. 25)}$$

V_{IA_Res} is the resolution value of the IA, which equals 1µV for the application. I_{min} is the minimum current to be measured. The example shows I_{min} equals 500pA. The shunt resistor is calculated to be 2kΩ.

The full scale current of any IA gain setting can be calculated using Equation 26:

$$Current_{FS} = \frac{Vshunt\_range}{G_{IA} \cdot R_{sense}} \quad \text{(EQ. 26)}$$

G_{IA} is the IA gain setting. R_{sense} is the shunt resistor value, which equals 2kΩ for the giving example. V_{shunt_range} is the PGA range setting for the ISL28022. For example the shunt range setting value is 300mV. The full scale current range for the circuit occurs at an IA gain setting of 1. Using Equation 26, the measurable full scale current equals 150µA.

The least significant bit, LSB, for the shunt input equals 10µV for the ISL28022. The $current_{Lsb}$ can be calculated using Equation 27:

$$Current_{LSB} = \frac{Current_{FS}}{G_{IA} \cdot ADC_{res}} \quad \text{(EQ. 27)}$$

The ADC_{res} equals 2^{15} or 32768 for the example. The $Current_{FS}$ is calculated using Equation 26. The G_{IA} is the gain of the IA. The V_{bus} input of the ISL28022 is connected to the load allowing for power measurements. The V_{bus} can also be connected as an independent node. The power measurement value returned from the ISL28022 would be meaningless.

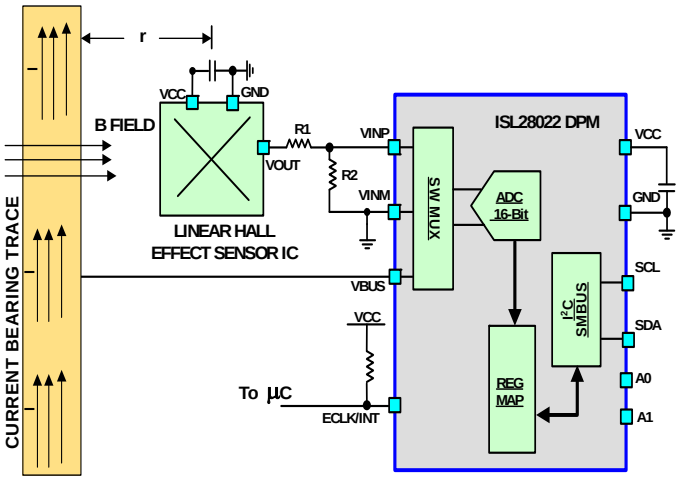


FIGURE 55. A SIMPLIFIED CIRCUIT DIAGRAM OF REMOTELY MEASURING CURRENT THROUGH A TRACE

A Lossless Current Sense Circuit

In measuring power to and from a system or load, the minimum voltage loss due to a sensing element and trace resistance is desired. The low voltage loss improves the efficiency of a system. The circuit in Figure 55 measures current through a trace by measuring the magnetic field, B, emitted from the current flowing through the trace. The B field is directly proportional to the magnitude and direction of the current flowing through the trace. The B field is perpendicular to the current flow. The direction of the B field with respect to current flow is illustrated in Figure 56.

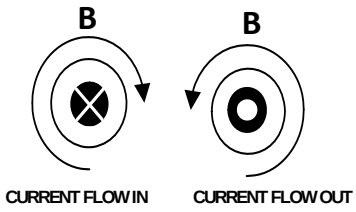


FIGURE 56. AN ILLUSTRATION OF CURRENT FLOW WITH RESPECT TO THE MAGNETIC FIELD DIRECTION

The mathematical relation between the magnitude of the current and the magnetic field is represented in Equation 28:

$$B = \frac{\mu_o \cdot I}{2 \cdot \pi \cdot r} \qquad I = \frac{2 \cdot \pi \cdot r \cdot B}{\mu_o} \qquad \text{(EQ. 28)}$$

μ_0 is the permeability of the magnetic field flow. The permeability value, μ_o, of free space equals $4\pi * 10^{-7}$ H/m. The value r is the distance in meters between the conductor and the linear hall effect sensor. The I is the current flowing in amps through the conductor. B is the magnetic field in Gauss.

CAUTION:

Every technology has drawbacks. The lossless current sense is no exception. Hall effect sensors measure the total available magnetic field at the set location. Current bearing traces routed near the sensor will change the magnetic field at the sensor and ultimately change the accuracy of the measurement. The sensor will also measure changes in the environmental magnetic field. This could be due to a switching motor or any device that radiates energy. A magnetic shield can encapsulate the current bearing trace of interest and the hall effect sensor to reduce the environmental interference the sensor is subjected to. The magnetic shield will change the gain between the current flowing in the trace and the output voltage of the sensor.

The resistor divider, R_1 and R_2, in Figure 55 attenuates the voltage from the linear hall effect sensor to the maximum voltage range, 300mV, of the ISL28022 V_{SHUNT} input (VINP, VINM). The V_{bus} input of the ISL28022 is connected to the current bearing trace allowing the ISL28022 to calculate power to the load.

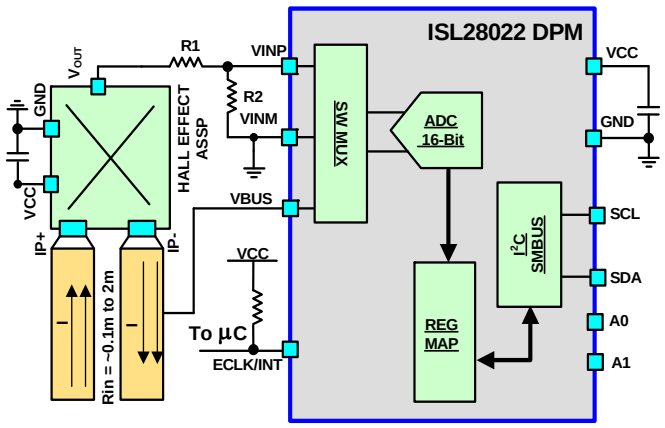


FIGURE 57. A SIMPLIFIED CIRCUIT DIAGRAM OF A HALL EFFECT SENSOR THAT INTEGRATES THE CURRENT CONDUCTION PATH

Improved Hall Effect Sensing

Recently, linear hall effect sensors that integrate the current conduction path, provide environmental shielding and temperature compensation circuitry in a single package have improved the drawbacks associated with the linear hall effect sensor. The integrated solution simplifies the gain calculation between the current flowing through the conductor and the output voltage. The single chip solution also simplifies the layout because the current bearing wire is a set distance from the hall effect sensor.

The integrated conduction path (IP+, IP-) has resistance ranging from 0.1mΩ to 2mΩ. The current sense in Figure 57 is not a lossless system.

The resistor divider, R1 and R2, in Figure 57 attenuates the voltage from the linear hall effect sensor to the maximum voltage range, 300mV, of the ISL28022 V_{SHUNT} input (VINP, VINM). The V_{bus} input of the ISL28022 is connected to the current bearing trace allowing the ISL28022 to calculate power to the load.

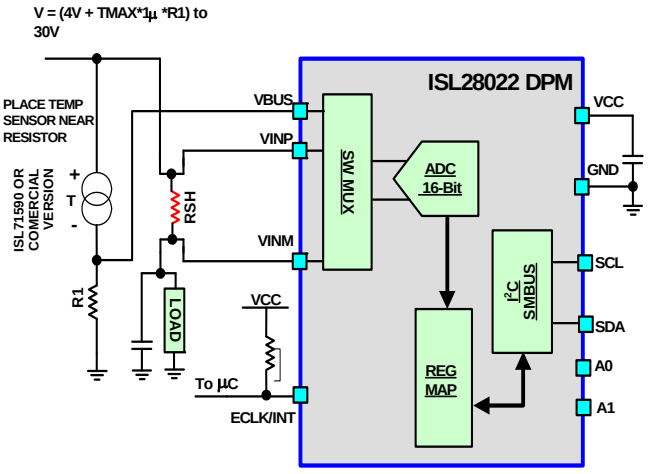


FIGURE 58. A SIMPLIFIED CIRCUIT DIAGRAM THAT MEASURES CURRENT AND TEMPERATURE

Precision Current Sense

The inaccuracies in most current sensing applications reside with either the sense resistor or the measurement system. The ISL28022 has a measurement accuracy of ±0.2% typically. Depending on the magnitude of the current to be sensed, the current sense resistor, RSH, is the least accurate device of the system. Applications that require large current measurements use small valued shunt resistors. The material composition of small resistors are often constructed with metal. Metal has a high temperature coefficient. Copper's temperature coefficient is 3862ppm/K. For a 50A current measurement system, the sense resistor value equals 0.8mΩ. Equation 29 is the relationship between Kelvin (K), Celsius (C) and Fahrenheit (F) temperatures.

$$C = \frac{5}{9}\cdot(F - 32) \qquad C = K - 273 \tag{EQ. 29}$$

Suppose a sense resistor, consisting of mostly metal, changes by 10°C. Assume the Temperature coefficient of the sense resistor is 600ppm/C. The change in shunt resistance for a 10°C rise is calculated using Equation 30:

$$R = R_0\cdot(1 + TC\cdot\Delta T) \tag{EQ. 30}$$

R_0 is the original value of the resistor at T which equals T_0 (0.8Ω). TC is the temperature coefficient of the shunt resistor (600ppm/C). ΔT is the change in temperature (10°C). The new resistance value of the shunt resistor is 0.8048mΩ. or a 0.6% change in resistance. The change in resistor value directly affects the measurement accuracy of the system.

Measuring the temperature change of the sense resistor with a known TC stabilizes the system accuracy measurement versus temperature. The simplified circuit in Figure 58 measures current and temperature. The ISL71590 or the commercial version of the part is a temperature sensor that outputs a current with respect to temperature. The output current changes 1µA/K.

Equation 31 is the temperature calculation with respect to a chosen r_{load} (R1) value.

$$T_C = \frac{V_{bus}}{1u\cdot R1} - 273 \tag{EQ. 31}$$

T_C is the temperature in centigrade. V_{bus} is the bus voltage measured across the R_1 resistor. The V_{bus} connects to the ISL28022. R_1 is the load resistor for the circuit. The temperature sensor needs at least 4V to operate. Equation 32 calculates the R_1 value that yields the largest temperature to voltage gain ratio.

$$R_1 = \frac{V - 4}{(T_{max} + 273)\cdot 1\cdot u} \tag{EQ. 32}$$

V is the voltage applied to the temperature sensor and the resistor. The temperature sensor requires a 4V drop across the sensor to be operational. T_{max} is the maximum temperature to be measured in centigrade.

Combustible Gas Sensor Circuit

The ISL28022 measures current by measuring a voltage across the shunt inputs (VINM, VINP). A 15-bit digital number representing the sense resistor value is stored in the calibration register. The ISL28022 divides the voltage measured across the shunt inputs by the calibration register value and stores the results in the current register.

In the combustible gas sensor application (Figure 59), the current measurement reading from the ISL28022 is not used. The voltage reading across the Wheatstone bridge determines the concentration of gas in the environment. The resistive network on the left leg of the Wheatstone bridge is a coarse null to the combustible gas sensor. The ISL95810 is a digitally controlled potentiometer (DCP). The DCP is used to fine tune the null potential to 0V across the shunt inputs for a known concentration of gas. In the event of a power interruption to the circuit, the ISL95810 has non-volatile memory integrated with the DCP. The DCP will default to the save memory position once power is resumed to the circuit.

The gain between the change in concentration and the change in volts varies between sensors and sensing gas. The ISL28022 has a digital comparator that can trigger an interrupt line when a voltage exceeds a set level. A set voltage threshold for the shunt input corresponds to a set gas level. When the concentration of gas exceeds a set level, the ISL28022 triggers an alarm causing the ECLK/INT pin to transition from VCC voltage level to ground. The ground potential activates the relay and disable power to the sensor circuit.

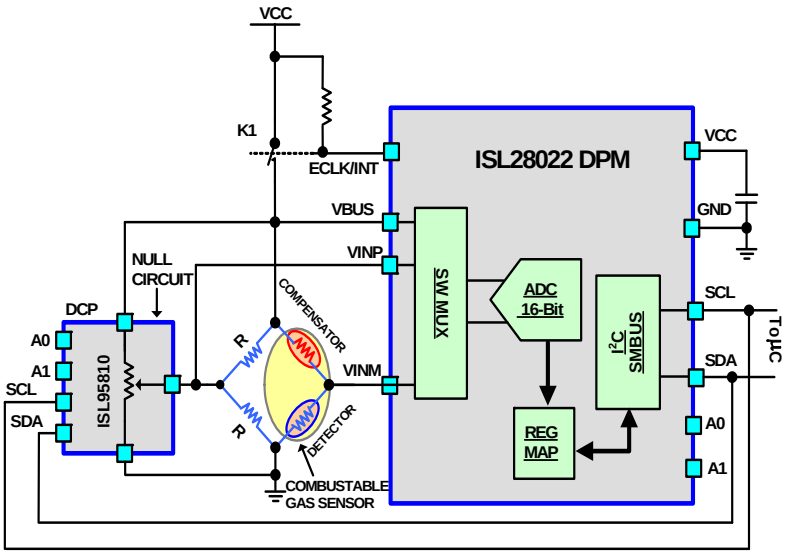


FIGURE 59. A SIMPLIFIED DIAGRAM OF A COMBUSTIBLE GAS SENSOR CIRCUIT USING THE ISL28022

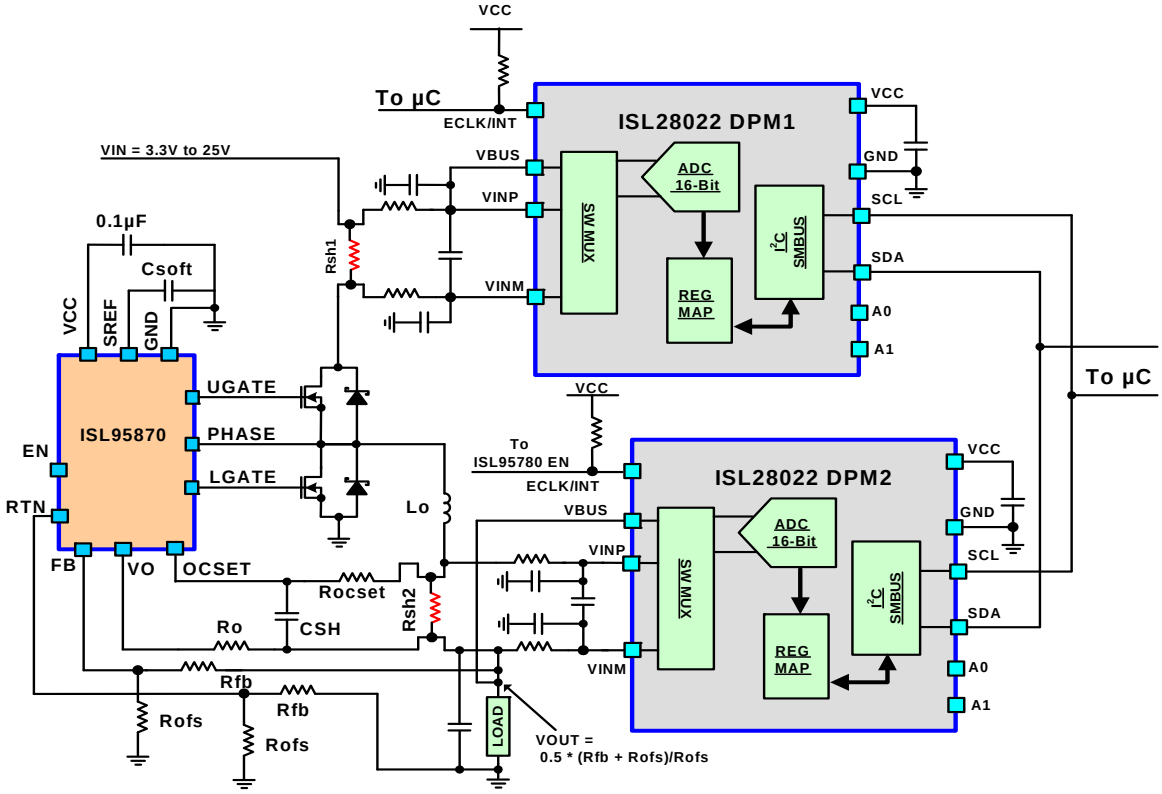


FIGURE 60. A SIMPLIFIED CIRCUIT THAT USES TWO ISL28022 TO MEASURE A SYSTEM EFFICIENCY

An Efficiency Measurement Using the ISL28022 Broadcast Feature

As energy costs rise and the world focuses on clean energy, there is a need for electronics to efficiently convert power delivered to a circuit into work performed. Power efficiency,η, is an electronic parameter use to quantify the efficiency of a system. Equation 33 defines the formula for power efficiency.

$$\eta = \left(\frac{P_{load}}{P_{total}} \right) \cdot 100 \quad \text{(EQ. 33)}$$

P_{total} is the power delivered to current leg prior to being converted.

In the electronics field, efficiency ratings are mostly associated with converting power from one form to another. Examples of power conversion circuitry are DC/DC converters, AC/ DC converters, buck/boost regulators and digital regulators. P_{load} is the power delivered to the load.

The simplified circuit in Figure 60 is an example of using two ISL28022s to measure the efficiency of a DC/DC converter (ISL95870). The first ISL28022, DPM1, measures the total power, P_{total}, for the circuit. DPM2 measures power to the load, P_{load}. DPM1 and DPM2 are connected to the same I^2C bus. The two ISL28022s can synchronously measure their respective signals by sending a broadcast trigger command sent to each device. A broadcast trigger command that instructs each ISL28022 device to measure both current and voltage is achieved by writing to the command register, register 0, using the slave address of 0x7F. The slave address 0x7F will write to all ISL28022s independent of address setting.

The command register, register 0, configures the range setting for both bus (BRNG) and shunt (PG) inputs and the sampling mode for the chip. The command register also configures the ADC sampling rate for both channels of the ISL28022. To successfully synchronize the ISL28022s to sample simultaneously, each ISL28022 has to have the same bus and shunt range and ADC acquisition settings.

Assume a bus range of 16V, a shunt range of 40mV and an ADC acquisition rate of 508µs for both channels. A single power acquisition will be made and the chip will sit idle. The command that is sent simultaneously to both chips is 0x7F, 0x00, 0x019B. The ranges for each input are for the lowest settings. PGA = BRNG = 0. The ADC acquisition rate is the same for both channels. SADC = BADC = 3 or 508µs. The setting for the mode bits is 3. Once the write command has been received and executed by the ISL28022, the ADC will begin converting the signal. The two ISL28022s should be synchronized as long the distance between master (microcontroller) and ISL28022 are roughly the same between the two ISL28022s.

Once the ADC has completed the conversion for both bus and shunt channels, the master should read register 3 of each ISL28022 serially.

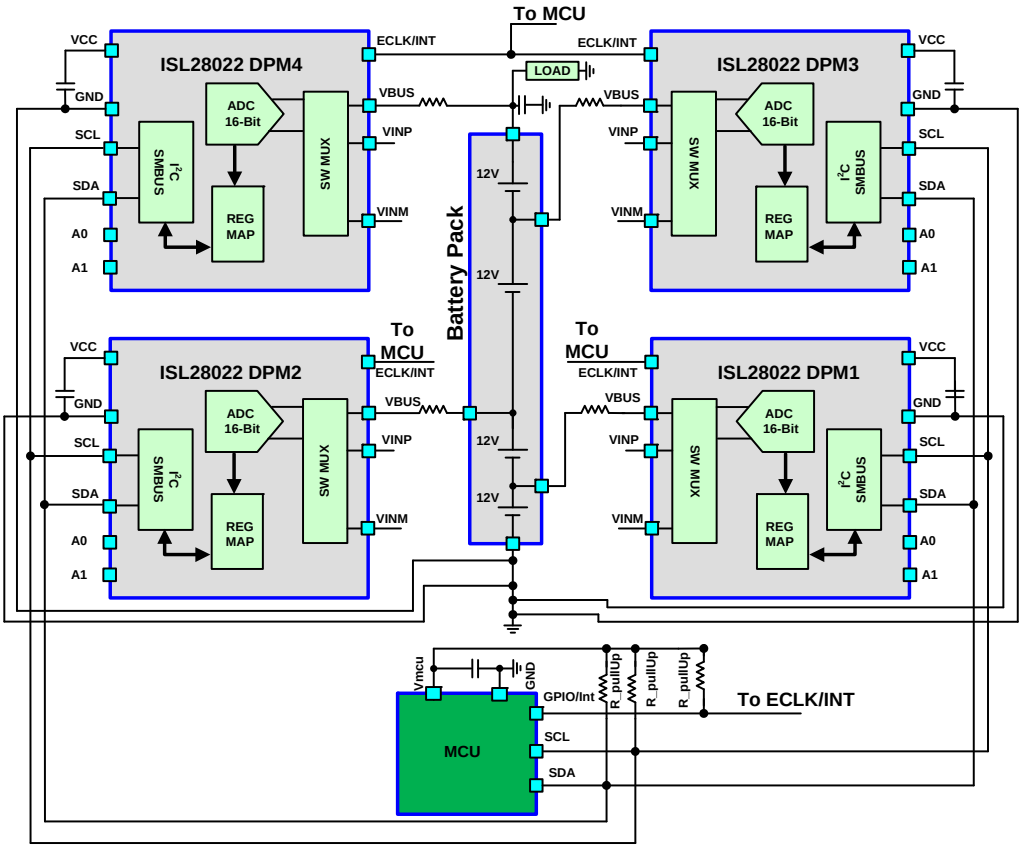


FIGURE 61. A SIMPLIFIED MULTICELL MONITORING CIRCUIT.

Monitoring MultiCell Battery Levels Using the ISL28022 Broadcast Command

There are many battery chemistries in today's marketplace. Each battery chemistry has its own unique benefits and drawbacks. For example, lithium ion batteries can deliver a lot of power to a load for an extended period of time but the technology comes with a cost due to the exotic materials used to construct the battery. Lithium ion cells degrade uniquely with each charge and discharge cycle. Lithium ion batteries often are paired with multicell balancing circuits to maximize battery life and discharge time.

Lead acid batteries are cheap and a mature technology. Lead acid batteries have a predictable and uniform degradation versus discharge and charging cycles. The batteries have more loss with respect to delivering power to a load. Many customers that use lead acid battery technology do not require multicell balancing but desire cell monitoring to determine the charge on the battery. It is similar to fuel gauge measurement.

Figure 61 is a simplified circuit that monitors each cell of a 48V battery pack. The ISL28022 can measure voltages up to 60V. The ground of each ISL28022 is referenced to the ground of the battery pack. The negative terminal of the V_{bus} input is the ground pin of the ISL28022. The ISL28022 has a unique feature that allows a master, microcontroller, to talk to all ISL28022s with one command. The use of the 0x7E slave address allows the master to write to all registers at once. The reading of the registers still has to be performed sequentially. The broadcast command allows the synchronization of measurements between two or more ISL28022.

Once a measurement has been retrieved by the master, each cell voltage is calculated by a series of subtractions.

Vcell1 = V_{bus}(DPM1)

Vcell2 = V_{bus}(DPM2) – V_{bus}(DPM1)

Vcell3 = V_{bus}(DPM3) – V_{bus}(DPM2)

Vcell4 = V_{bus}(DPM4) – V_{bus}(DPM3)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
June 9, 2014	FN8386.4	Equation 17 on page 25 added I_L before = R_{dcr} Figure 41 on page 26 changed "Of a Strip" to "For a Strip" Figure 46 on page 27 changed "Current flow" to "A current flow" Last sentence in paragraph following Figure 45 on page 27 and second sentence in paragraph under Equation 28 on page 32 changed "10^{7}" to "10^{-7}"
April 17, 2014	FN8386.3	Text revisions done in section "Signal Integrity" on page 22. Added section "Lossless Current Sensing (DCR)" on page 25 and "Monitoring MultiCell Battery Levels Using the ISL28022 Broadcast Command" on page 36. Updated the Ordering Information on page 4 by removing R-spec parts.
October 10, 2013	FN8386.2	Added sections from "Shunt Resistor Selection" on page 24 to "An Efficiency Measurement Using the ISL28022 Broadcast Feature" on page 35.
April 26, 2013	FN8386.1	Added R-spec parts to ordering information and updated verbiage in About Intersil.
April 16, 2013	FN8386.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

For additional products, see www.intersil.com/en/products.html

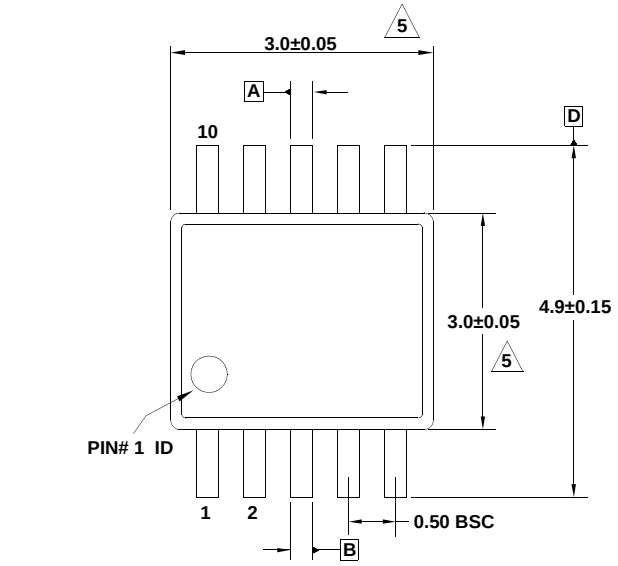
Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Package Outline Drawing

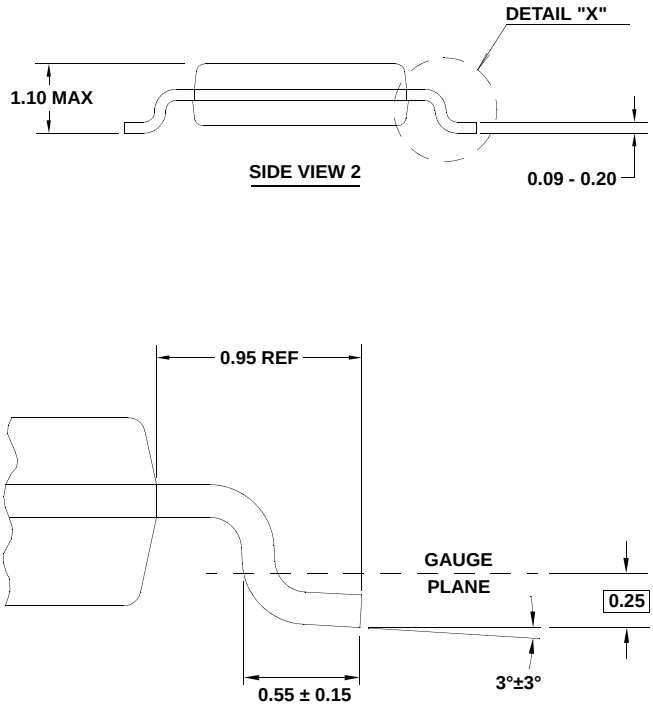
M10.118

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

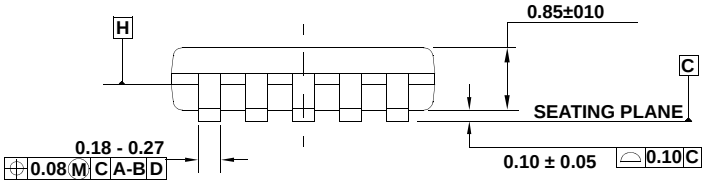
Rev 1, 4/12



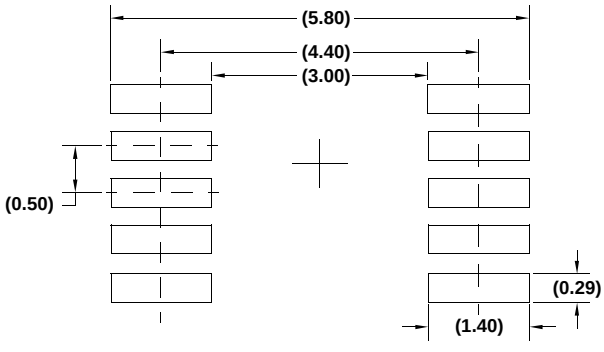
TOP VIEW



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

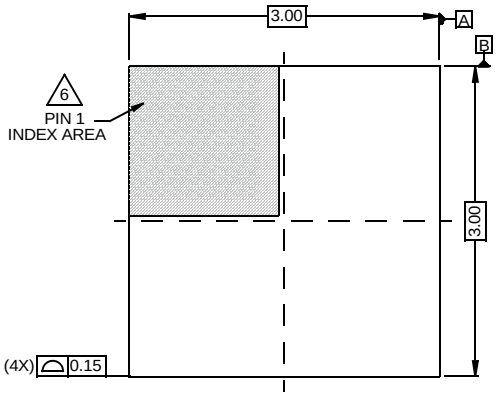
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

Package Outline Drawing

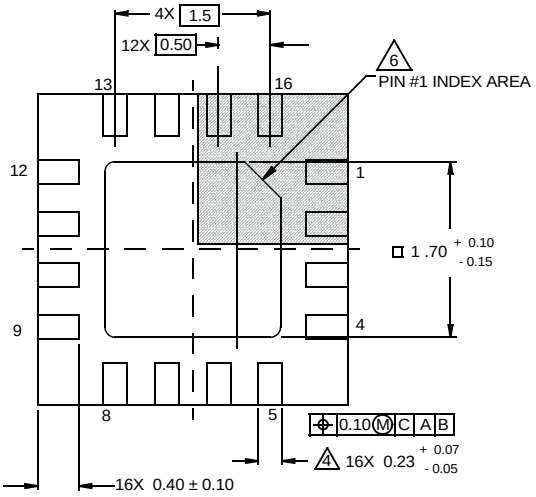
L16.3x3B

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

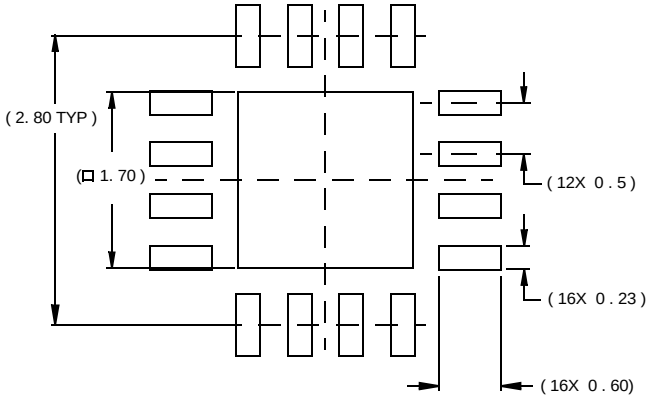
Rev 1, 4/07



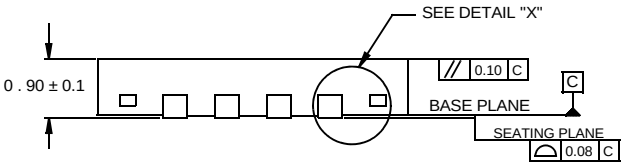
TOP VIEW



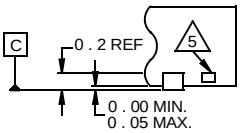
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.