



3.3V CMOS 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

IDT74ALVC16646

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16646:

- High Output Drivers: $\pm 24\text{mA}$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

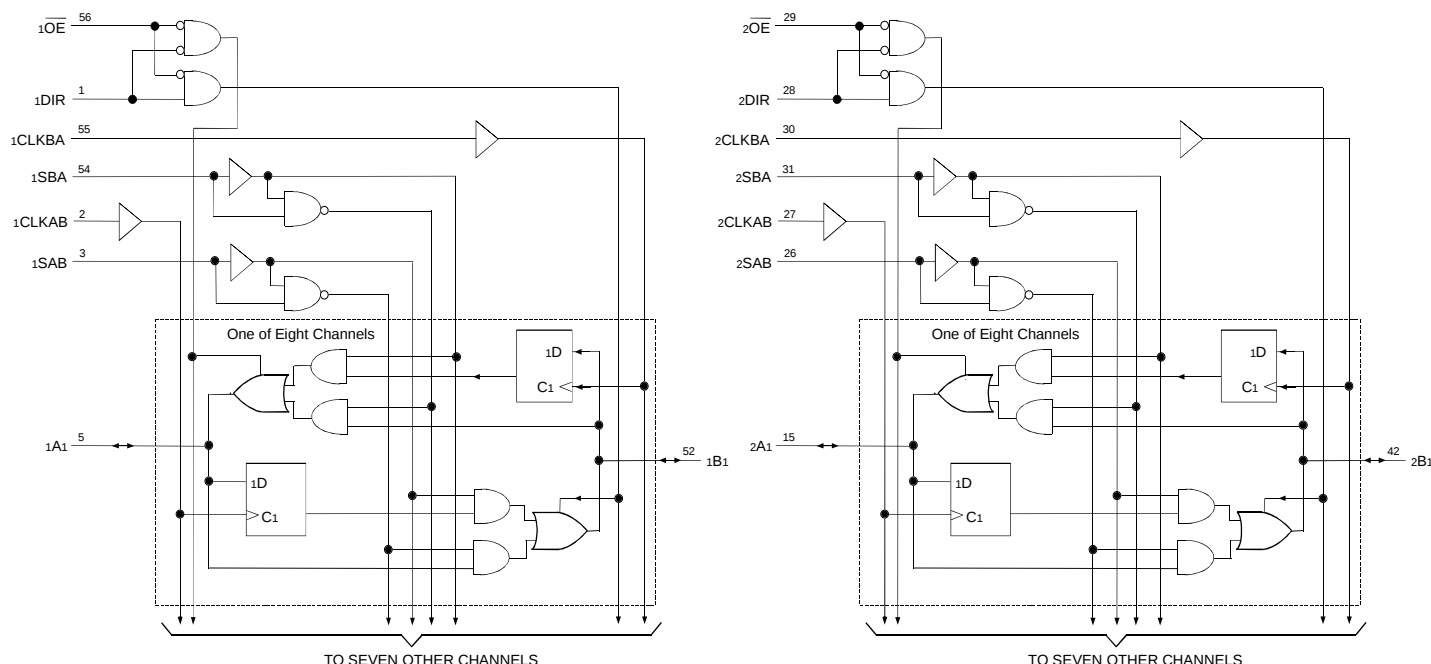
DESCRIPTION:

This 16-bit bus transceiver is built using advanced dual metal CMOS technology. The ALVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input.

Output-enable ($\overline{\text{OE}}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or both. The select control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{\text{OE}}$ is low. In the isolation mode ($\overline{\text{OE}}$ high), A data may be stored in one register and/or B data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

The ALVC16646 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

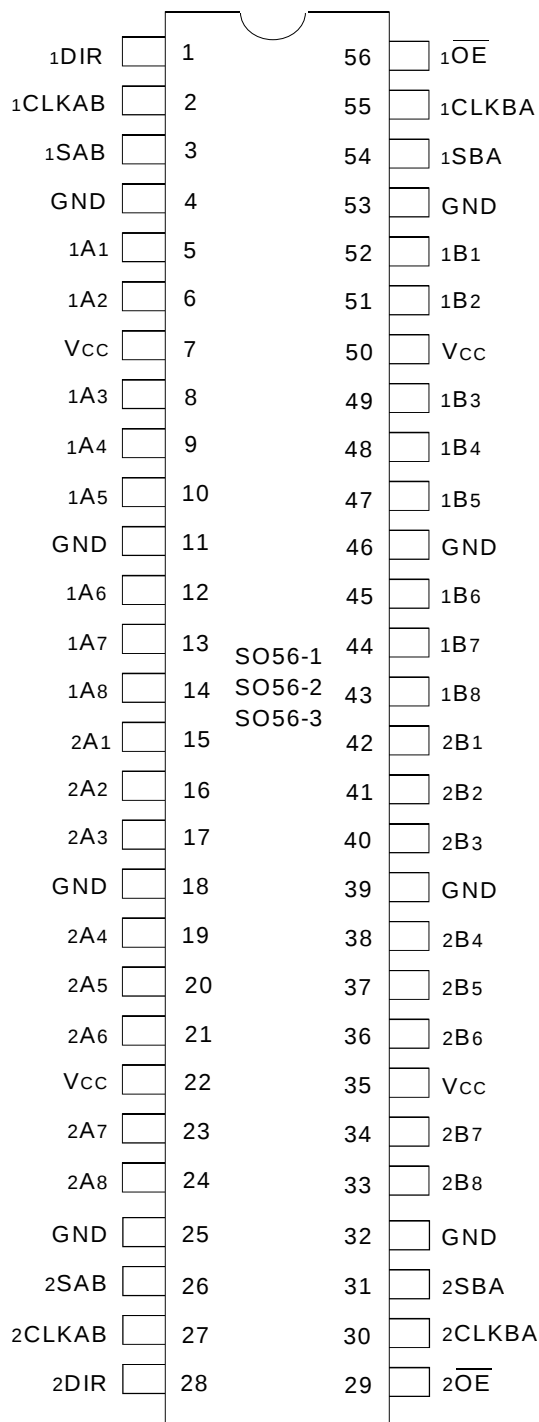
FUNCTIONAL BLOCK DIAGRAM



EXTENDED COMMERCIAL TEMPERATURE RANGE

MARCH 1999

PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to V _{CC} + 0.5	V
TSTG	Storage Temperature	– 65 to + 150	°C
IOUT	DC Output Current	– 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	– 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
x $\overline{OE}$	Output Enable Inputs
xDIR	Direction-control Inputs

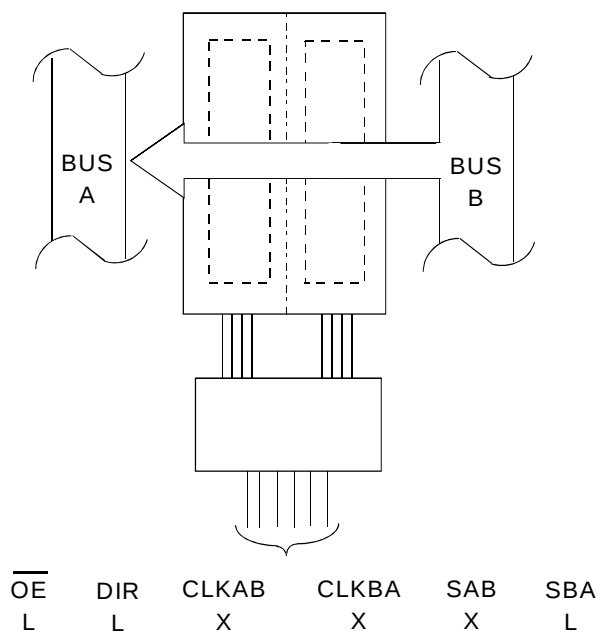
FUNCTION TABLE⁽¹⁾

Inputs						Data I/O		Operation or Function
$\overline{xOE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
X	X	↑	X	X	X	Input	Unspecified ⁽²⁾	Store A, B unspecified ⁽²⁾
X	X	X	↑	X	X	Unspecified ⁽²⁾	Input	Store B, A unspecified ⁽²⁾
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

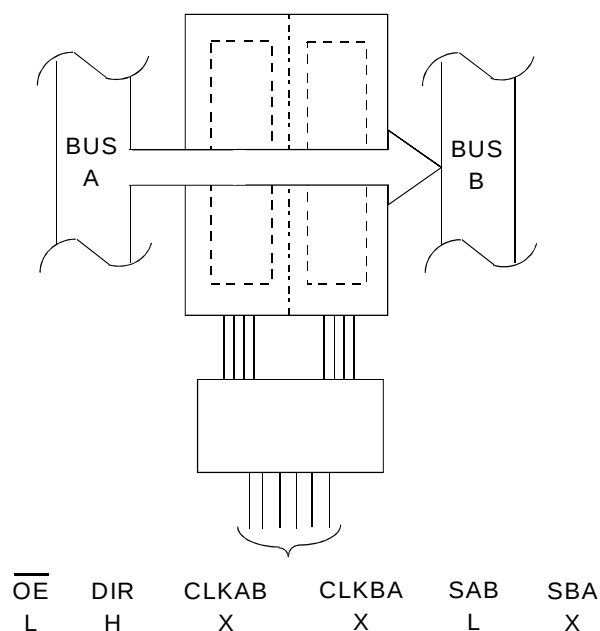
NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the $\overline{xOE}$ or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

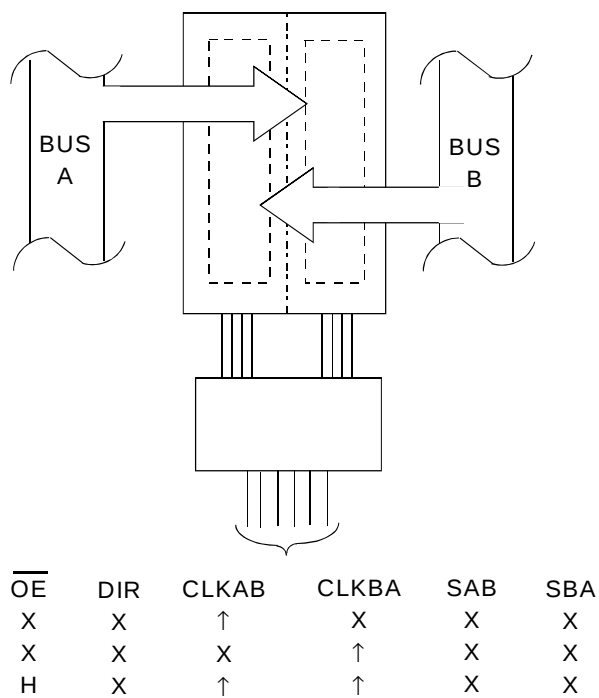
BUS MANAGEMENT FUNCTIONS



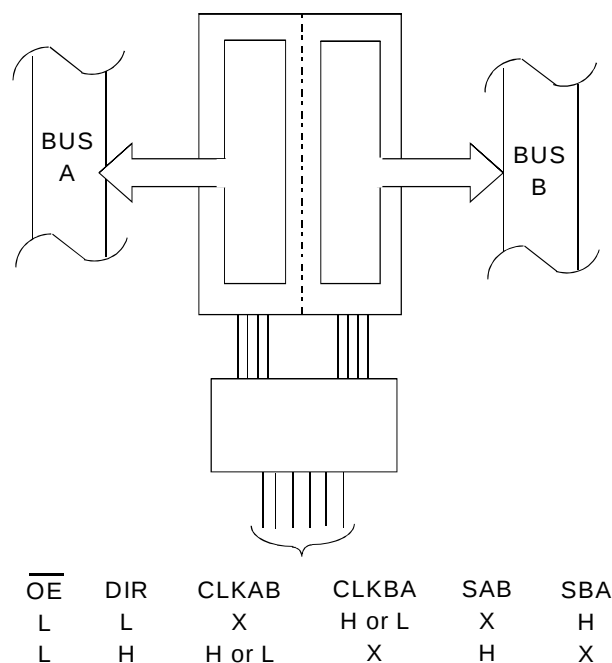
**REAL-TIME TRANSFER
BUS B TO A**



**REAL-TIME TRANSFER
BUS A TO B**



**STORAGE FROM
A AND/OR B**



**TRANSFER STORED DATA TO
A AND/OR B**

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	VCC = 3.6V	V _I = VCC	—	—	± 5	μA
I _{IL}	Input LOW Current	VCC = 3.6V	V _I = GND	—	—	± 5	
I _{OZH}	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	V _O = VCC	—	—	± 10	μA
I _{OZL}			V _O = GND	—	—	± 10	μA
V _{IK}	Clamp Diode Voltage	VCC = 2.3V, I _{IN} = – 18mA		—	– 0.7	– 1.2	V
V _H	Input Hysteresis	VCC = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	VCC = 3.6V V _{IN} = GND or VCC		—	0.1	40	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at VCC – 0.6V, other inputs at VCC or GND		—	—	750	μA

NOTE:

- Typical values are at VCC = 3.3V, +25°C ambient.

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OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	I _{OH} = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	I _{OH} = – 6mA	2	—	
		VCC = 2.3V	I _{OH} = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	I _{OH} = – 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		VCC = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		VCC = 2.7V	I _{OL} = 12mA	—	0.4	
		VCC = 3.0V	I _{OL} = 24mA	—	0.55	

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to + 85°C.

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OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	$V_{CC} = 2.5V \pm 0.2V$	$V_{CC} = 3.3V \pm 0.3V$	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	$C_L = 0\text{pF}$, $f = 10\text{MHz}$	39	43	pF
CPD	Power Dissipation Capacitance Outputs disabled		10	12	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		150	—	150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay xAx to xBx or xBx to xAx	1	4.8	—	4.5	1	3.9	ns
t_{PLH} t_{PHL}	Propagation Delay xCLKAB to xBx or xCLKBA to xAx	1	5.6	—	5.2	1	4.5	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xAx or xSAB to xBx	1	6.8	—	6.4	1	5.3	ns
t_{PZH} t_{PZL}	Output Enable Time xOE to xAx or xBx	1	6.5	—	6.2	1	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to xAx or xBx	1	7.8	—	6.2	1	5.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time xOE to xAx or xBx	1.6	5.7	—	5	1.4	4.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to xAx or xBx	1.5	6.5	—	6	1.1	5.3	ns
t_{SU}	Setup Time, xAx before xCLKAB $\uparrow$ or xBx before xCLKBA $\uparrow$	1.6	—	1.7	—	1.4	—	ns
t_H	Hold Time, xAx after xCLKAB $\uparrow$ or xBx after xCLKBA $\uparrow$	0.6	—	0.4	—	0.7	—	ns
t_W	Pulse Width, xCLKAB or xCLKBA HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
$t_{SK(0)}$	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

- See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
- Skew between any two outputs of the same package and switching in the same direction.

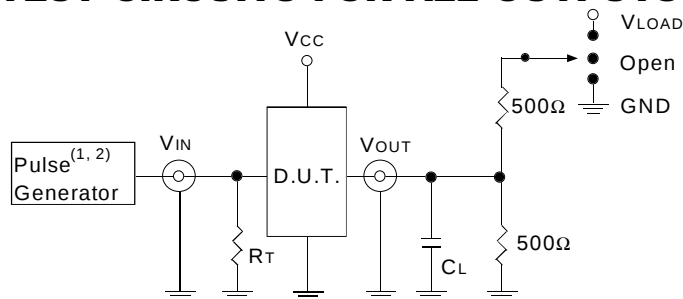
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

R_T= Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

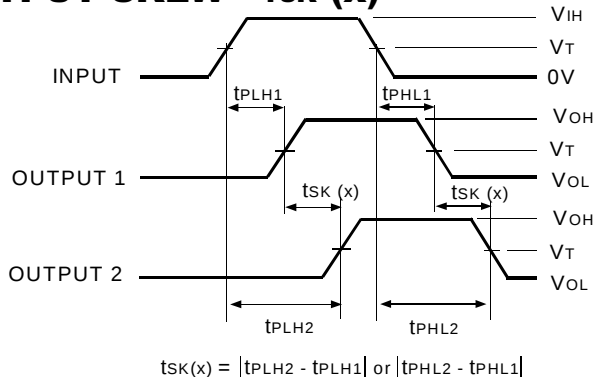
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)



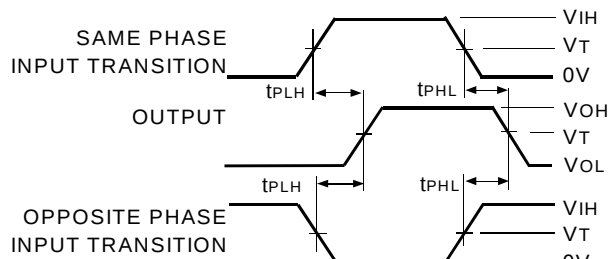
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

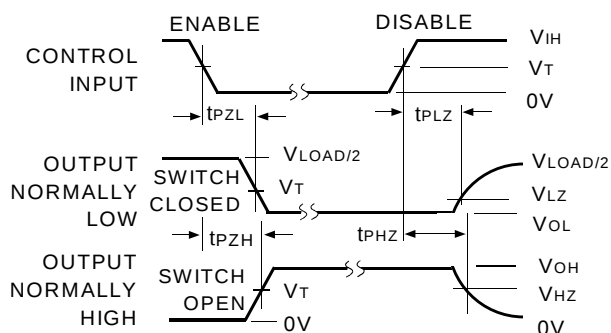
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

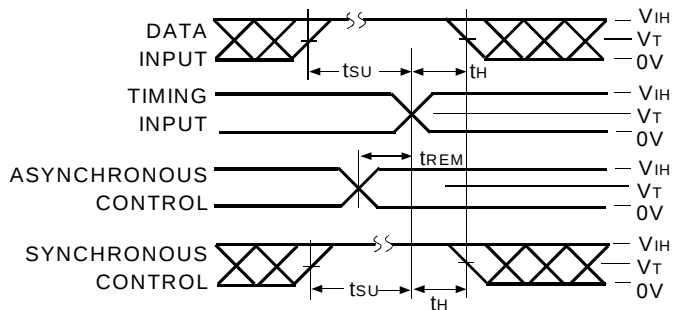


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NOTE:

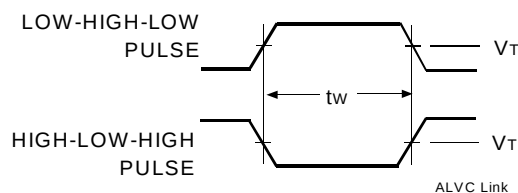
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
Temp. Range	Bus-Hold	Family	Device Type	Package			
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
				646			16-Bit Bus Transceiver and Register with 3-State Outputs
			16				Double-Density with Resistors, $\pm 24\text{mA}$
			Blank				No Bus-Hold
			74				-40°C to $+85^{\circ}\text{C}$



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