CHT-PALLAS - DATASHEET

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High-TemperatureFull-Bridge Driver

General Description

The CHT-FBDR is a High-Temperature Full-Bridge n-channel MOSFET driver comprising two independent low-side and high-side driver channels including integrated charge pumps associated to high-side channels.
The driver outputs swing from 0 to 10 V, and are able to source and sink up to 80 mA of peak current for the low side channel and 20 mA of peak current for the high-side channel. The low-side channel is referenced to ground, whereas the high-side channel is floating above ground.

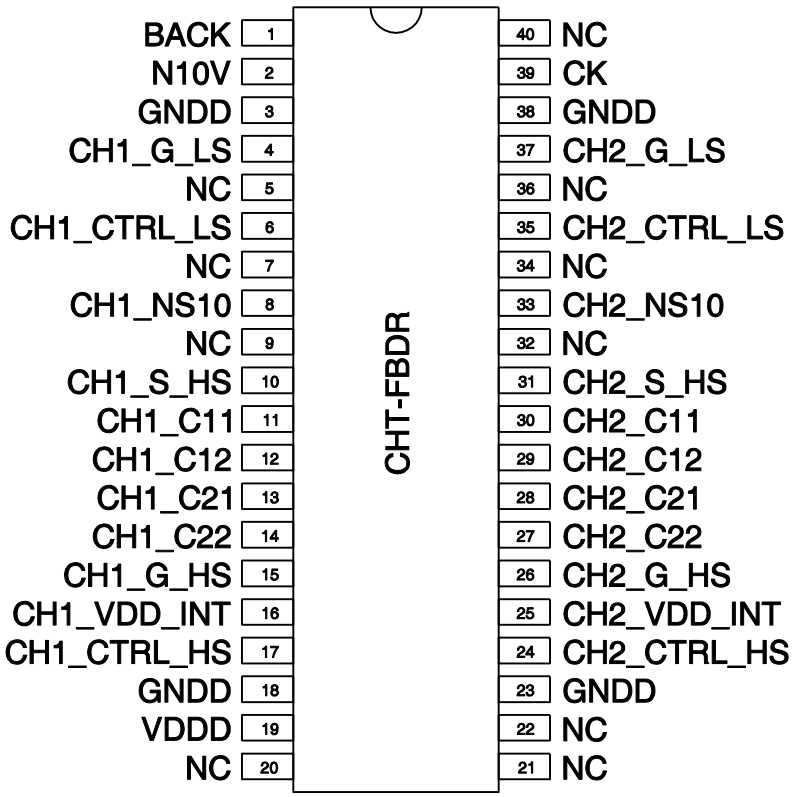
Features

- Gate high-side voltage up to 60 V
- High-side n-channel MOSFET supply voltage up to 50 V
- Gate low-side voltage up to 10 V
- 10 V analog supply
- 5 V digital supply
- Qualified from -55 to +225°C (Tj)

Applications

- Well logging
- Automotive, Aeronautics & Aerospace

Package Configuration



Functional Block Diagram and Typical Application (One Channel)

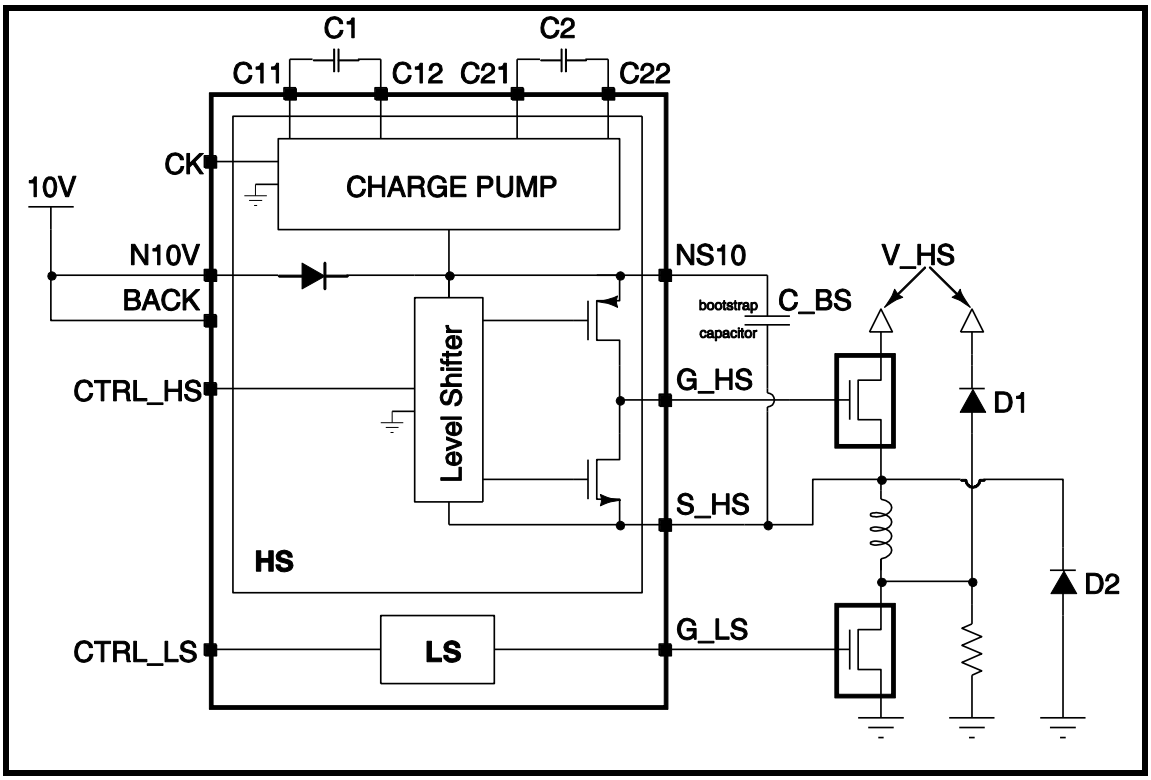


Figure 1. Functional block diagram of one channel of CHT-FBDR.

Pin Description

Pin number	Pin name	Pin description
1	BACK	Back of the die[1] (connect to 10 V to 20 V)
2	N10V	Power supply (8 to 10 V)[2]
3	GNDD	Digital ground
4	CH1_G_LS	Channel 1 low-side gate voltage up to 10 V
5	NC	Not connected
6	CH1_CTRL_LS	Channel 1 low-side digital input (0 to 5 V)
7	NC	Not connected
8	CH1_NS10	Channel 1 high-side power supply up to 60 V
9	NC	Not connected
10	CH1_S_HS	Channel 1 high-side source voltage up to 50 V floating
11	CH1_C11	Channel 1 charge pump capacitor 1 (positive terminal)[3]
12	CH1_C12	Channel 1 charge pump capacitor 1 (negative terminal)[3]
13	CH1_C21	Channel 1 charge pump capacitor 2 (positive terminal)[3]
14	CH1_C22	Channel 1 charge pump capacitor 2 (negative terminal)[3]
15	CH1_G_HS	Channel 1 high-side gate voltage up to 60 V floating
16	CH1_VDD_INT	Channel 1 optional power supply for charge pump
17	CH1_CTRL_HS	Channel 1 high-side digital input (0 to 5 V)
18	GNDD	Digital ground
19	VDDD	Digital power supply 5 V
20	NC	Not connected
21	NC	Not connected
22	NC	Not connected
23	GNDD	Digital ground
24	CH2_CTRL_HS	Channel 2 high-side digital input (0 to 5 V)
25	CH2_VDD_INT	Channel 2 optional power supply for charge pump

Pin number	Pin name	Pin description
26	CH2_G_HS	Channel 2 high-side gate voltage up to 60 V floating
27	CH2_C22	Channel 2 charge pump capacitor 2 (positive terminal)[3]
28	CH2_C21	Channel 2 charge pump capacitor 2 (negative terminal)[3]
29	CH2_C12	Channel 2 charge pump capacitor 1 (positive terminal)[3]
30	CH2_C11	Channel 2 charge pump capacitor 1 (negative terminal)[3]
31	CH2_S_HS	Channel 2 high-side source voltage up to 50 V floating
32	NC	Not connected
33	CH2_NS10	Channel 2 High-side supply up to 60 V
34	NC	Not connected
35	CH2_CTRL_LS	Channel 2 low-side digital input (0 to 5 V)
36	NC	Not connected
37	CH2_G_LS	Channel 2 low-side gate voltage up to 10 V
38	GNDD	Digital ground
39	CK	Charge pump clock (0 to 5 V)
40	NC	Not connected

[1] It **must** be connected to a clean supply voltage between 10 V and 20 V.
[2] Depending on external components (free-wheeling diodes D1 and D2 in Figure 1), the applied voltage on pin "N10V" should be adjusted to guarantee that the voltage on the high-side bootstrap capacitor C_BS (see Figure 1) does not exceed 10 V.
[3] Polarity must be respected if polarized capacitors are used.

Absolute Maximum Ratings

Digital Voltage Supply **VDDD**	6V
High-side MOSFET supply voltage **V_HS**	55V
Junction temperature T_j	300°C
ESD Rating (expected)	
Human Body Model	1kV

Operating Conditions

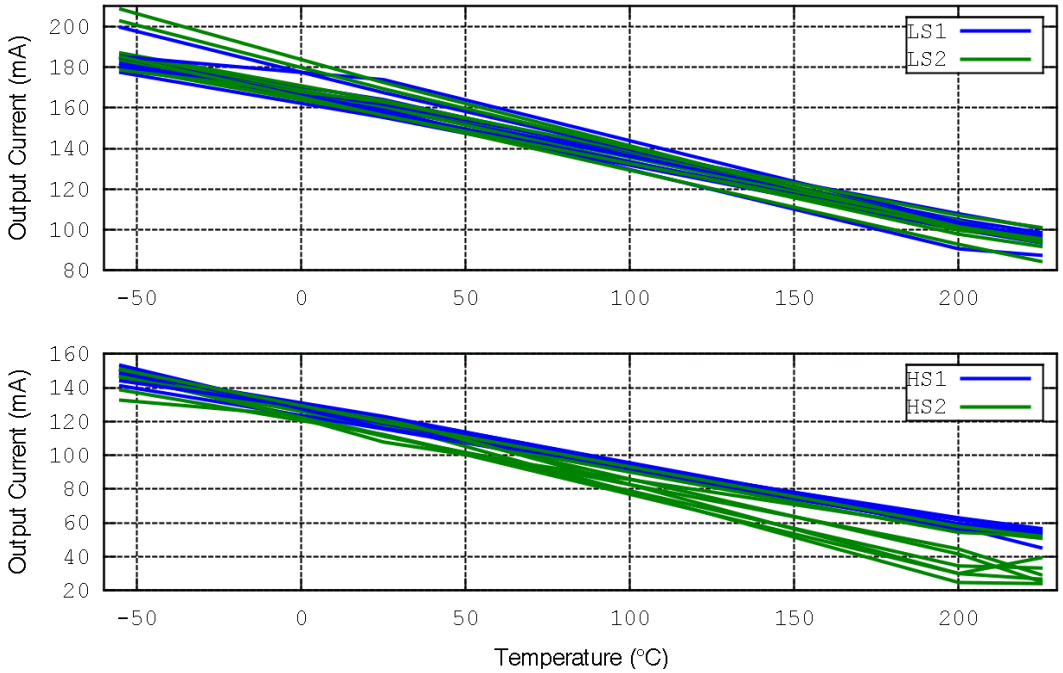
Supply Voltage **N10V**	8V to 10V
Gate High-side voltage	0V to 60V
Source High-side voltage	0V to 50V
Junction temperature	-55°C to +225°C

Electrical Characteristics

Unless otherwise stated: N10V=9V, VDDD=5V, -55°C < T j < +225°C.

Parameter	Condition	Min	Typ	Max	Units
Digital supply voltage **VDDD**		4.75		5.25	V
Analog supply voltage **N10V** (see section operating conditions)		8	9	10	V
High-side MOSFET supply voltage (**V_HS** in Figure 1)				50	V
Floating power supply voltage (pins **CH1_NS10** and **CH2_NS10**)	10V on pin **N10V**, 50V on high-side MOSFET supply voltage (**V_HS** in Figure 1)			60	V
Rising delay HS	1 nF load, 25°C			400	ns
	1 nF load, 225°C			500	
Falling delay HS	1 nF load, 25°C			150	ns
	1 nF load, 225°C			250	
Rising delay LS	1 nF load, 25°C			75	ns
	1 nF load, 225°C			100	
Falling delay LS	1 nF load, 25°C			300	ns
	1 nF load, 225°C			500	
Peak output current HS	1 nF load, 25°C	25			mA
	1 nF load, 225°C	20			
Peak output current LS	1 nF load, 25°C	120			mA
	1 nF load, 225°C	80			
Clock frequency **CK** (optional, to be connected to **GNDD** if not used)			200		kHz
Amplitude of incoming clock signal **CK** (optional, to be connected to **GNDD** if not used)		4.75		5.25	V
Digital supply **VDDD** current consumption	25 °C, **CH1_S_HS** and **CH2_S_HS** connected to **GNDD**		0.005		µA
	225 °C, **CH1_S_HS** and **CH2_S_HS** connected to **GNDD**		14.1		
Analog supply **N10V** current consumption	25 °C, **CH1_S_HS** and **CH2_S_HS** connected to **GNDD**		1.27		mA
	225 °C, **CH1_S_HS** and **CH2_S_HS** connected to **GNDD**		1.08		

Typical Performance Characteristics



Peak output current (1nF load)

Circuit Functionality

Operating conditions

The CHT-FBRD has been developed to drive n-channel MOSFETs within the 0V/10V range. Drivers are internally supplied by node “N10V” (Figure 1). If less than 10V is applied on this node, the MOSFET drive voltage will be lower than 0/10V. Drivers remain functional with “N10V” down to 8V. On the other side, this voltage cannot exceed 10V due to long term reliability reasons. Indeed, depending on external components (free-wheeling diodes), the applied voltage on pin “N10V” should be adjusted to guarantee that the voltage between G_HS and S_HS does not exceed 10V.

Bootstrap capacitor

Pins CH1_NS10 and CH2_NS10 are the internal positive supply of each high-side driver. They are internally connected to “N10V” node through a diode (Figure 1). Each high-side driver needs an external bootstrap capacitor in order to maintain its supply voltage in all conditions.
The bootstrap capacitor must be connected between:

- C_BS_CH1: “CH1_NS10” and “CH1_S_HS”: at least 470nF *(+ and – nodes respectively)*
- C_BS_CH2: “CH2_NS10” and “CH2_S_HS”: at least 470nF *(+ and – nodes respectively)*

Charge pump operation

An internal charge pump is integrated within each high-side driver. The purpose is to maintain the voltage on C_BS_CH1 and C_BS_CH2 bootstrap capacitors (Figure 1). In practice, if floating drivers are periodically turned “on” and “off”, such charge pump is not needed. However, if for any reason one high-side driver is kept in “on” state for long period of time, the bootstrap capacitor could discharge significantly. The aim of the charge pump is to maintain the voltage across these capacitors high enough to bias the high-side driver.
To activate the charge pump:

- Apply a 5V, 200kHz clock on pin **CK**.
- For each channel, connect one external capacitor of 2.2nF or more between pins “C11” and “C12” as well as another identical capacitor between pins “C21” and “C22”.
- Connect Pins 16 and 25 (CH1_VDD_INT and CH2_VDD_INT) to 5V DC supply (left floating if not used).

Secondary charge-pumping

Parasitic capacitances due to packaging and board routing connected between nodes NS10, C12 and C22 and ground are charged to V_HS each time the node S_HS is pulled down either by a low-side transistors or a resistive of inductive load.
The total equivalent parasitic capacitance, C_P, can be considered as connected in parallel to capacitors C1 and C2 of Figure 1 in order to obtain the total energy stored on this capacitance. Being C_T the total equivalent capacitance, when S_HS is pulled down to ground, the energy stored in C_T is $C_T.V\_HS^2$.
The energy spent by the driver on every cycle to drive the external transistor is $C_{ext}.V_{GS}^2$. V_{GS} is the output voltage of the HS driver in ON state, which is nearly equal to the voltage across the bootstrap capacitor C_BS. We neglect here the energy needed by the HS driver itself to operate.
If $C_T.V\_HS^2 > C_{ext}.V_{GS}^2$, the exceeding energy is transferred to the bootstrap capacitor C_BS, causing its voltage to increase every time the HS driver is switched. This voltage increase continues until the steady state is reached ($C_T.V\_HS^2=C_{ext}.V_{GS}^2$).
In practice, it has been observed that the voltage on C_BS starts increasing for V_HS higher than 15V.
To avoid having the voltage across the bootstrap capacitor above 10V, two solutions can be considered.
If the charge pump is not needed, node C22 should be connected to S_HS. Notice this must be done for each channel separately if both charge pumps are not used.
If the charge pump is used, it is recommended to use an external Zener diode, or any other controlled clamping device, with a threshold voltage of about 10V in parallel with C_BS. For applications up to 200°C, the BZT55C10 from SPC Multicomp can be used.

Packaging options

At the packaging stage, many functional features can be enabled or disabled (i.e. charge pump, two channels, high-side, low-side, …) in order to optimize the form factor according to the final user needs.
The standard package is a DIL40 including integrated charge pump, and two inde-

pendent high-side and low-side driver channels. Other packaging possibilities are available upon request.

Typical application

The CHT-FBDR can be used to drive two inductive loads using four external n-channel MOSFETs (see Figure 2). Both high-side MOSFETs are driven by high-side (floating) drivers (called “HS” within driver blocks). Both low-side MOSFETs are driven by low-side (grounded) drivers (called “LS” within driver blocks). All driver outputs can swing from 0 to 10V. All driver inputs must be driven with 0/5V logical levels (versus ground). The supply voltage of the high-side drivers can reach 60V above ground (when 50V is used for the voltage supply of the external MOSFETs).

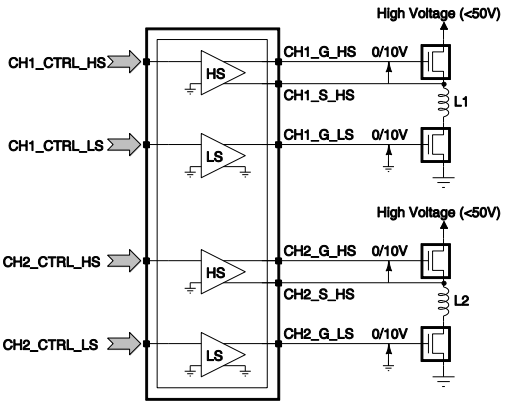
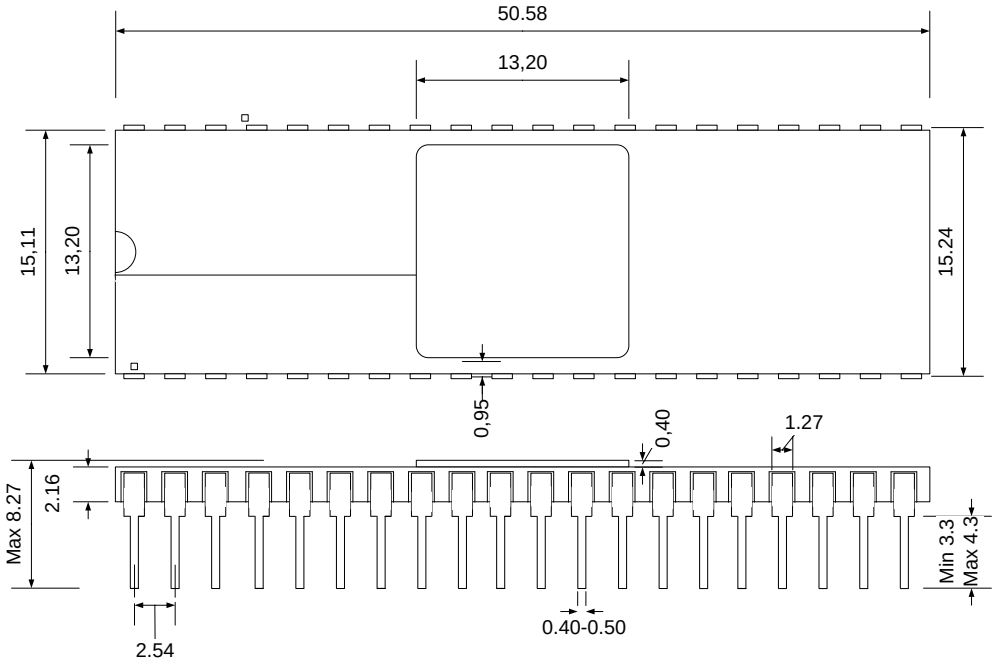


Figure 2. Overview of the overall driver system. Free-wheeling diodes associated with inductive loads and pull-up/down resistors are not represented here.

Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-PALLAS-DIL40-T	Ceramic DIL40	-55°C to +225°C	CHT-PALLAS Or CHT-FBDR (former name)

Package Dimensions



CDIL40 (mm +/- 10%)

Contact & Ordering

CISSOID S.A.

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