DATA SHEET

CX65003: 1400 – 2500 MHz Linear Power Amplifier Driver

Applications

- PCS/DCS/2.5G/3G base stations
- Wireless Local Area Networks (WLANs)
- GSM/CDMA/W-CDMA handsets
- Wireless Local Loop (WLL) and Industrial, Scientific, Medical (ISM) bands
- Repeaters
- Telematics

Features

- 5 V single supply operation
- Linear P_{OUT} of 24.5 dBm
- OIP3 of 48 dBm
- Excellent W-CDMA performance
- Internal bias circuits
- 8-pin SOIC 5.994 x 4.928 mm package with downset paddle

Description

Skyworks' CX65003 power amplifier driver offers a desirable combination of features that provide superb performance and ease of use in a low-cost Surface-Mounted Technology (SMT) package. This Gallium Arsenide (GaAs) Heterojunction Bipolar Transistor (HBT) power amplifier driver was developed and optimized for extreme linear performance in a variety of applications. It is ideal as a driver or output stage in transceivers and repeaters for Wideband Code Division Multiple Access (W-CDMA) and CDMA2000 applications.

The 8-pin Small Outline Integrated Circuit (SOIC) device package and pinout are shown in Figure 1. Figure 2 shows a functional block diagram for the CX65003. Signal pin assignments and functional pin descriptions are provided in Table 1.

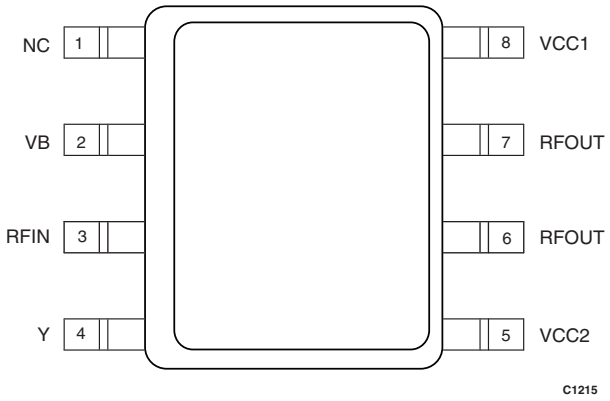

Figure 1. CX65003 Pinout – 8-Pin SOIC Package (Top View)

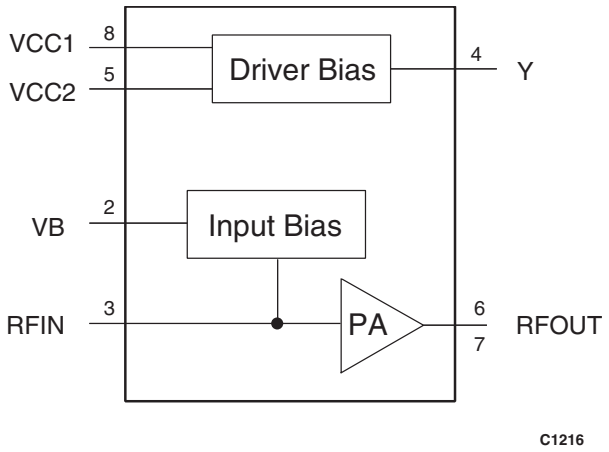

Figure 2. CX65003 Functional Block Diagram

Table 1. CX65003 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	NC	No connection	5	VCC2	Supply voltage
2	VB	Input bias for amplifier driver	6	RFOUT	RF output
3	RFIN	RF input	7	RFOUT	RF output
4	Y	Output of internal bias circuit	8	VCC1	Supply voltage

Evaluation Board Description

The CX65003 Evaluation Board is used to test the performance of the CX65003 power amplifier driver. An Evaluation Board schematic diagram, optimized for the 3rd Order Output Intercept Point (OIP3), is shown in Figure 19. A schematic diagram optimized for Adjacent Channel Power Rejection (ACPR) is provided in Figure 20. The Evaluation Board assembly diagram is shown in Figure 21 and the Evaluation Board layer detail is shown in Figure 22. The mounting footprint for the CX65003 is shown in Figure 23.

Circuit Design Configurations

The following design considerations are general in nature and must be followed regardless of final use or configuration.

1. Paths to ground should be made as short as possible.
2. The ground pad of the CX65003 power amplifier has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the amplifier. As such, design the connection to the ground pad to dissipate the maximum wattage produced to the circuit board. Multiple vias to the grounding layer are required.

***NOTE**: Junction temperature (T_J) of the device increases with a poor connection to the slug and ground. This reduces the lifetime of the device.*

3. External bypass capacitors are required on the VCC line and on pins 4, 5, and 8.
4. Bias resistor R1 is used to control the reference voltage of the bias circuit (VCC1) at pin 8.
5. Inductor L1 is placed between the bias circuit output (pin 4) and the base of RF transistor (pin 2) for bias circuit and RF transistor connection.

Suggested matching circuits are shown in Figures 19 and 20.

Testing Procedure

Use the following procedure to set up the CX65003 Evaluation Board for testing. Refer to Figure 24 for guidance:

1. Connect a 5.0 V supply to VCC. If available, enable the current limiting function of the power supply to 240 mA.
2. Connect a signal generator to the RF signal input port. Set it to the desired RF frequency at a power level of –15 dBm or less to the Evaluation Board but do NOT enable the RF signal.
3. Connect a spectrum analyzer to the RF signal output port.
4. Enable the power supply.
5. Enable the RF signal
6. Take measurements.

***CAUTION:** If any of the input signals exceed the rated maximum values, the CX65003 Evaluation Board can be permanently damaged.*

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second. Maximum temperature should not exceed 225 °C and the time spent at a temperature that exceeds 210 °C should be limited to less than 10 seconds. If the part is manually attached, precaution should be taken to ensure that the part is not subjected to a temperature that exceeds 300 °C for more than 10 seconds.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks' Application Note, *Tape and Reel*, document number 101568.

Electrical and Mechanical Specifications

The absolute maximum ratings of the CX65003 are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

Typical performance characteristics of the CX65003 are shown in Figures 3 through 18. Typical application circuits are shown in Figure 19, optimized for OIP3, and in Figure 20, optimized for

ACPR. Evaluation Board mechanical details are shown in Figures 21 and 22, and mounting footprint measurements are provided in Figure 23. The testing configuration for the CX65003 Evaluation Board is shown in Figure 24.

Figure 25 provides the package dimensions for the 8-pin SOIC and Figure 26 provides the tape and reel dimensions.

Electrostatic Discharge (ESD) Sensitivity

The CX65003 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper ESD precautions.

Table 2. CX65003 Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Units
RF input power	P_{IN}			15	dBm
Supply voltage (VCC1 and VCC2 pins)	VCC			5.5	V
Supply current (I_D + I_{BIAS})	I_{CC}			240	mA
Power dissipation				1.3	W
Case operating temperature	T_C	–40		+85	°C
Storage temperature	T_{ST}	–55		+125	°C
Junction temperature	T_J			+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value.

Table 3. CX65003 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Supply voltage (VCC1 and VCC2 pins)	VCC		5		V
Operating frequency	F_O	1400		2500	MHz
Junction temperature	T_J			140	°C
Maximum bias condition	$(VCC \times I_D) < (T_{J\_RECOMMENDED} - T_C)/R_{TH,J\text{-}C}$				

Table 4. CX65003 Electrical Characteristics
(VCC = 5 V, T_C = 25 °C)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Units
OIP3 Match, Frequency = 1960 MHz (Note 1)						
Quiescent current (I_D + I_{BIAS})	Iq	R_{BIAS} = 270 Ω		120	130	mA
Small signal gain	G	P_{IN} = –15 dBm	10	11.5		dB
Linear output power (Note 2)	P_{OUT}	P_{IN} = +13 dBm	23	24.5		dBm
Power Added Efficiency	PAE	P_{IN} = +13 dBm	30	38		%
Noise Figure (NF)	NF			5	6	dB
Output IP3	OIP3	Two CW tones with 1 MHz spacing, P_{IN} = –4 dBm per tone	42	48		dBm
Thermal resistance (junction – case)	$R_{TH,J-C}$			65		°C/W
ACPR Match, Frequency = 2140 MHz (Note 3)						
Quiescent current (I_D + I_{BIAS})	Iq	R_{BIAS} = 330 Ω		90	105	mA
Small signal gain (Note 4)	G	P_{IN} = –15 dBm	9.5	11		dB
Peak envelope power (Note 2)	P_{PEP}	3G-WCDMA downlink test model #1 signal or IS95 downlink 9 ch Fwd signal, P_{IN} = 9 dBm		29		dBm
Average output power (F = 1.96 GHz) @ ACPR = –45 dBc (Note 3), 885 kHz offset	P_{OUT}ACPR	IS95 downlink CDMA signal, 9 ch Fwd, P_{IN} = 11 dBm	20	21		dBm
Average output power (F = 2.14 GHz) @ ACLR = –45 dBc, 5 MHz offset	P_{OUT}ACLR	3G-WCDMA downlink test model #1 signal with 64 DPCH, P_{IN} = 9 dBm	18.5	20		dBm

Note 1: Device matched for optimum OIP3 according to circuit shown in Figure 19.

Note 2: For reliable operation, do not violate the maximum input drive level specified in Table 2.

Note 3: Device matched for optimum ACPR according to circuit shown in Figure 20.

Note 4: For optimum output small signal gain and Noise Figure, use the matching circuit shown in Figure 19 and the characterization values for 1960 MHz operation.

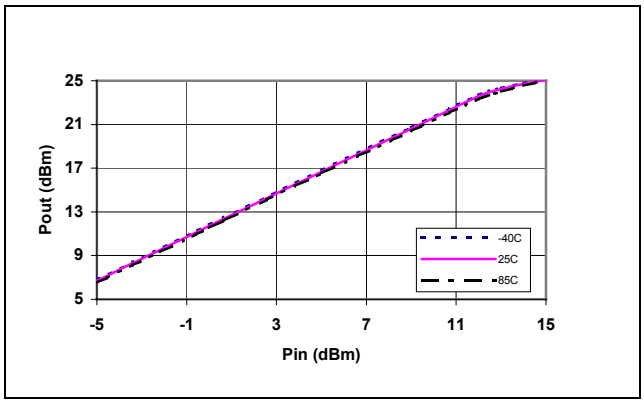

Figure 3. Typical P_{OUT} vs P_{IN} @ 1960 MHz Over Temperature (Circuit Match for Optimum OIP3)

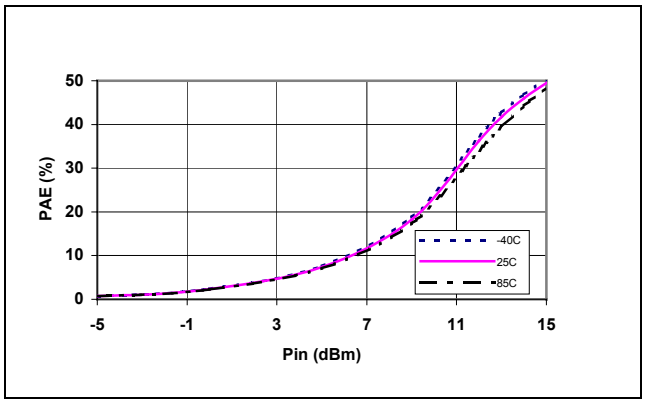

Figure 4. Typical PAE vs P_{IN} @ 1960 MHz Over Temperature (Circuit Match for Optimum OIP3)

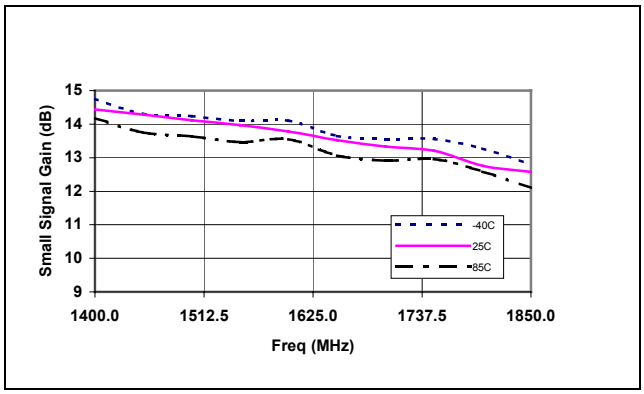

Figure 5. Typical Small Signal Gain From 1.4 to 1.85 GHz Over Temperature (Circuit Match for Optimum Gain)

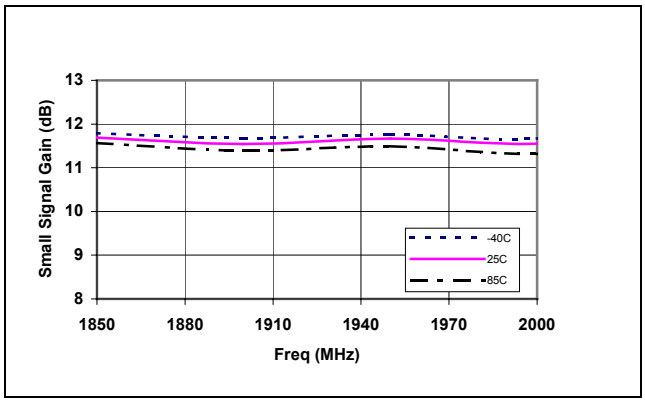

Figure 6. Typical Small Signal Gain From 1.85 to 2.0 GHz Over Temperature (Circuit Match for Optimum OIP3)

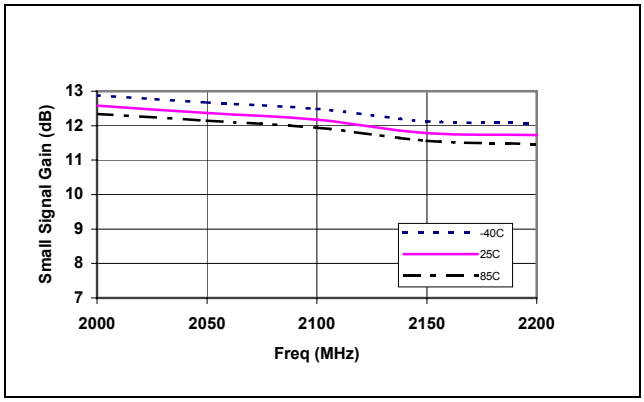

Figure 7. Typical Small Signal Gain From 2 to 2.2 GHz Over Temperature (Circuit Match for Optimum OIP3)

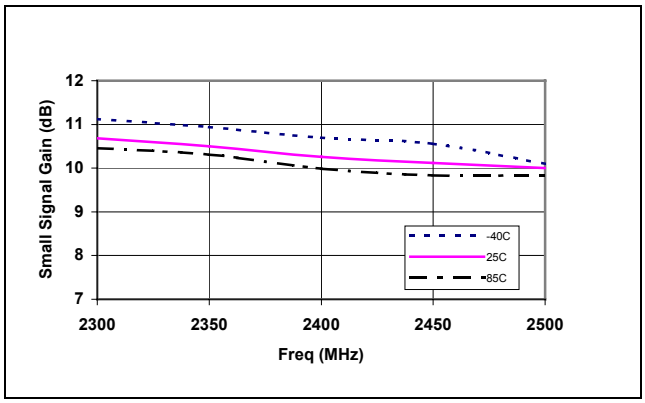

Figure 8. Typical Small Signal Gain From 2.3 to 2.5 GHz Over Temperature (Circuit Match for Optimum OIP3)

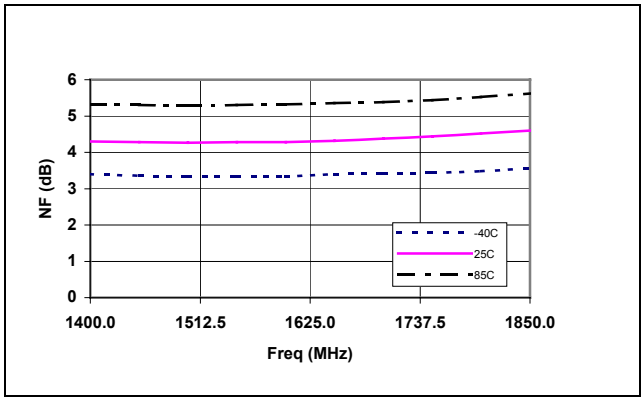

Figure 9. Typical Noise Figure From 1.4 to 1.85 GHz Over Temperature (Circuit Match for Optimum Gain)

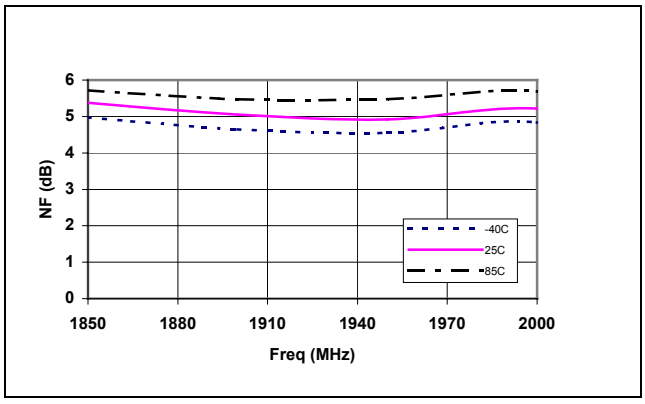

Figure 10. Typical Noise Figure From 1.85 to 2.0 GHz Over Temperature (Circuit Match for Optimum OIP3)

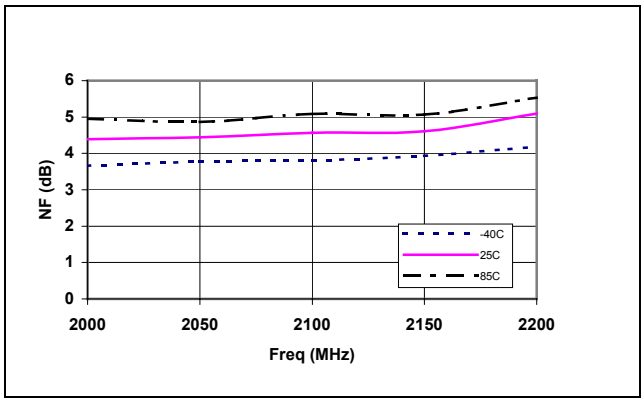

Figure 11. Typical Noise Figure From 2.0 to 2.2 GHz Over Temperature (Circuit Match for Optimum OIP3)

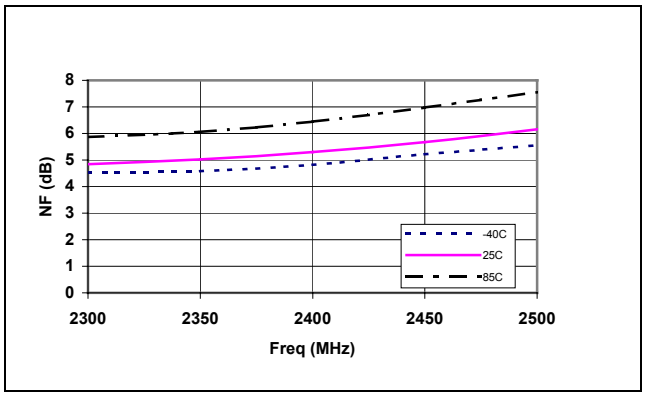

Figure 12. Typical Noise Figure From 2.3 to 2.5 GHz Over Temperature (Circuit Match for Optimum OIP3)

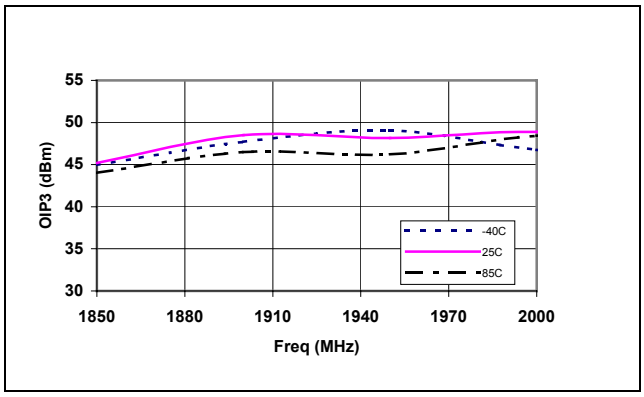

Figure 13. Typical OIP3 From 1.85 to 2.0 GHz Over Temperature (Circuit Match for Optimum OIP3)

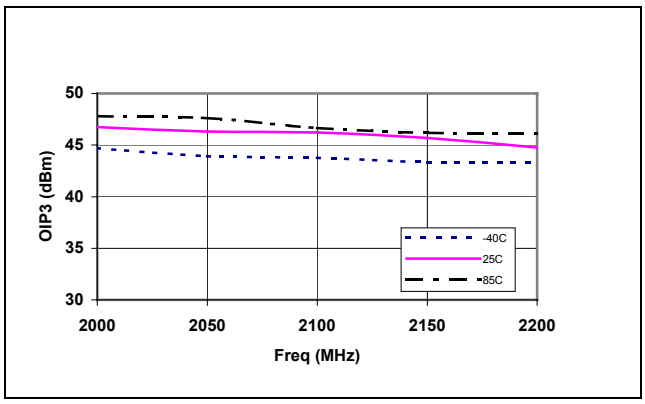

Figure 14. Typical OIP3 From 2.0 to 2.2 GHz Over Temperature (Circuit Match for Optimum OIP3)

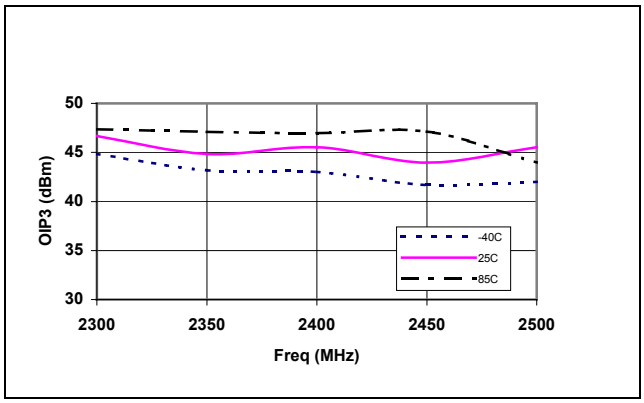

Figure 15. Typical OIP3 From 2.3 to 2.5 GHz Over Temperature (Circuit Match for Optimum OIP3)

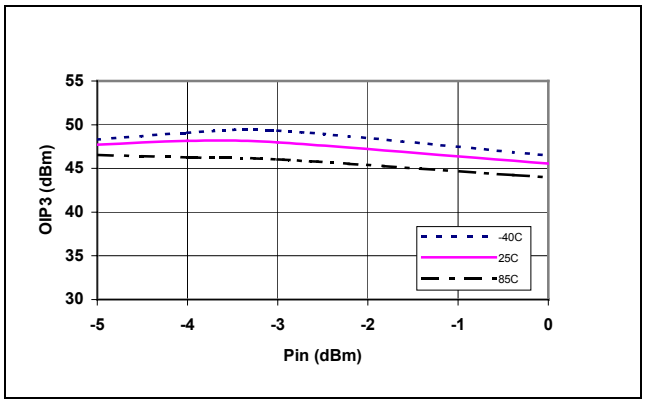

Figure 16. Typical OIP3 vs P_{IN} @ 1960 MHz Over Temperature (Circuit Match for Optimum OIP3)

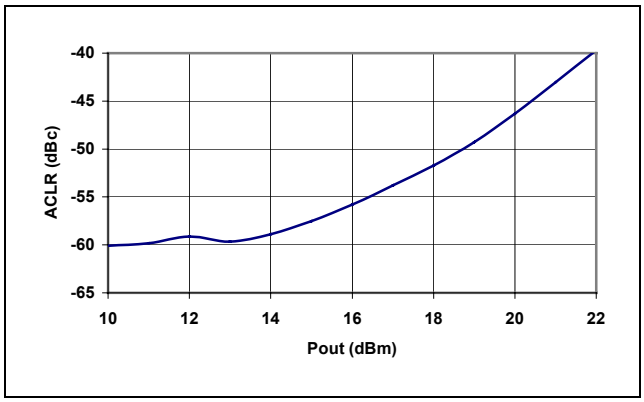

Figure 17. Typical ACLR vs P_{OUT} @ 2.14 GHz, 5 MHz Offset, 25 °C (Circuit Match for Optimum ACPR)

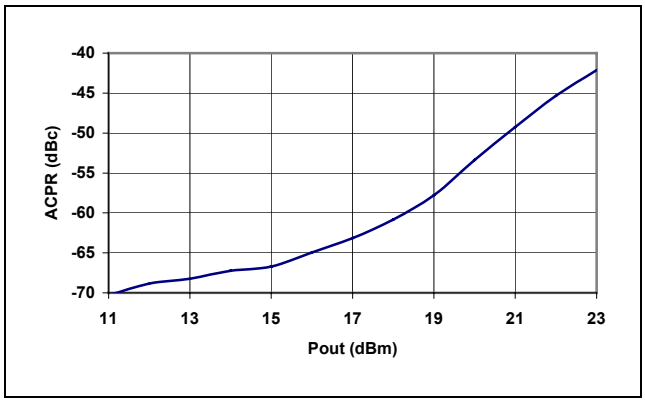

Figure 18. Typical ACPR vs P_{OUT} @ 1.96 GHz, 885 kHz Offset, 25 °C (Circuit Match for Optimum ACPR)

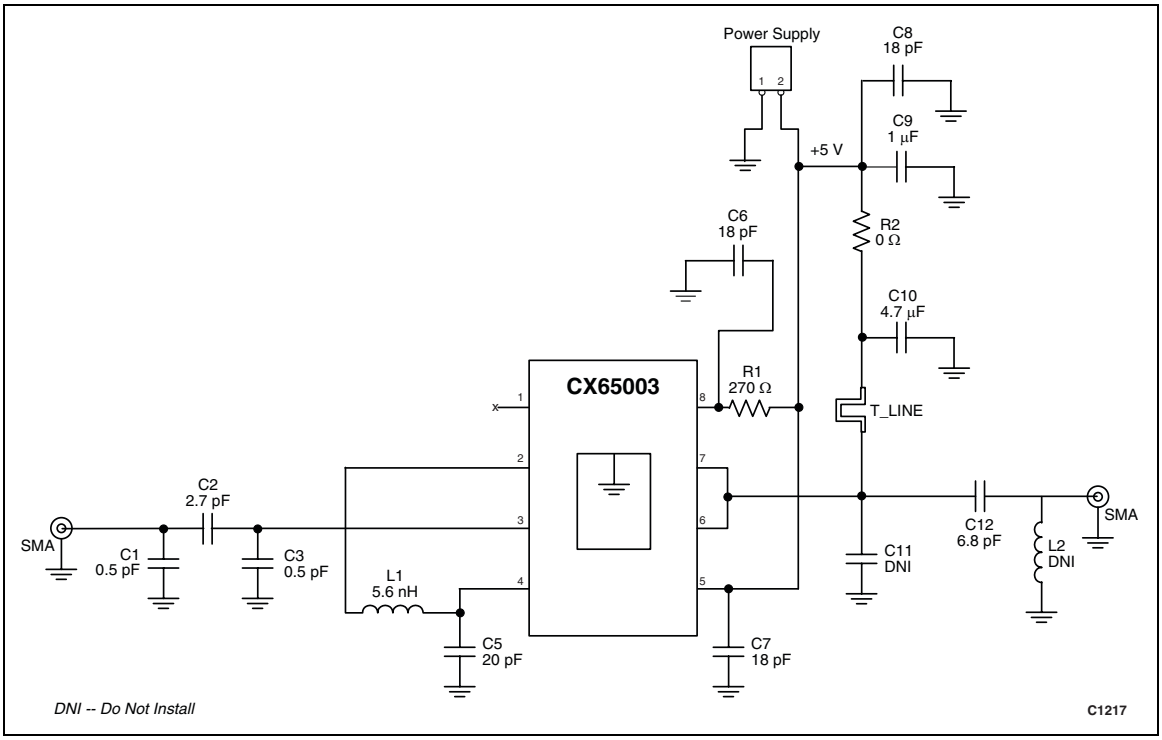

Figure 19. Application Schematic Optimized for OIP3 @ 1960 MHz

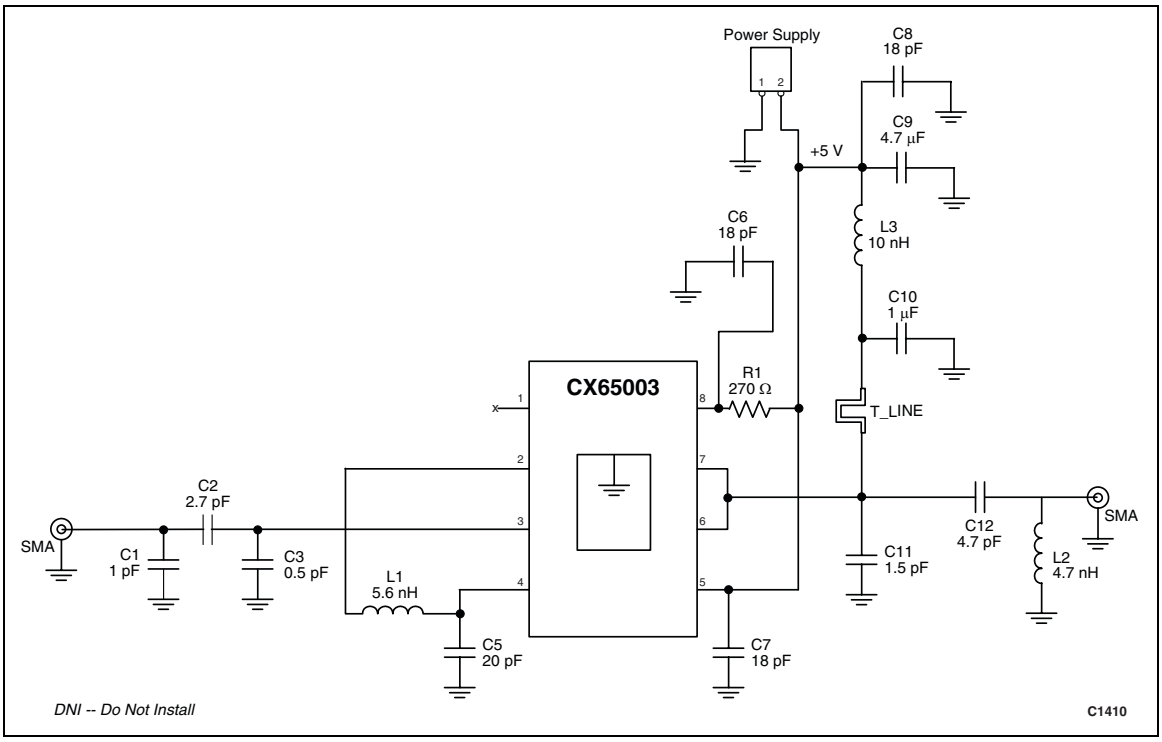

Figure 20. Application Schematic Optimized for ACPR @ 2140 MHz

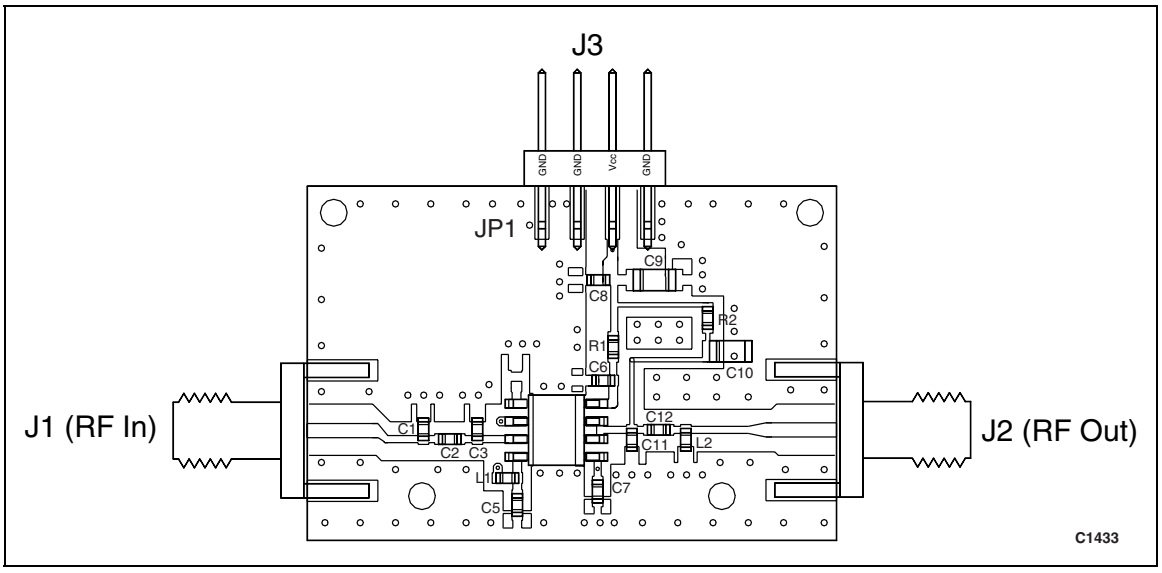

Figure 21. Evaluation Board Assembly Diagram

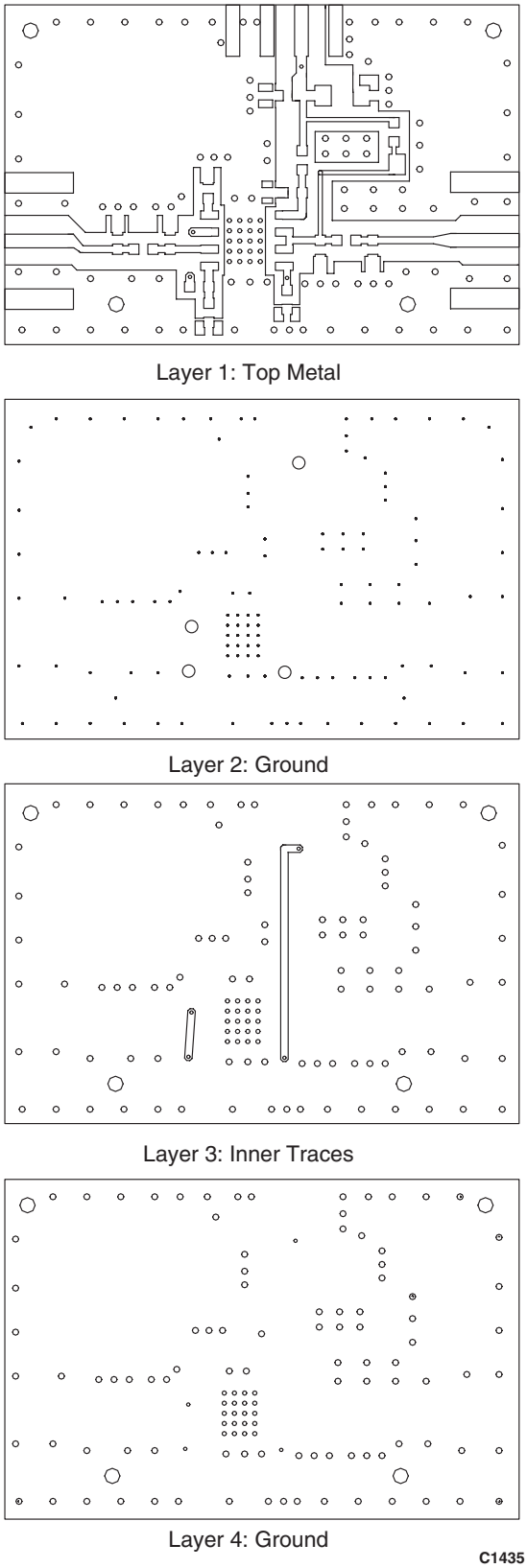

Figure 22. Evaluation Board Layer Detail

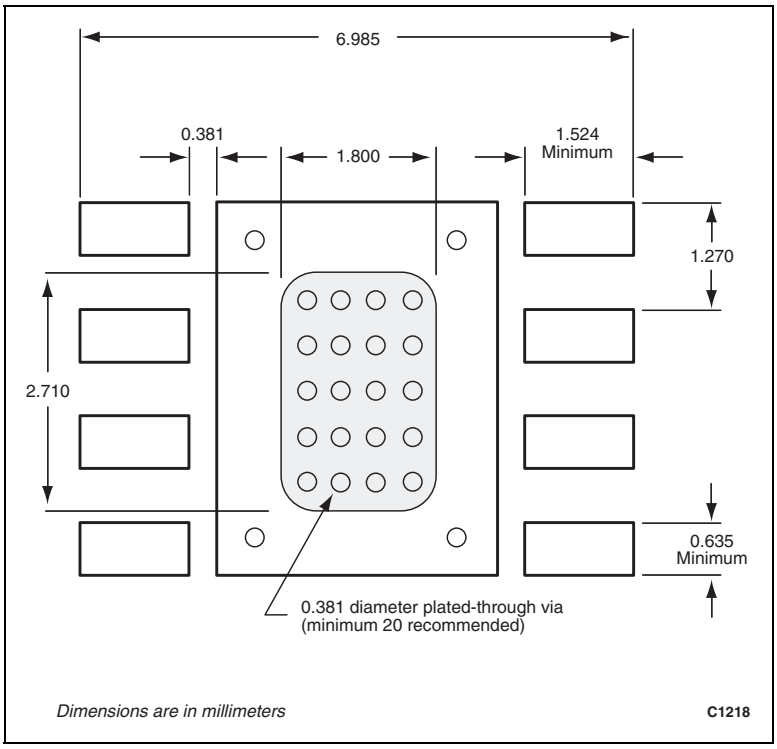

Figure 23. PCB Mounting Footprint

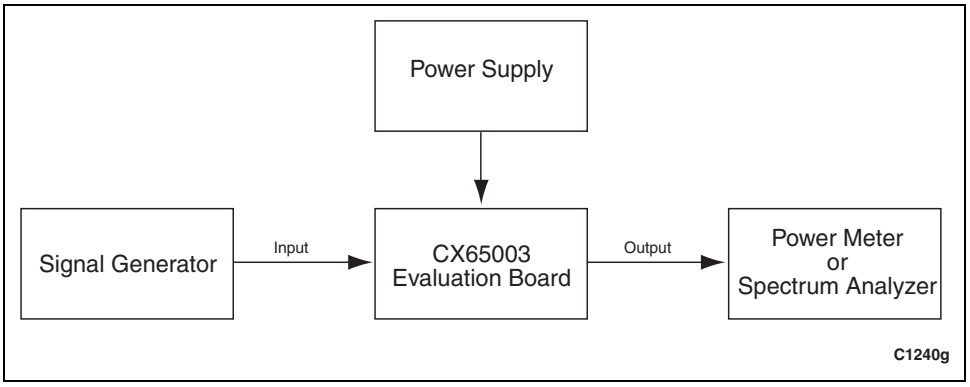

Figure 24. CX65003 Evaluation Board Testing Configuration

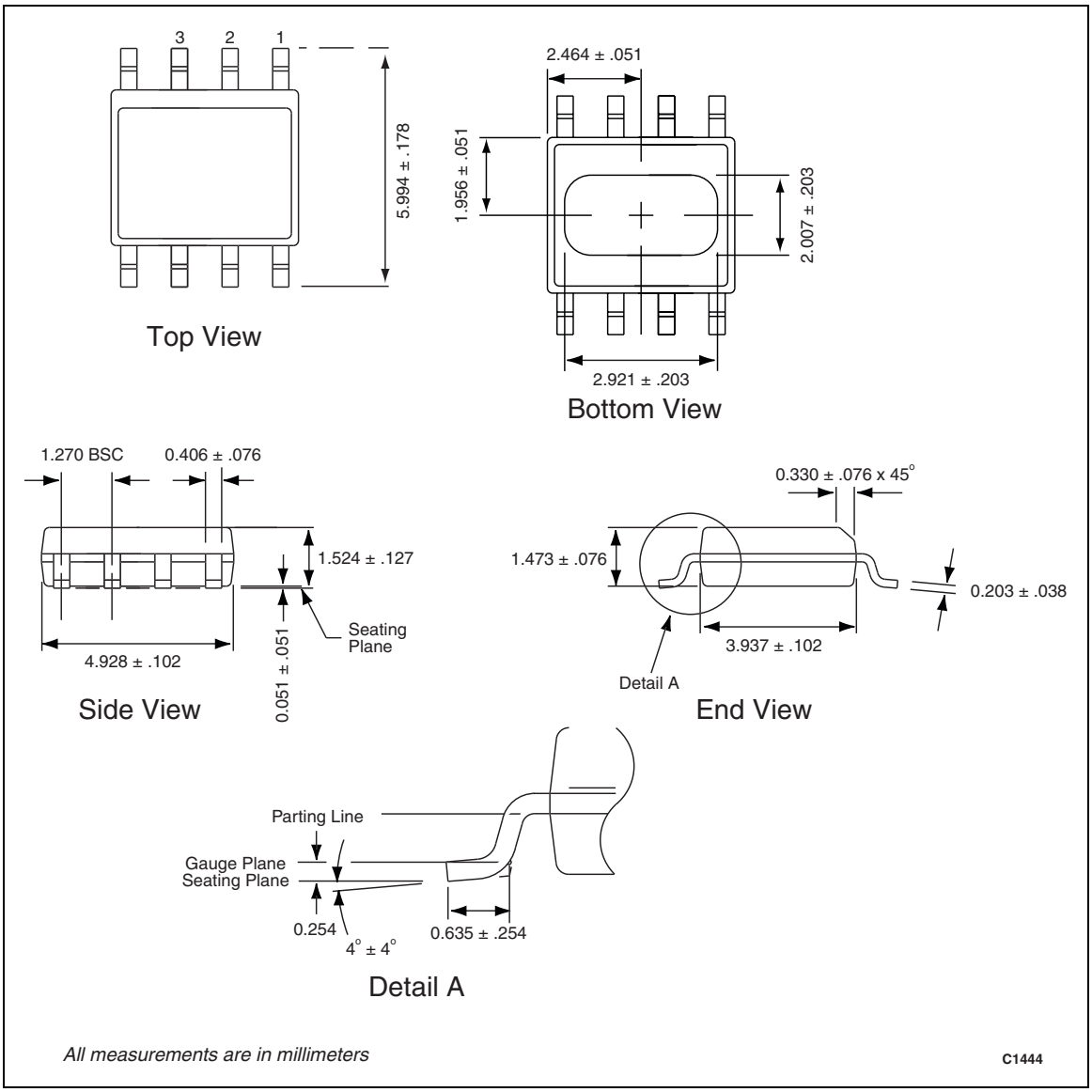

Figure 25. CX65003 8-Pin SOIC Package Dimensions

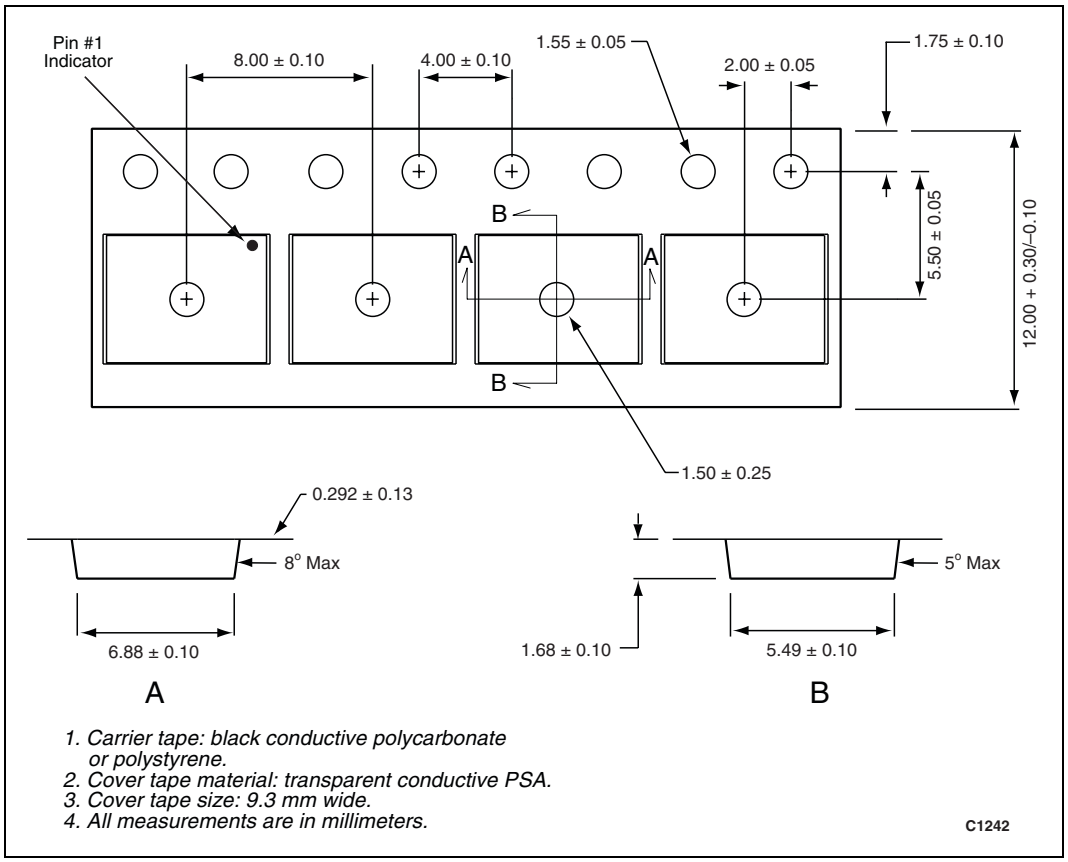

Figure 26. CX65003 8-Pin SOIC Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Kit Part Number
CX65003 1400-2500 MHz Linear Power Amplifier Driver	CX65003-12	TW10-D292 (tuned for optimum OIP3 @ 1.96 GHz) TW10-D293 (tuned for optimum ACPR @ 2.14 GHz and 1.96 GHz)