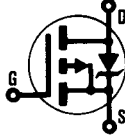


INTERNATIONAL RECTIFIER



HEXFET® TRANSISTORS

4P CHANNEL
POWER MOSFETs14 LEAD DUAL-IN-LINE QUAD
(CERAMIC SIDE BRAZED PACKAGE)

IRFG9110

2N7335

JANTX2N7335

JANTXV2N7335

[REF: MIL-S-19500/599]

-100 Volt, 1.4 Ohm (P-Channel)

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The P-Channel HEXFETs are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification; for this IRFG110 is the perfect answer. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers. These packages are well suited for both military and commercial applications.

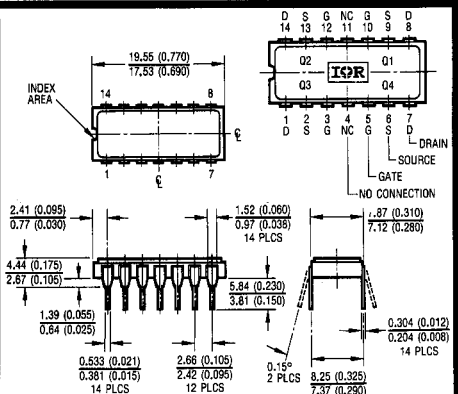
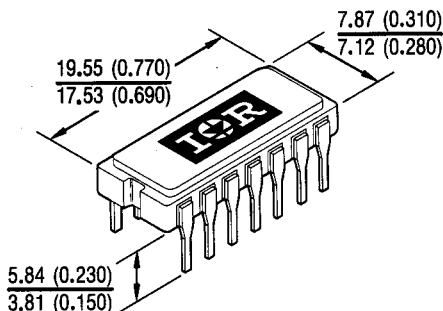
Product Summary

Part Number	VDSS	RDS(on)	ID
IRFG9110	-100V	1.4Ω	-0.75A

Features:

- Avalanche Energy Rating
- Dynamic dv/dt Rating
- Hermetically Sealed
- For Automatic Insertion
- Lightweight
- Simple Drive Requirements
- Ease of Paralleling
- 4 P-Channel Co-Packaged HEXFETs

CASE STYLE AND DIMENSIONS



Conforms to JEDEC MO-036AB
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings For Each Chip ①

Parameter		Units
I_D @ $V_{GS} = -10V$, $T_C = 25^\circ C$	Continuous Drain Current	-0.75 A
I_D @ $V_{GS} = -10V$, $T_C = 100^\circ C$	Continuous Drain Current	-0.50 A
I_{DM}	Pulsed Drain Current	-30 A
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	1.4 W
	Linear Derating Value	0.011 W/K ⑤
V_{GS}	Gate-to-Source Voltage	± 20 V
E_{AS}	Single Pulse Avalanche Energy ②	75 mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5 V/ns
T_J	Operating Junction	-55 to 150
T_{STG}	Storage Temperature Range	
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)
	Weight	1.3 (typical) g

Electrical Characteristics For Each Chip @ $T_J = 25^\circ C$ (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	-100	—	—	V	$V_{GS} = 0V$, $I_D = -1.0$ mA
$\Delta BV_{DSS}/\Delta T_J$	—	0.098	—	V/ $^\circ C$	Reference to $25^\circ C$, $I_D = -1.0$ mA
$R_{DS(on)}$	—	—	1.4	Ω	$V_{GS} = -10V$, $I_D = -0.50A$
	—	—	1.73		$V_{GS} = -10V$, $I_D = -0.75A$ ④
$V_{GS(th)}$	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -250$ μA
g_{fs}	0.67	—	—	S (S)	$V_{DS} \geq -15V$, $I_{DS} = -0.50A$ ④
I_{DSS}	—	—	-25	μA	$V_{DS} = 0.8 \times \text{Max. Rating}$, $V_{GS} = 0V$
	—	—	-250		$V_{DS} = 0.8 \times \text{Max. Rating}$, $V_{GS} = 0V$, $T_J = 125^\circ C$
I_{GSS}	—	—	-100	nA	$V_{GS} = -20V$
I_{GSS}	—	—	100		$V_{GS} = 20V$
Q_g	—	—	15	nC	$V_{GS} = -10V$, $I_D = -0.75A$
Q_{gs}	—	—	7.0		$V_{DS} = 0.5 \times \text{Max. Rating}$
Q_{gd}	—	—	8.0		See Fig. 6 and 14
$t_{d(on)}$	—	—	30	ns	$V_{DD} = -50V$, $I_D = -0.75A$, $R_G = 24\Omega$
t_r	—	—	60		
$t_{d(off)}$	—	—	40		See Fig. 11
t_f	—	—	40		
L_D	—	4.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	—	6.0	—		Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	—	200	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$
C_{oss}	—	85	—		$f = 1.0$ MHz
C_{res}	—	30	—		See Fig. 5



Source-Drain Diode Ratings and Characteristics for Each P-Channel Chip

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	—	—	-0.75	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM} Pulse Source Current (Body Diode) ①	—	—	-3.0		
V_{SD} Diode Forward Voltage	—	—	-5.5	V	$T_J = 25^\circ\text{C}$, $I_S = -0.75\text{A}$, $V_{GS} = 0\text{V}$ ④
t_{rr} Reverse Recovery Time	—	—	200	ns	$T_J = 25^\circ\text{C}$, $I_F = -0.75\text{A}$, $di/dt \leq -100\text{ A}/\mu\text{s}$
Q_{RR} Reverse Recovery Charge	—	—	9.0	μC	$V_{DD} \leq -50\text{V}$
t_{on} Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 9)
Refer to current HEXFET reliability report

③ $I_{SD} \leq -0.75\text{A}$, $di/dt \leq -75\text{ A}/\mu\text{s}$
 $V_{DD} \leq BV_{DSS}$, $T_J \leq 150^\circ\text{C}$
Suggested $R_G = 24\Omega$

⑤ $K/W = ^\circ\text{C}/\text{W}$
 $W/K = \text{W}/^\circ\text{C}$

② @ $V_{DD} = -25\text{V}$. Starting $T_J = 25^\circ\text{C}$
 $L \geq 200\text{ mH}$. $R_G = 250$
Peak $I_L = -0.75\text{A}$

④ Pulse width $\leq 300\text{ }\mu\text{s}$; Duty Cycle $\leq 2\%$

Power Ratings

Power Rating Test	Single FET Channel	All Four FETs With Equal Power	Units
P_D @ $T_A = 25^\circ\text{C}$ Maximum Power Dissipation	1.4	2.5	W
L_{DF} Linear Derating Factor	0.011	0.020	W/K
R_{thJC} Thermal Resistance Junction-to-Case	17	—	K/W
R_{thJA} Thermal Resistance Junction-to-Ambient	90	50	K/W
K_1, K_4, T_{CF} Thermal Coupling Factors	—	40	%

To a first order approximation the temperature rise of each device within the package is the result of the power dissipated by the device itself and the power dissipated by the other adjacent devices. The power dissipated by the adjacent devices does not have the same effect as the power dissipated within the junction itself. The temperature rise for any particular unit (e.g. (1)) within the package can be calculated with the following expression:

$$(1) \Delta T_1 = 90 (P_1 + K_{12} P_2 + K_{13} P_3 + K_{14} P_4)$$

where the K_{ij} are the thermal coupling coefficients shown in the Power Ratings Table.

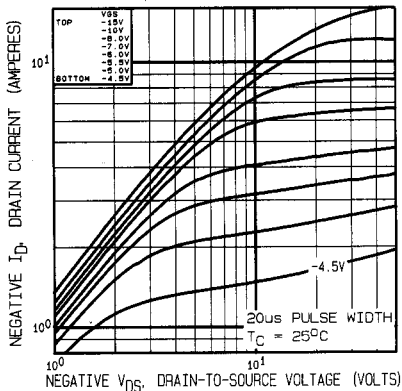
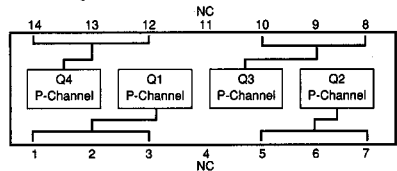


Fig. 1—Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

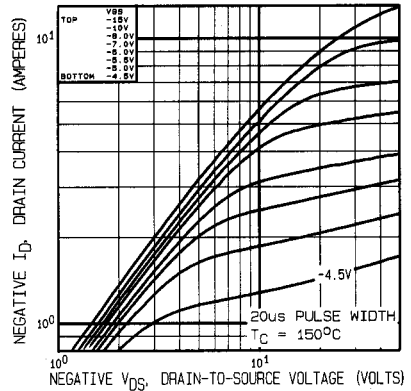


Fig. 2—Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$

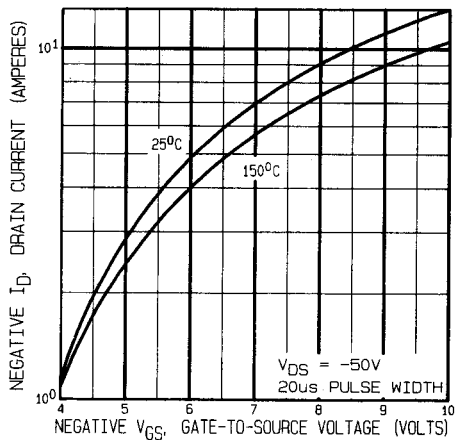


Fig. 3 — Typical Transfer Characteristics

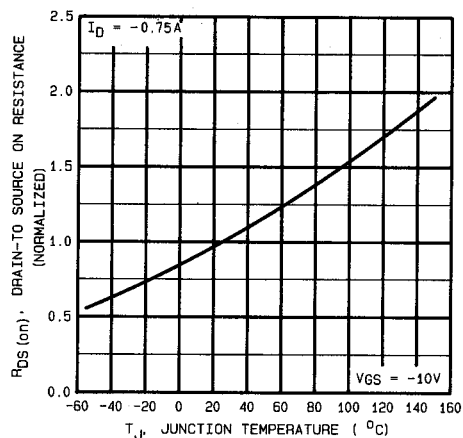


Fig. 4 — Normalized On-Resistance Vs. Temperature

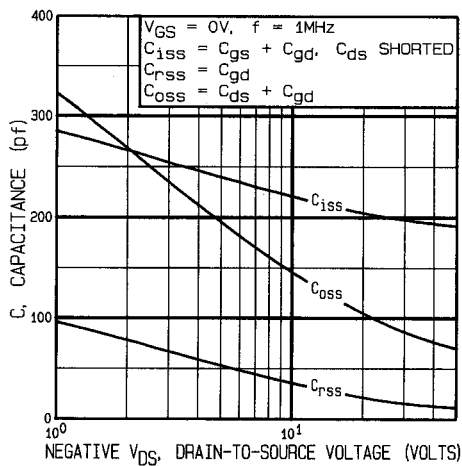


Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage

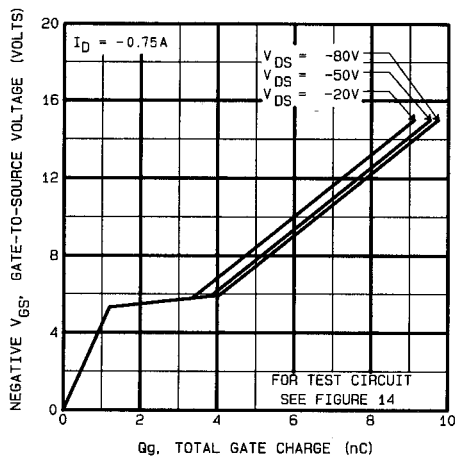


Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage

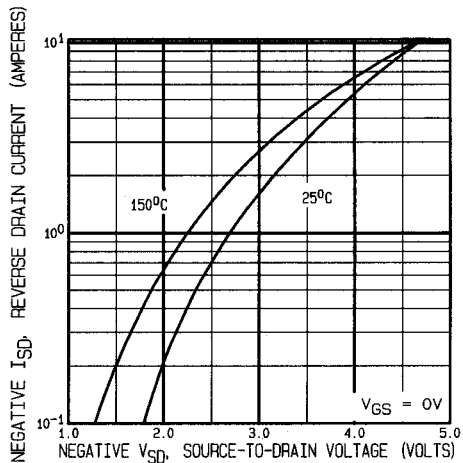


Fig. 7 — Typical Source-Drain Diode Forward Voltage

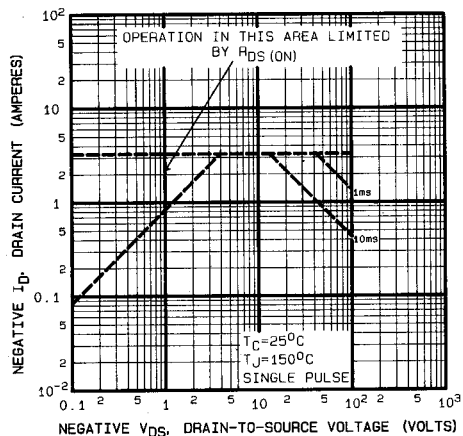


Fig. 8 — Maximum Safe Operating Area

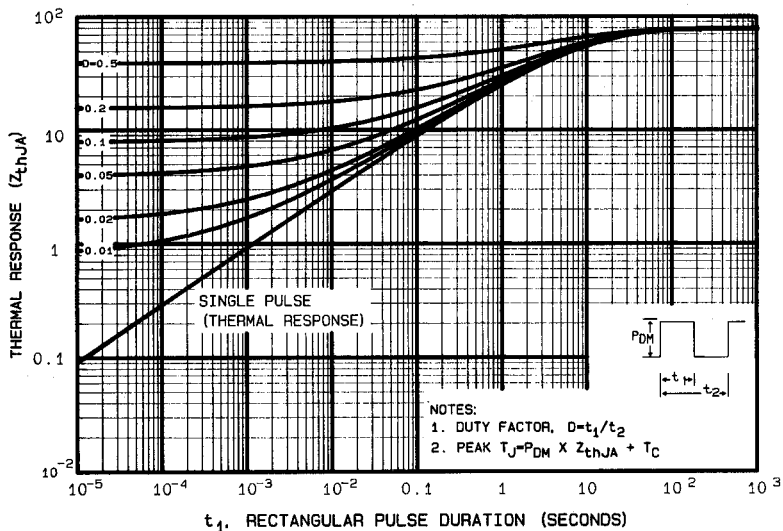


Fig. 9 — Maximum Effective Transient Thermal Impedance, Junction-to-Ambient Vs. Pulse Duration

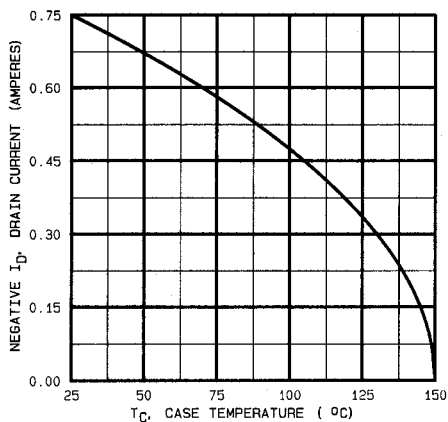


Fig. 10 — Maximum Drain Current Vs. Case Temperature

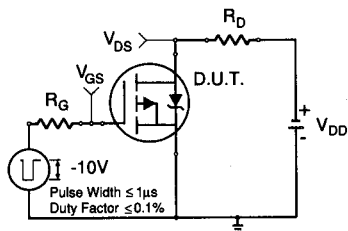


Fig. 11a — Switching Time Test Circuit

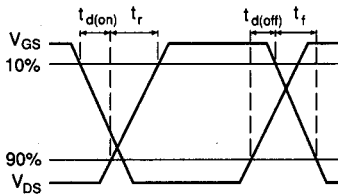


Fig. 11b — Switching Time Waveforms

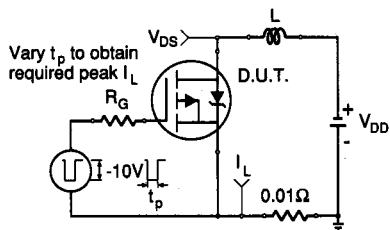


Fig. 12a — Unclamped Inductive Test Circuit

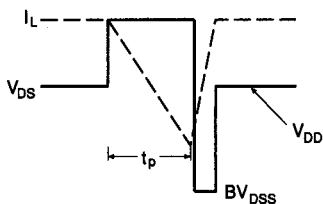


Fig. 12b — Unclamped Inductive Waveforms

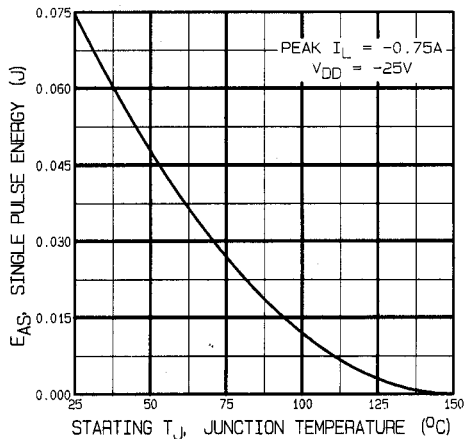
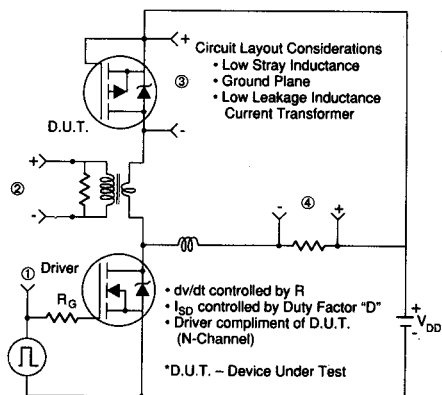
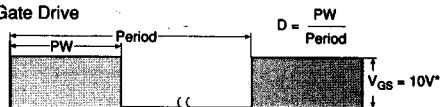
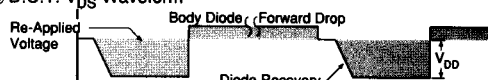
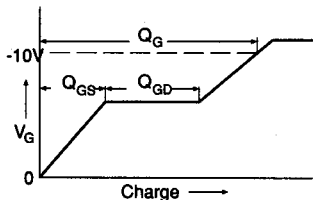
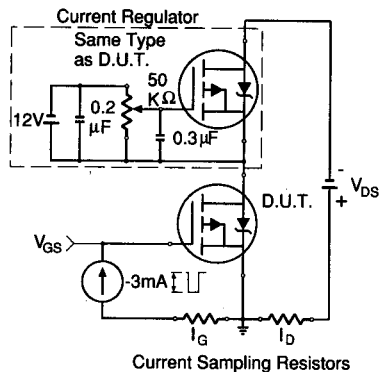


Fig. 12c — Maximum Avalanche Energy Vs. Starting Junction Temperature


① Driver Gate Drive

② D.U.T. I_{SD} Waveform

③ D.U.T. V_{DS} Waveform

④ Inductor Current


* $V_{GS} = 5V$ for Logic Level Devices

Fig. 13 — Peak Diode Recovery dv/dt Test Circuit

Figure. 14a — Basic Gate Charge Waveform

Fig. 14b — Gate Charge Test Circuit