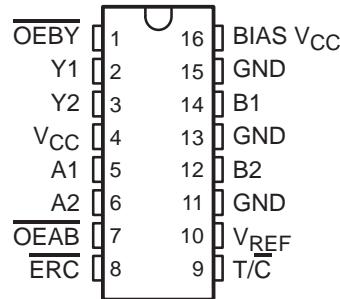


- Bidirectional Interface Between GTL+ Signal Levels and LVTTL Logic Levels
- LVTTL Interfaces Are 5-V Tolerant
- High-Drive GTL+ Outputs (100 mA)
- LVTTL Outputs (-24 mA/24 mA)
- Variable Edge-Rate Control (ERC) Input Selects GTL+ Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity
- I_{off} , Power-Up 3-State, and BIAS V_{CC} Support Live Insertion
- Polarity Control Selects True or Complementary Outputs
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

D, DGV, OR PW PACKAGE

(TOP VIEW)



description

The SN74GTLP1394 is a high-drive 2-bit 3-wire bus transceiver that provides LVTTL-to-GTL+ and GTL+-to-LVTTL signal-level translation. It allows for transparent and inverted transparent modes of data transfer with separate LVTTL input and LVTTL output pins. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTL+ signal levels and is especially designed to work with the Texas Instruments TSB14C01A 1394 Backplane Physical-Layer Controller. High-speed (about two times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, and output edge control (OEC™). Improved GTLP OEC circuits minimize bus settling time and have been designed and tested using several backplane models. The high drive is suitable for driving double-terminated low-impedance backplanes using incident-wave switching.

GTL+ is the Texas Instruments derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The AC specification of the SN74GTLP1394 is given only at the preferred higher noise margin GTL+, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V) or GTL+ ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels.

Normally, the B port operates at GTL or GTL+ levels. The A inputs, Y outputs, and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

This device is fully specified for live-insertion applications using I_{off} , power-up 3-state, and BIAS V_{CC} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

OEC is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Copyright © 1999, Texas Instruments Incorporated



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN74GTLP1394

2-BIT LVTTL-TO-GTL+ ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER WITH SELECTABLE POLARITY

SCES286 – OCTOBER 1999

description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTLP1394 is characterized for operation from -40°C to 85°C .

functional description

The output-enable (\overline{OEAB}) input controls the activity of the B port. When \overline{OEAB} is low, the B-port outputs are active. When \overline{OEAB} is high, the B-port outputs are disabled.

Separate input and output pins allow the device to transmit and receive simultaneously. The \overline{OEY} input controls the Y outputs. When \overline{OEY} is low, the Y outputs are active. When \overline{OEY} is high, the Y outputs are disabled.

The polarity-control (T/\overline{C}) input is provided to select polarity of data transmission in both directions. When T/\overline{C} is high, data transmission is true, and A data goes to the B bus and B data goes to the Y bus. When T/\overline{C} is low, data transmission is complementary, and \overline{A} data goes to the B bus and \overline{B} data goes to the Y bus.

Function Tables

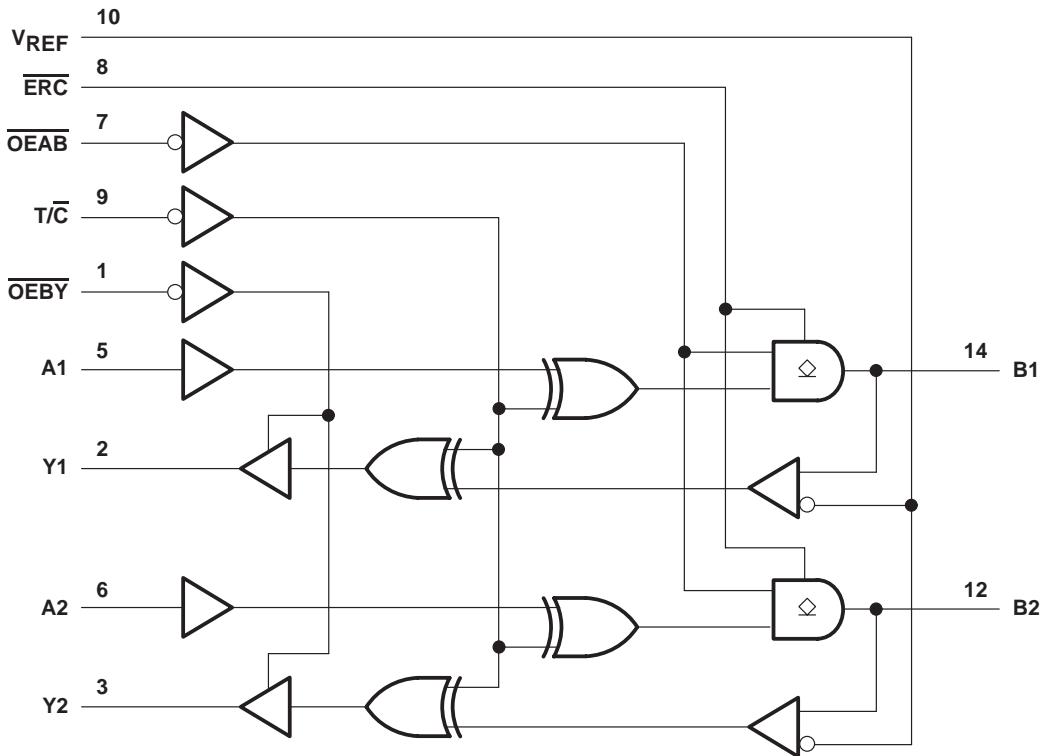
OUTPUT ENABLE

INPUTS			OPERATION OR FUNCTION	MODE
T/C	\overline{OEAB}	\overline{OEY}		
X	H	H	Z	Isolation
H	L	H	A data to B bus	True driver
H	H	L	B data to Y bus	True driver
H	L	L	A data to B bus, B data to Y bus	True transceiver
L	L	H	\overline{A} data to B bus	Inverted driver
L	H	L	\overline{B} data to Y bus	Inverted driver
L	L	L	\overline{A} data to B bus, \overline{B} data to Y bus	Inverted transceiver

OUTPUT EDGE-RATE CONTROL (\overline{ERC})

INPUT \overline{ERC}		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

1. The input and output negative voltage ratings may be exceeded if the input current is negative.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Notes 4 through 6)

			MIN	NOM	MAX	UNIT
V_{CC} , BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port			V_{CC}	
V_{IH}	High-level input voltage	B port	$V_{REF}+0.05$			V
		\overline{ERC}	$V_{CC}-0.6$	V_{CC}		
		Except B port and \overline{ERC}	2			
V_{IL}	Low-level input voltage	B port		$V_{REF}-0.05$		V
		\overline{ERC}		GND	0.6	
		Except B port and \overline{ERC}			0.8	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Y			-24	mA
I_{OL}	Low-level output current	Y			24	mA
		B port			100	
T_A	Operating free-air temperature		-40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Normal connection sequence is GND first, BIAS V_{CC} = 3.3 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. However, if the B-port I/O precharge is not required, the acceptable connection sequence is GND first and V_{CC} = 3.3 V, BIAS V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. When V_{CC} is connected, the BIAS V_{CC} circuitry is disabled.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute I_{OL} ratings. Similarly, V_{REF} can be adjusted to optimize noise margins, but normally is 2/3 V_{TT} .

electrical characteristics over recommended operating free-air temperature range for GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 3.15 \text{ V}$, $I_I = -18 \text{ mA}$				-1.2	V
V_{OH}	Y	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC} = 0.2$				V
		$V_{CC} = 3.15 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2.4				
		$V_{CC} = 3.15 \text{ V}$, $I_{OH} = -24 \text{ mA}$	2				
V_{OL}	Y	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$, $I_{OL} = 100 \mu\text{A}$	0.2				V
		$V_{CC} = 3.15 \text{ V}$, $I_{OL} = 12 \text{ mA}$	0.4				
		$V_{CC} = 3.15 \text{ V}$, $I_{OL} = 24 \text{ mA}$	0.5				
	B port	$V_{CC} = 3.15 \text{ V}$, $I_{OL} = 10 \text{ mA}$	0.2				
		$V_{CC} = 3.15 \text{ V}$, $I_{OL} = 64 \text{ mA}$	0.4				
I_I ‡	B port	$V_{CC} = 3.45 \text{ V}$, $V_I = 0 \text{ to } 1.5 \text{ V}$			±5		μA
	A and control inputs	$V_{CC} = 3.45 \text{ V}$, $V_I = 0 \text{ to } V_{CC}$			±5		
		$V_{CC} = 3.45 \text{ V}$, $V_I = 5.5 \text{ V}$			±5		
I_{CC}	Y or B port	$V_{CC} = 3.45 \text{ V}$, $I_O = 0$, V_I (A or control input) = V_{CC} or GND V_I (B port) = V_{TT} or GND	Outputs high		20		mA
			Outputs low		20		
			Outputs disabled		20		
ΔI_{CC} §		$V_{CC} = 3.45 \text{ V}$, One A or control input at $V_{CC} - 0.6 \text{ V}$, Other A or control inputs at V_{CC} or GND				1.5	mA
C_i	A	$V_I = 3.15 \text{ V or } 0$					pF
	Control inputs						
C_o	Y	$V_O = 3.15 \text{ V or } 0$					pF
C_{io}	B port	$V_O = 1.5 \text{ V or } 0$					pF

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.‡ For I/O ports, the parameter I_I includes the off-state output leakage current.§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

live-insertion specifications for A and Y over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	BIAS $V_{CC} = 0$,	V_I or $V_O = 0 \text{ to } 5.5 \text{ V}$		100	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$,	$V_O = 0.5 \text{ V to } 3 \text{ V}$,	$\overline{OE} = 0$		±100	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$,	$V_O = 0.5 \text{ V to } 3 \text{ V}$,	$\overline{OE} = 0$		±100	μA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	BIAS $V_{CC} = 0$,	V_I or $V_O = 0 \text{ to } 1.5 \text{ V}$		100	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$,	$V_O = 0.5 \text{ V to } 1.5 \text{ V}$,	$\overline{OE} = 0$		±100	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$,	$V_O = 0.5 \text{ V to } 1.5 \text{ V}$,	$\overline{OE} = 0$		±100	μA
I_{CC} (BIAS V_{CC})	$V_{CC} = 0 \text{ to } 3.15 \text{ V}$	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$,	V_O (B port) = 0 to 1.5 V		5	mA
	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$				10	μA
V_O	$V_{CC} = 0$,	BIAS $V_{CC} = 3.3 \text{ V}$		0.95	1.05	V
I_O	$V_{CC} = 0$,	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$,	V_O (B port) = 0.6 V	-1		μA

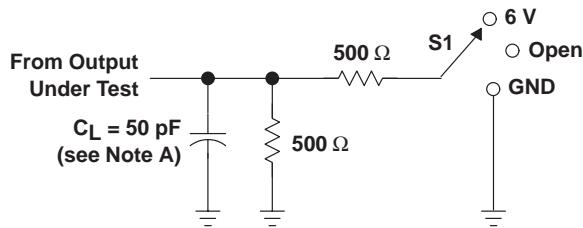
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE [†]	MIN	TYP [‡]	MAX	UNIT		
t_{pd}	A	B	Slow				ns		
			Fast						
		Y	Slow						
			Fast						
	T/C	B	Slow				ns		
			Fast						
			Slow						
		B	Fast						
			Slow						
			Fast						
t_{en}	\overline{OEAB}	B	Slow				ns		
t_{dis}									
t_{en}	\overline{OEAB}	B	Fast				ns		
t_{dis}									
t_r	Rise time, B outputs (0.6 V to 1.3 V)			Slow			ns		
t_f	Fall time, B outputs (1.3 V to 0.6 V)			Fast					
t_{pd}	B T/C	Y					ns		
t_{en}									
t_{dis}	\overline{OEBY}	Y					ns		

[†]Slow ($\overline{ERC} = GND$) and Fast ($\overline{ERC} = V_{CC}$)

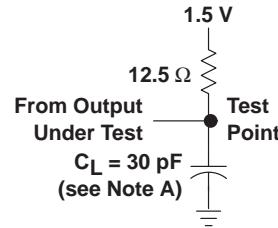
[‡]All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$.

PARAMETER MEASUREMENT INFORMATION

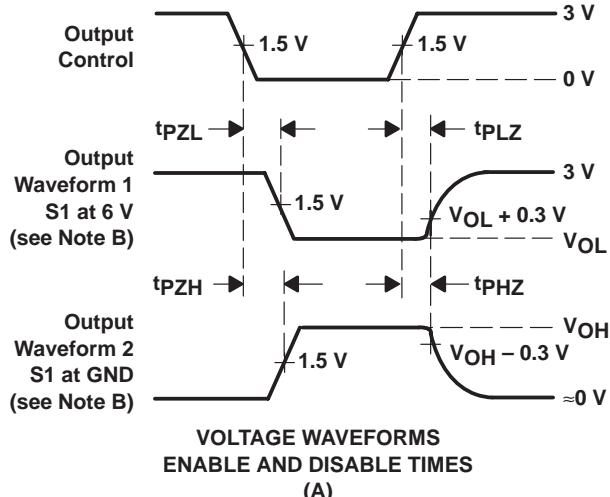
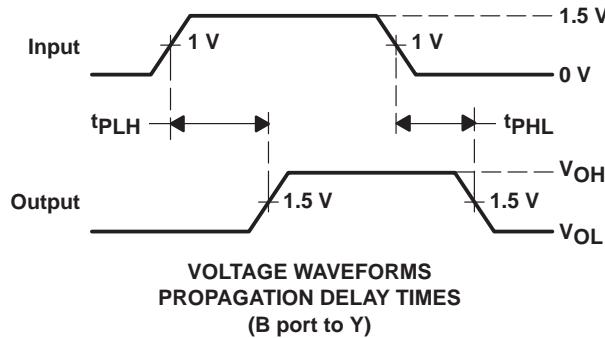
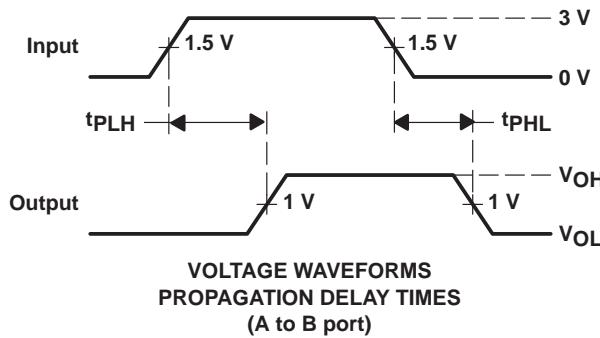


LOAD CIRCUIT FOR Y OUTPUTS

TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	6 V
tPHZ/tPZH	GND



LOAD CIRCUIT FOR B OUTPUTS



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, slew rate $\leq 1 \text{ V/ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

This data sheet is specified for and tested to the lump load shown in Figure 1. However, the designer probably uses this GTLP device in a distributed load like that shown in Figure 2, in which actual B-port backplane switching characteristics are different. Therefore, the device is modeled as shown in Figure 3, which very closely matches the results obtained using Figure 2. Switching characteristics based on Figure 3 more closely match actual backplane design requirements.

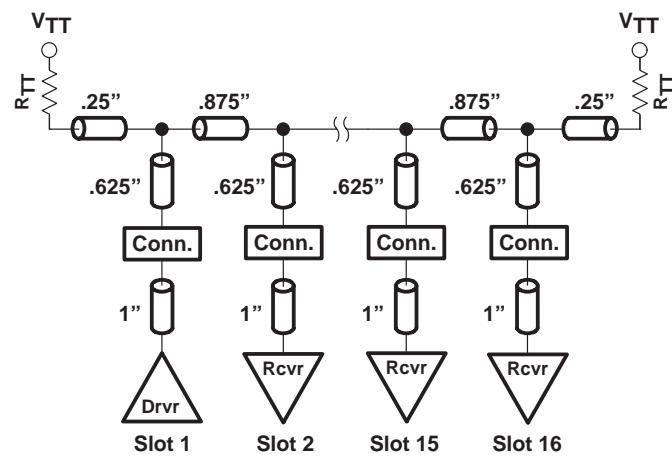


Figure 2. Test Backplane Model

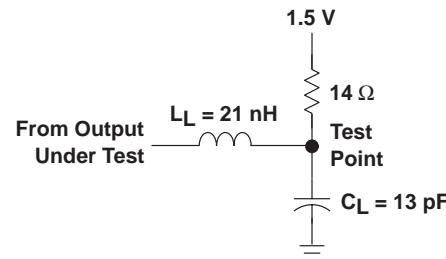


Figure 3. Distributed-Load Circuit for B Outputs

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTL+ (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE [†]	MIN	TYP [‡]	MAX	UNIT
t_{pd}	A	B	Slow				ns
			Fast				
		Y	Slow				
	T/C	B	Fast				
			Slow				
			Fast				
t_{en}	OEAB	B	Slow				ns
t_{dis}			Fast				
t_{en}	OEAB	B	Fast				ns
t_{dis}			Slow				
t_r	Rise time, B outputs (0.6 V to 1.3 V)		Fast				ns
t_f			Slow				
	Fall time, B outputs (1.3 V to 0.6 V)		Fast				ns
			Slow				

[†] Slow ($\overline{ERC} = GND$) and Fast ($\overline{ERC} = V_{CC}$)

[‡] All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated