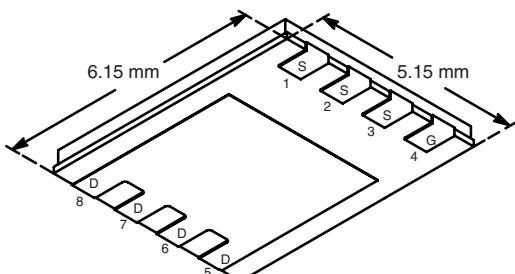


N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
25	0.0028 at $V_{GS} = 10$ V	50 ^{a, g}	29.5 nC
	0.0038 at $V_{GS} = 4.5$ V	50 ^{a, g}	

PowerPAK® SO-8



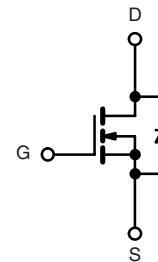
Bottom View

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- New MOSFET Technology Optimized for Ringing Reduction in Switching Applications
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Low-Side MOSFET
 - Server, V_{core}
 - DC/DC



N-Channel MOSFET

Ordering Information: SiR844DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	50 ^{a, g}	A
		50 ^g	
		30 ^{b, c}	
		24 ^{b, c}	
Pulsed Drain Current	I_{DM}	70	
Continuous Source-Drain Diode Current	I_S	50 ^g	
		4.5 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	40	mJ
Single Pulse Avalanche Energy	E_{AS}	80	
Maximum Power Dissipation	P_D	50	W
		32	
		5.0 ^{b, c}	
		3.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	2.0	2.5	

Notes:

- Based on $T_C = 25$ °C.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 70 °C/W.
- Package limited.



SiR844DP

Vishay Siliconix

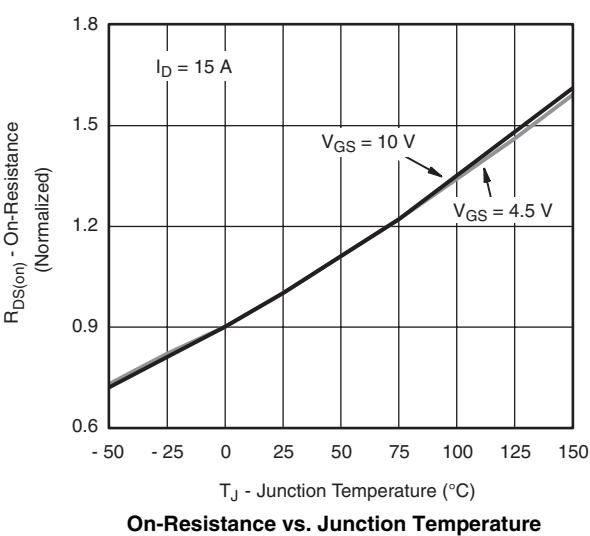
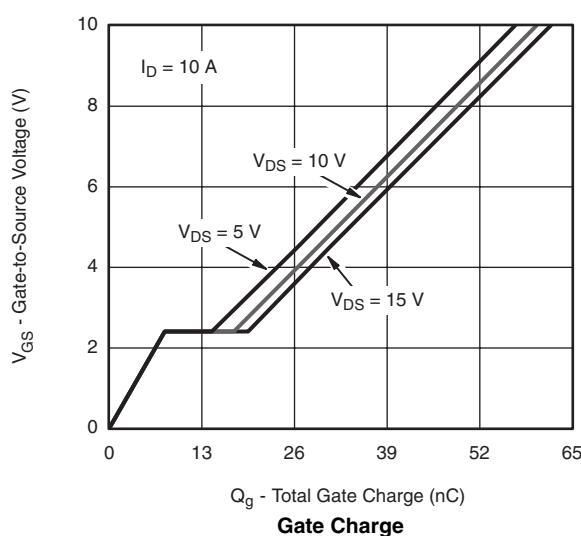
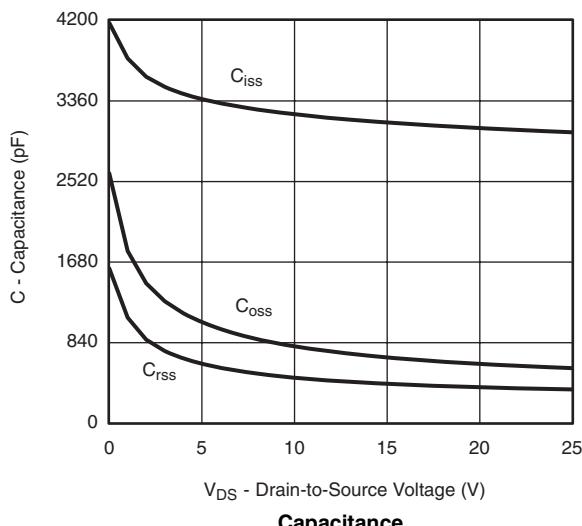
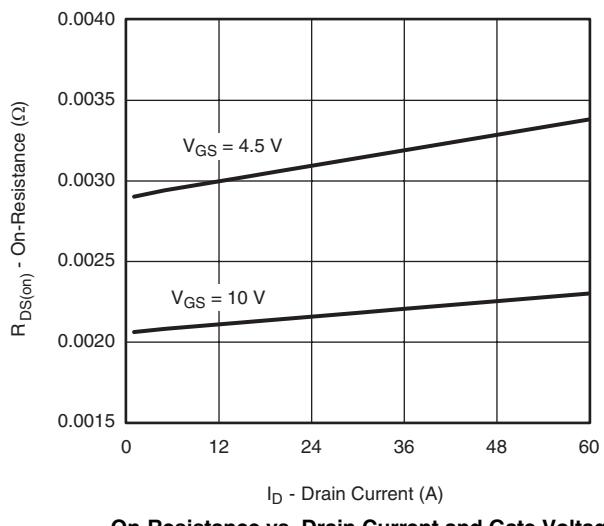
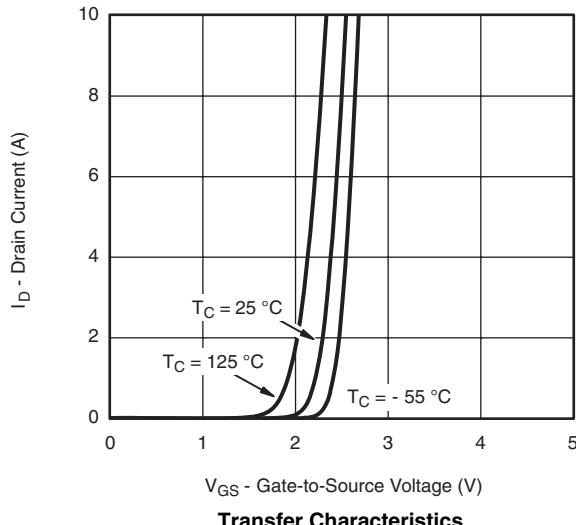
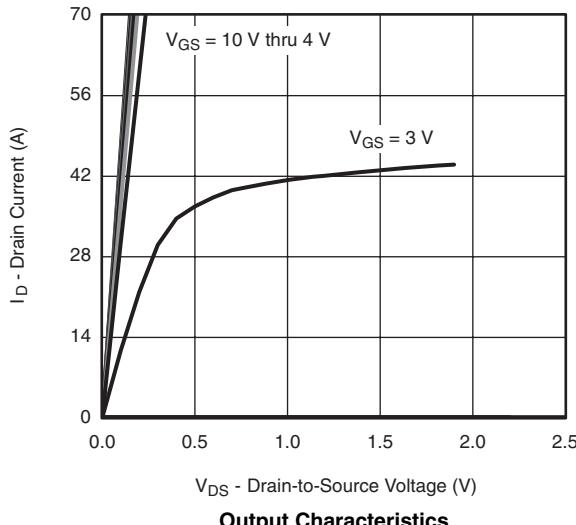
**SPECIFICATIONS** $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	25			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		20		mV/ $^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 5.6		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	1.0		2.6	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$		1		μA
		$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$		0.0022	0.0028	Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 10 \text{ A}$		0.0030	0.0038	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}$, $I_D = 15 \text{ A}$		50		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		3215		pF
Output Capacitance	C_{oss}			800		
Reverse Transfer Capacitance	C_{rss}			475		
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$		60	90	nC
Gate-Source Charge	Q_{gs}			29.5	44	
Gate-Drain Charge	Q_{gd}			7.8		
Gate Resistance	R_g		$f = 1 \text{ MHz}$	0.15	0.6	1.2
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 10 \text{ V}$, $R_L = 1 \Omega$ $I_D \geq 10 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$		14	28	ns
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(\text{off})}$			33	60	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(\text{on})}$			30	55	
Rise Time	t_r	$V_{DD} = 10 \text{ V}$, $R_L = 1 \Omega$ $I_D \geq 10 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$		21	40	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			39	75	
Fall Time	t_f			18	35	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			50	A
Pulse Diode Forward Current ^a	I_{SM}				70	
Body Diode Voltage	V_{SD}	$I_S = 3 \text{ A}$		0.73	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}			15	30	nC
Reverse Recovery Fall Time	t_a			13		ns
Reverse Recovery Rise Time	t_b			12		

Notes:

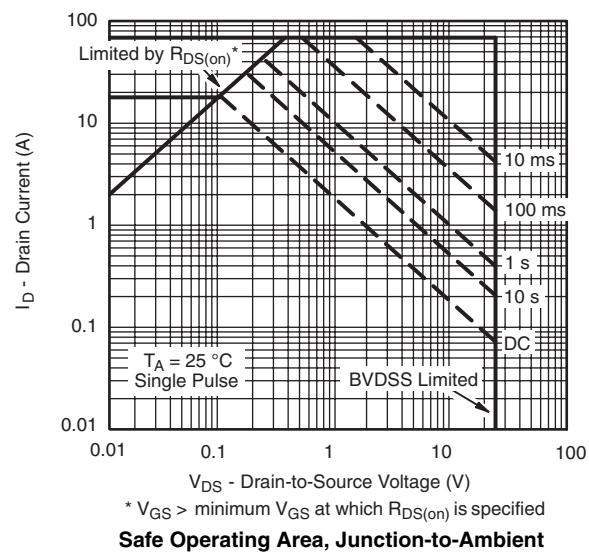
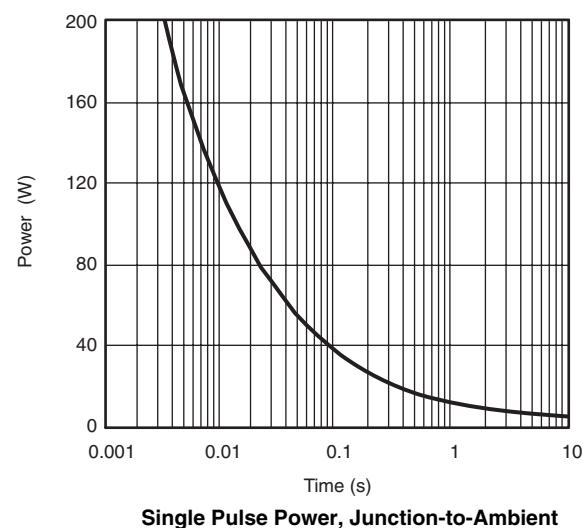
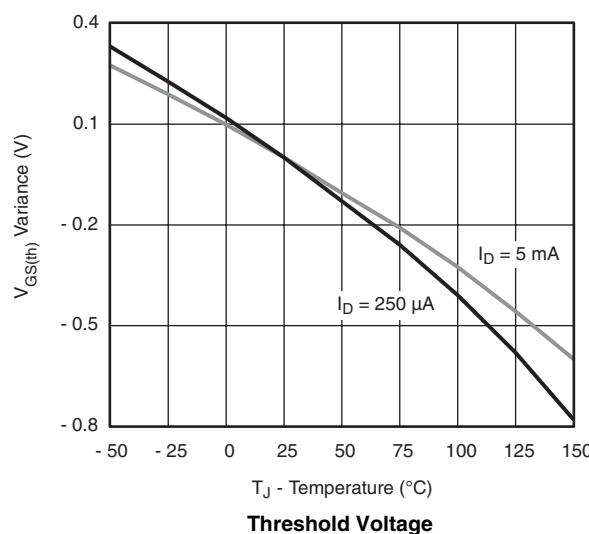
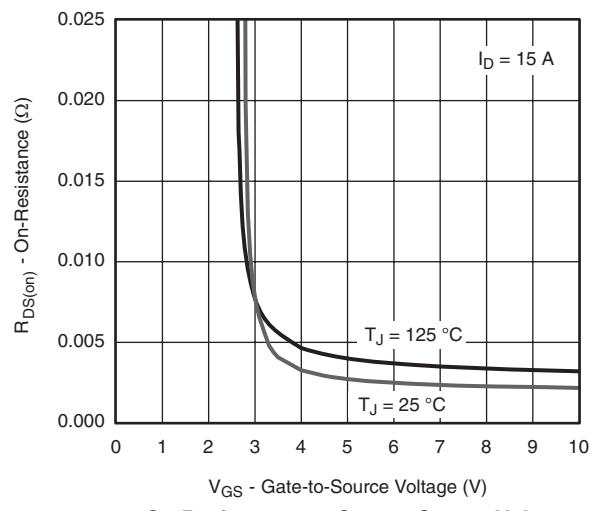
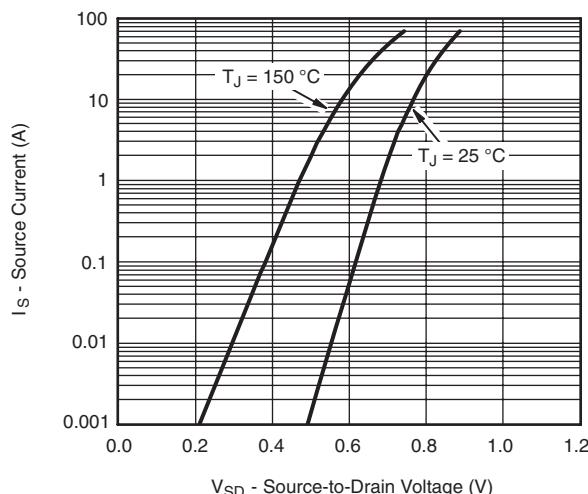
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

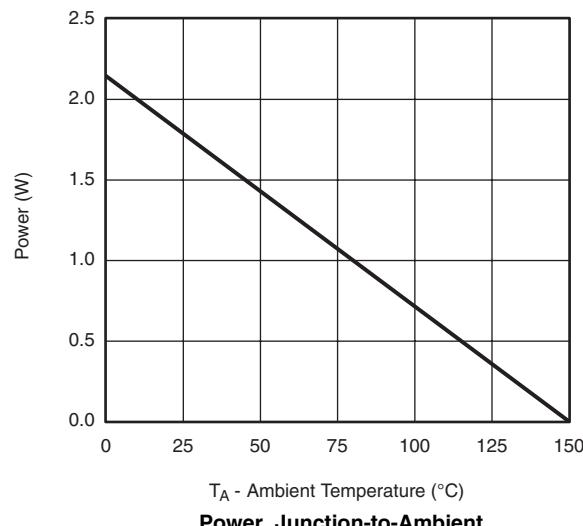
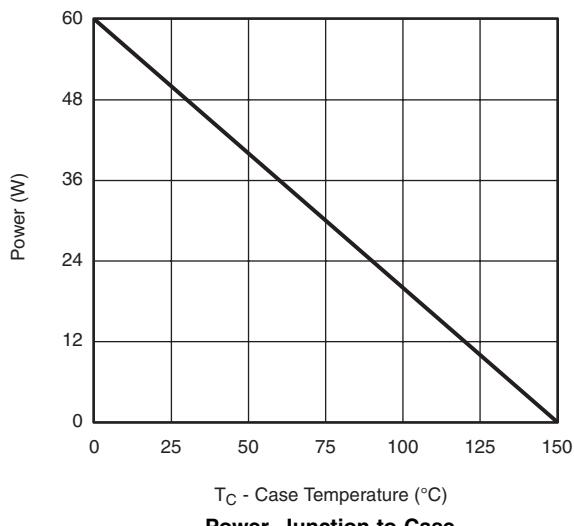
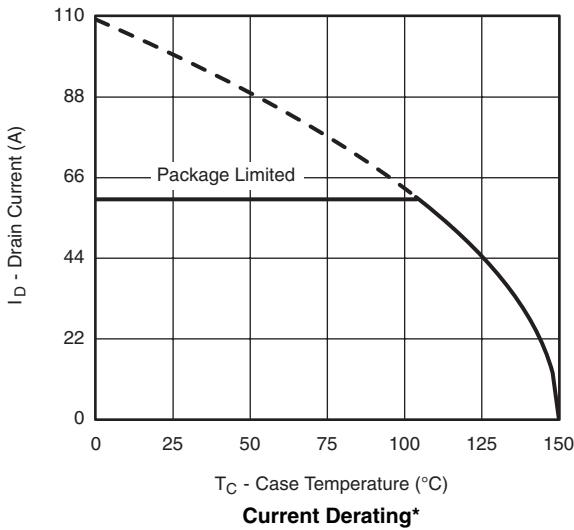
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


SiR844DP

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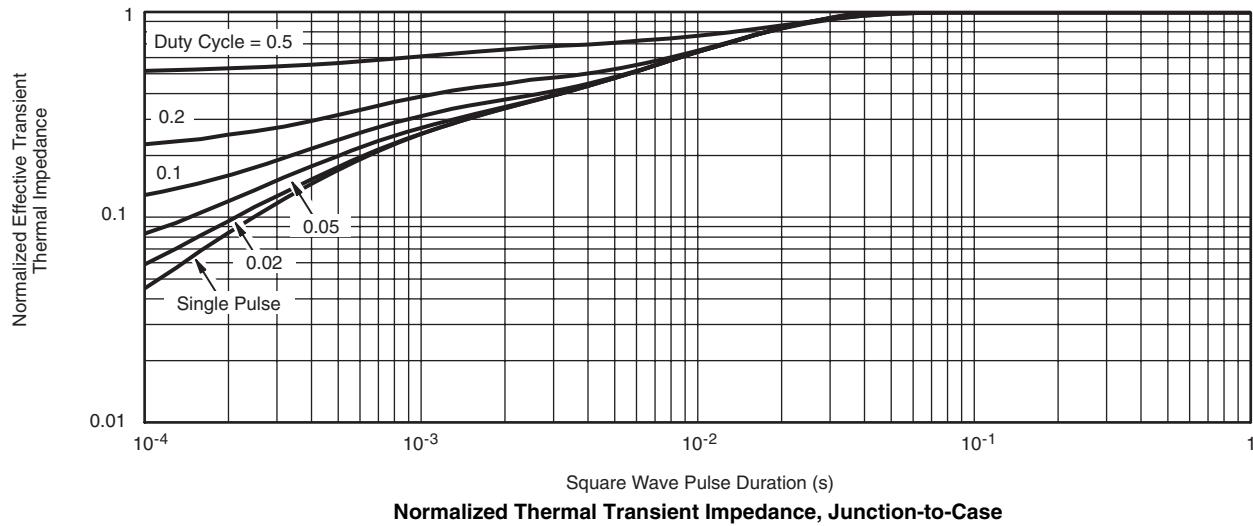
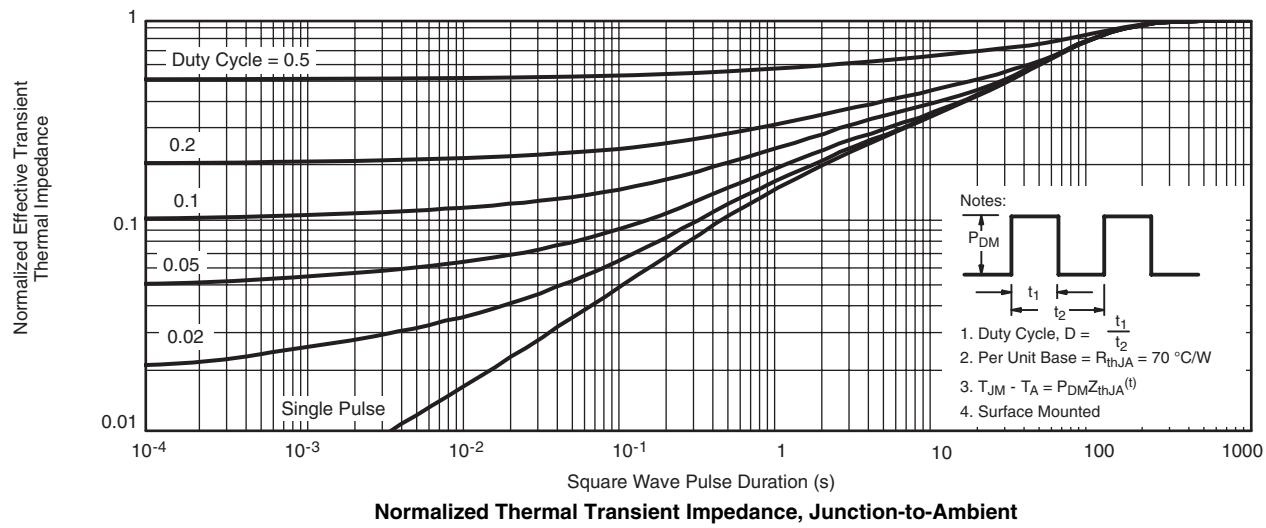
* The power dissipation P_D is based on $T_{J(\max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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