FemtoClock™ Crystal-to-LVDS 400MHz Frequency Synthesizer

ICS844801I-24

PRELIMINARY DATASHEET

General Description

The ICS844801I-24 is a 400MHz Frequency Synthesizer. The ICS844801I-24 uses an 18pF parallel resonant crystal over the range of 21.5625MHz - 25.3125MHz. The ICS844801I-24 has excellent <1ps phase jitter performance, over the 12kHz - 20MHz integration range. The ICS844801I-24 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

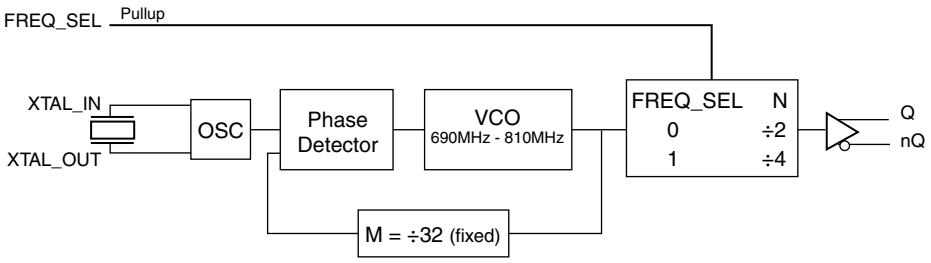
Features

- One differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (21.5625MHz – 25.3125MHz)
- Output frequency ranges: 172.5MHz – 202.5MHz, and 345MHz – 405MHz
- VCO range: 690MHz – 810MHz
- RMS phase jitter at 400MHz, using a 25MHz crystal (12kHz – 20MHz): 0.57ps (typical) @ 3.3V
- Full 3.3V or 2.5V output supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

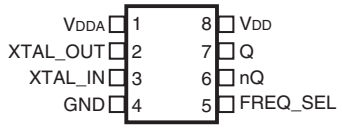
Common Configuration Table

Inputs					Output Frequency (MHz)
Crystal Frequency (MHz)	FREQ_SEL	M	N	Multiplication Value M/N	
25	0	32	2	16	400
25	1	32	4	8	200

Block Diagram



Pin Assignment



ICS844801I-24
8 Lead TSSOP
4.40mm x 3.0mm x 0.925mmpackage body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2, 3	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	GND	Power		Power supply ground.
5	FREQ_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. LVDS interface levels.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Ohter Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.07	3.3	V_{DD}	V
I_{DD}	Power Supply Current				83	mA
I_{DDA}	Analog Supply Current				7	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.07	2.5	V_{DD}	V
I_{DD}	Power Supply Current				78	mA
I_{DDA}	Analog Supply Current				7	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V	2		V_{DD} + 0.3	V
		V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V	-0.3		0.8	V
		V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 3D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			415		mV
ΔV_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage			1.22		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 3E. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			380		mV
ΔV_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage			1.17		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		21.5625		25.3125	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

AC Electrical Characteristics

Table 5A. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		172.5		202.5	MHz
			345		405	MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	200MHz, Integration Range: 12kHz – 20MHz		0.62		ps
		400MHz, Integration Range: 12kHz – 20MHz		0.57		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		305		ps
odc	Output Duty Cycle			50		%

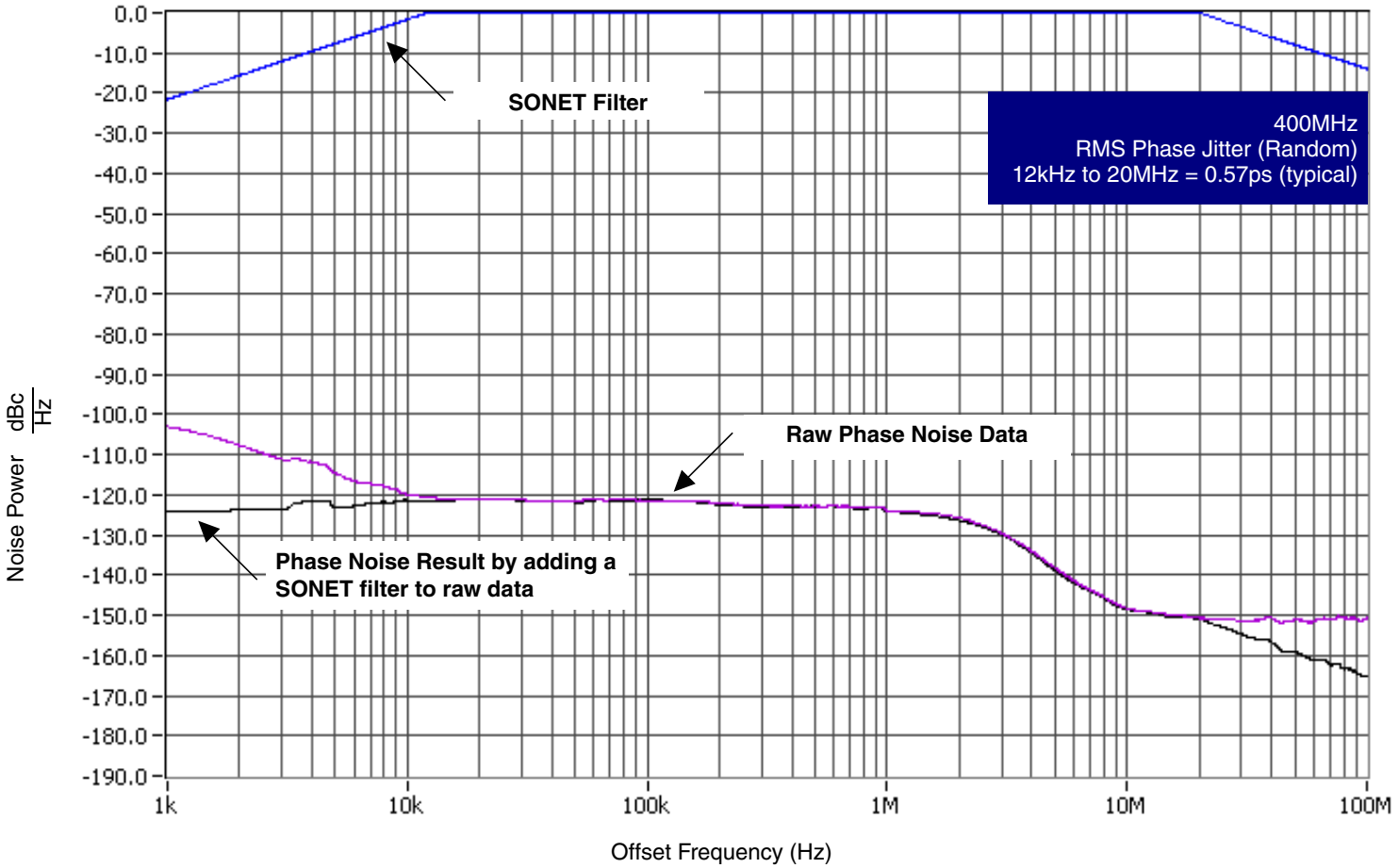
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to Phase Noise Plot.

Table 5B. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°

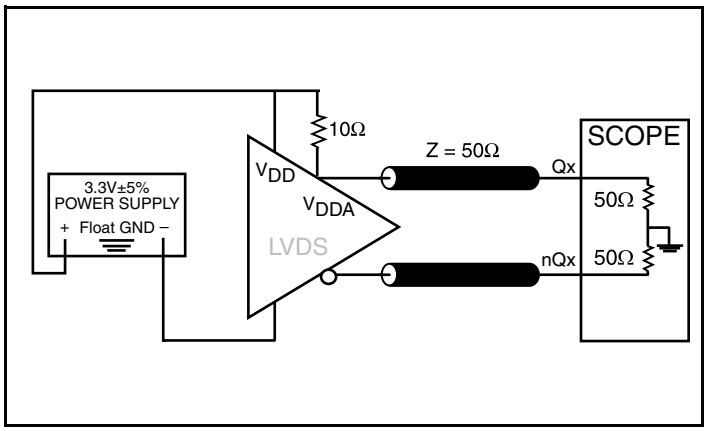
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		172.5		202.5	MHz
			345		405	MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random	200MHz, Integration Range: 12kHz – 20MHz		0.64		ps
		400MHz, Integration Range: 12kHz – 20MHz		0.57		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		310		ps
odc	Output Duty Cycle			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

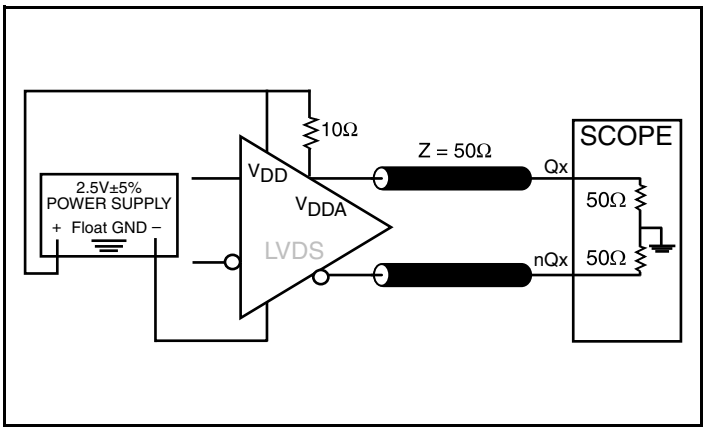
Typical Phase Noise at 400MHz (3.3V)



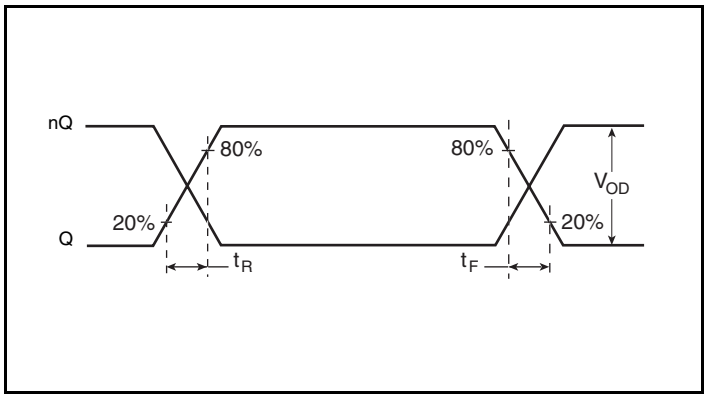
Parameter Measurement Information



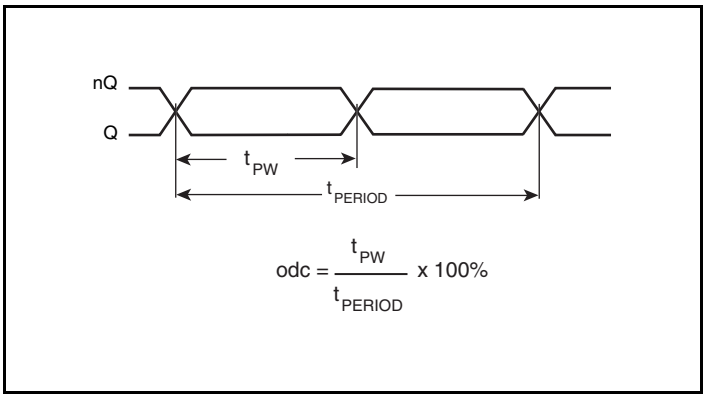
3.3V LVDS Output Load AC Test Circuit



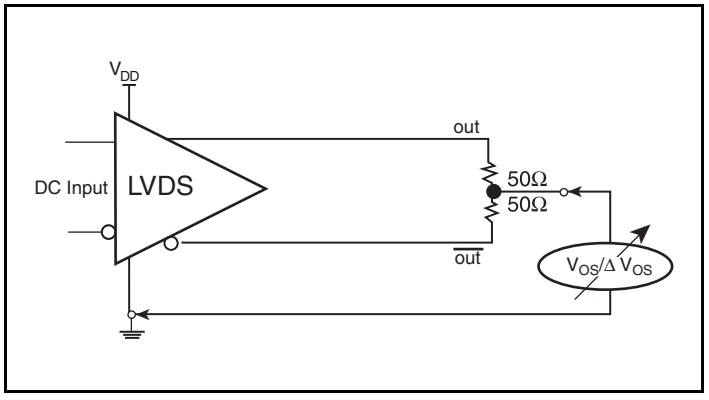
2.5V LVDS Output Load AC Test Circuit



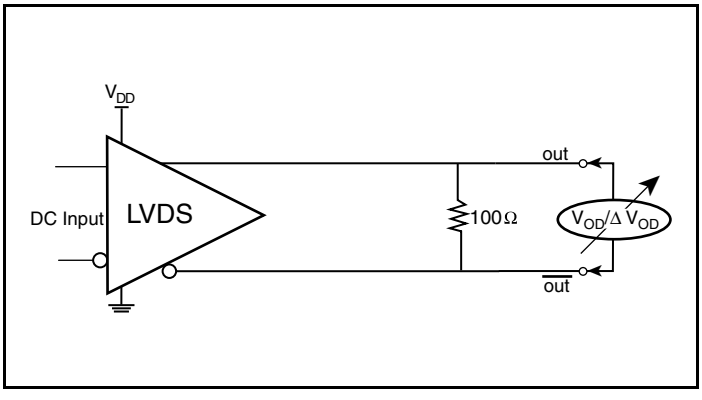
Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

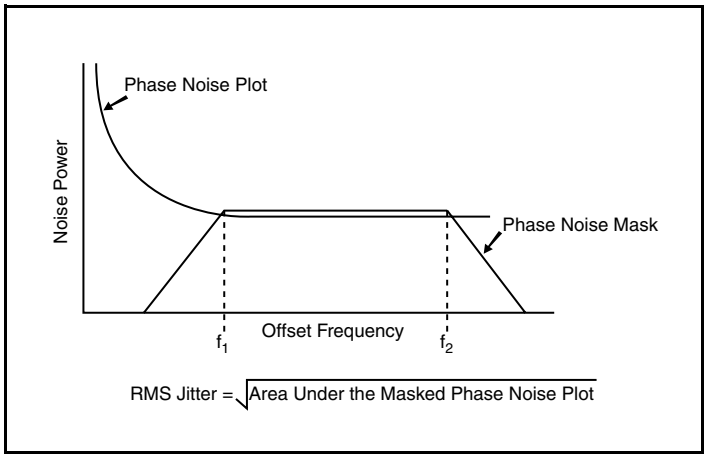


Offset Voltage Setup



Differential Output Voltage Setup

Parameter Measurement Information, continued



RMS Phase Jitter

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844801I-24 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

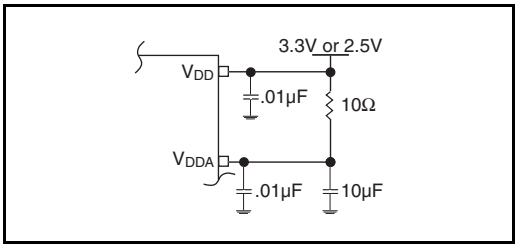


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS844801I-24 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

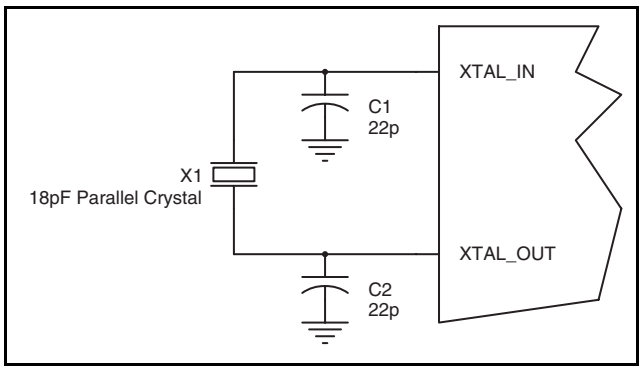


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

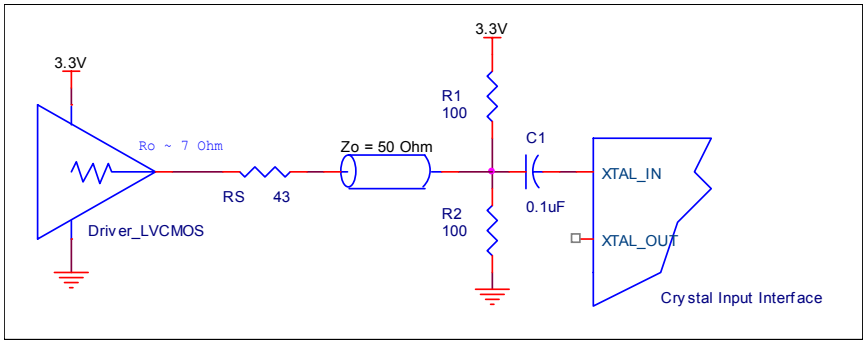


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

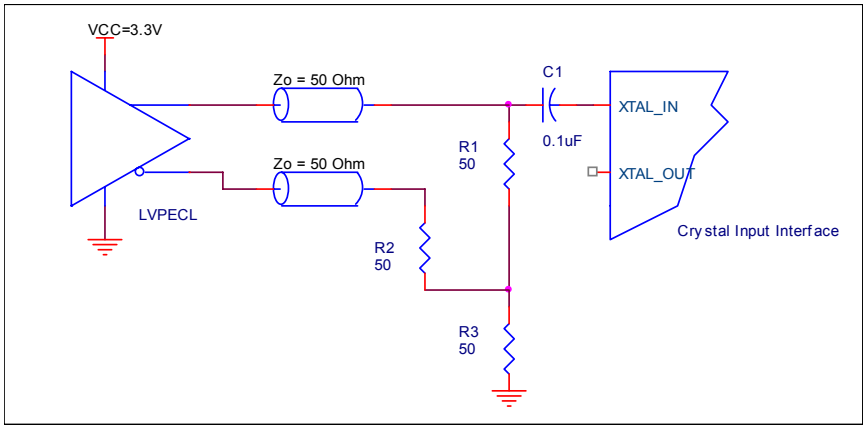


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure X can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

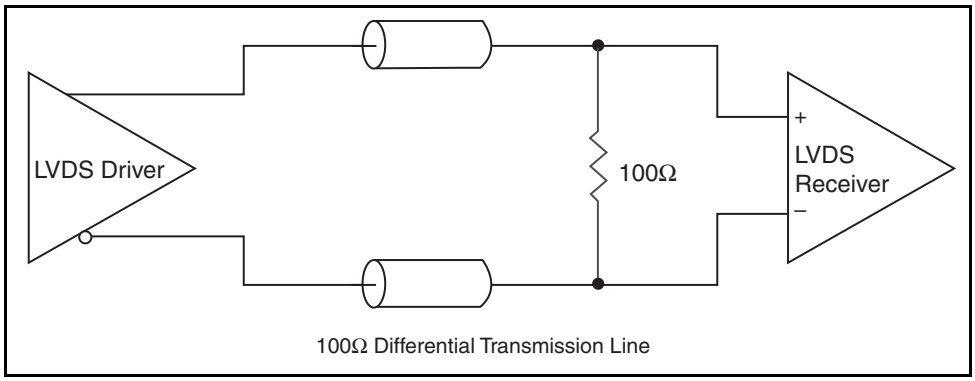


Figure 4. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844801I-24.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844801I-24 is the sum of the core power plus the analog power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (83mA + 7mA) = **311.85mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 125.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.312W * 125.5°C/W = 124.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Transistor Count

The transistor count for ICS844801I-24 is: 1662

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

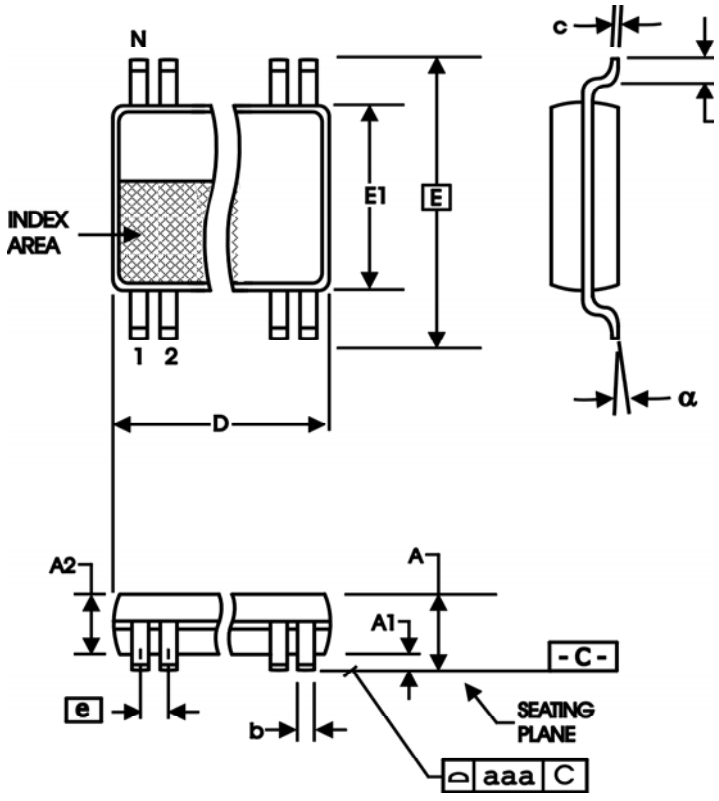


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844801AGI-24	4AI24	8 Lead TSSOP	Tube	-40°C to 85°C
844801AGI-24T	4AI24	8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
844801AGI-24LF	AI24L	“Lead-Free” 8 Lead TSSOP	Tube	-40°C to 85°C
844801AGI-24LFT	AI24L	“Lead-Free” 8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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