

60MHz Rail-to-Rail Input-Output Op Amp

The EL5211A is a low power, high voltage, rail-to-rail input-output amplifier. The EL5211A contains two amplifiers. Operating on nominal supplies ranging from 5V to 15V while consuming only 2.5mA per amplifier, the EL5211A has a bandwidth of 60MHz (-3dB) and provides common-mode input ability beyond the supply rails, as well as rail-to-rail output capability. This enables the EL5211A to offer maximum dynamic range at any supply voltage.

The EL5211A also features fast slewing and settling times, as well as a high continuous output drive capability of 65mA (sink and source). These features make the EL5211A ideal for high speed filtering and signal conditioning application. Other applications include battery-powered, portable devices and anywhere low power consumption is important.

The EL5211A is available in the 8 Ld HMSOP package, features a standard operational amplifier pinout, and is specified for operation over a temperature range of -40°C to +85°C.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
EL5211AIYEZ	BBLAA	8 Ld HMSOP (3.0mm)	MDP0050
EL5211AIYEZ-T7*	BBLAA	8 Ld HMSOP (3.0mm)	MDP0050
EL5211AIYEZ-T13*	BBLAA	8 Ld HMSOP (3.0mm)	MDP0050

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

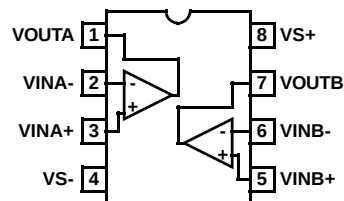
- 60MHz (-3dB) bandwidth
- Supply voltage = 4.5V to 16.5V
- Low supply current (per amplifier) = 2.5mA
- High slew rate = 75V/μs
- Unity-gain stable
- Beyond the rails input capability
- Rail-to-rail output swing
- ±110mA output short current
- Pb-free (RoHS compliant)

Applications

- TFT-LCD panels
- V_{COM} amplifiers
- Drivers for A/D converters
- Data acquisition
- Video processing
- Audio processing
- Active filters
- Test equipment
- Battery-powered applications
- Portable equipment

Pinout

EL5211A
(8 LD HMSOP)
TOP VIEW



Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$)

Supply Voltage between V_{S+} and V_{S-} +18V
 Input Voltage $V_{S-} - 0.5\text{V}$, $V_{S+} + 0.5\text{V}$
 Maximum Continuous Output Current $\pm 65\text{mA}$

Thermal Information

Storage Temperature -65°C to $+150^\circ\text{C}$
 Ambient Operating Temperature -40°C to $+85^\circ\text{C}$
 Maximum Die Temperature $+150^\circ\text{C}$
 Power Dissipation See Curves
 Pb-Free Reflow Profile. see link below
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_{S+} = +5\text{V}$, $V_{S-} = -5\text{V}$, $R_L = 1\text{k}\Omega$ to 0V , $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ\text{C}$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 0\text{V}$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{CM} = 0\text{V}$		2	60	nA
R_{IN}	Input Impedance			1		$\text{G}\Omega$
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -5.5V to 5.5V	50	70		dB
A_{VOL}	Open-Loop Gain	$-4.5\text{V} \leq V_{OUT} \leq 4.5\text{V}$	60	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5\text{mA}$		-4.9	-4.8	V
V_{OH}	Output Swing High	$I_L = 5\text{mA}$	4.8	4.9		V
I_{SC}	Short-Circuit Current			± 110		mA
I_{OUT}	Output Current			± 65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from $\pm 2.25\text{V}$ to $\pm 7.75\text{V}$	60	80		dB
I_S	Supply Current	No load		5	7.5	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	$-4.0\text{V} \leq V_{OUT} \leq 4.0\text{V}$, 20% to 80%		75		$\text{V}/\mu\text{s}$
t_S	Settling to $\pm 0.1\%$ ($A_V = +1$)	($A_V = +1$), $V_O = 2\text{V}$ step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		$^\circ$
CS	Channel Separation	$f = 5\text{MHz}$		110		dB
d_G	Differential Gain (Note 3)	$R_F = R_G = 1\text{k}\Omega$ and $V_{OUT} = 1.4\text{V}$		0.17		%
d_P	Differential Phase (Note 3)	$R_F = R_G = 1\text{k}\Omega$ and $V_{OUT} = 1.4\text{V}$		0.24		$^\circ$

NOTES:

1. Measured over operating temperature range.
2. Slew rate is measured on rising and falling edges.
3. NTSC signal generator used.

Electrical Specifications $V_{S+} = +5V$, $V_{S-} = 0V$, $R_L = 1k\Omega$ to $2.5V$, $T_A = +25^\circ C$, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 4)			7		$\mu V/^\circ C$
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	60	nA
R_{IN}	Input Impedance			1		$G\Omega$
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 5.5V	45	66		dB
A_{VOL}	Open-Loop Gain	$0.5V \leq V_{OUT} \leq 4.5V$	60	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		100	200	mV
V_{OH}	Output Swing High	$I_L = 5mA$	4.8	4.9		V
I_{SC}	Short-Circuit Current			± 110		mA
I_{OUT}	Output Current			± 65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current	No load		5	7.5	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 5)	$1V \leq V_{OUT} \leq 4V$, 20% to 80%		75		V/ μs
t_S	Settling to $+0.1\%$ ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		$^\circ$
CS	Channel Separation	$f = 5MHz$		110		dB
d_G	Differential Gain (Note 6)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.17		%
d_P	Differential Phase (Note 6)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.24		$^\circ$

NOTES:

- Measured over operating temperature range.
- Slew rate is measured on rising and falling edges.
- NTSC signal generator used.

Electrical Specifications $V_{S+} = +15V$, $V_{S-} = 0V$, $R_L = 1k\Omega$ to $7.5V$, $T_A = +25^\circ C$, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 7.5V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 7)			7		$\mu V/^\circ C$
I_B	Input Bias Current	$V_{CM} = 7.5V$		2	60	nA
R_{IN}	Input Impedance			1		$G\Omega$

Electrical Specifications $V_{S+} = +15V$, $V_{S-} = 0V$, $R_L = 1k\Omega$ to $7.5V$, $T_A = +25^\circ C$, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+15.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 15.5V	53	72		dB
A_{VOL}	Open-Loop Gain	$0.5V \leq V_{OUT} \leq 14.5V$	60	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		100	200	mV
V_{OH}	Output Swing High	$I_L = 5mA$	14.8	14.9		V
I_{SC}	Short-Circuit Current			± 110		mA
I_{OUT}	Output Current			± 65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current	No load		5	7.5	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 8)	$1V \leq V_{OUT} \leq 14V$, 20% to 80%		75		V/ μs
t_S	Settling to $\pm 0.1\%$ ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		$^\circ$
CS	Channel Separation	$f = 5MHz$		110		dB
d_G	Differential Gain (Note 9)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.16		%
d_P	Differential Phase (Note 9)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.22		$^\circ$

NOTES:

7. Measured over operating temperature range.
8. Slew rate is measured on rising and falling edges.
9. NTSC signal generator used.

Typical Performance Curves

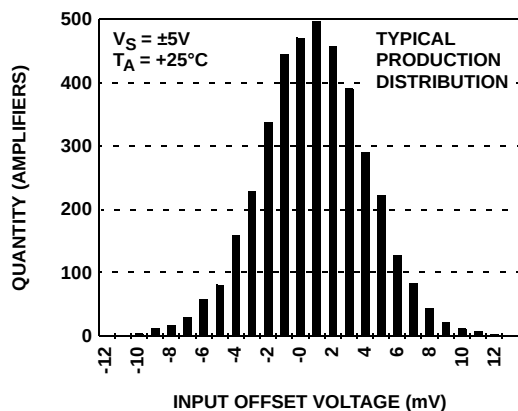


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

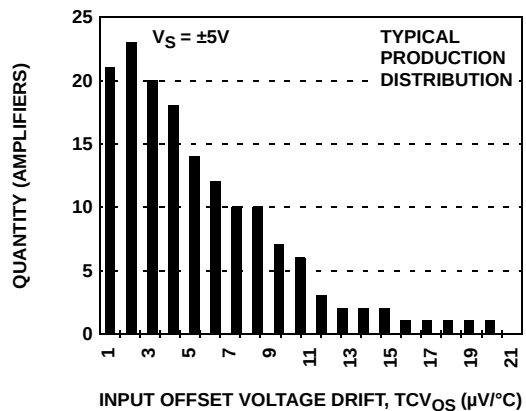


FIGURE 2. INPUT OFFSET VOLTAGE DRIFT

Typical Performance Curves (Continued)

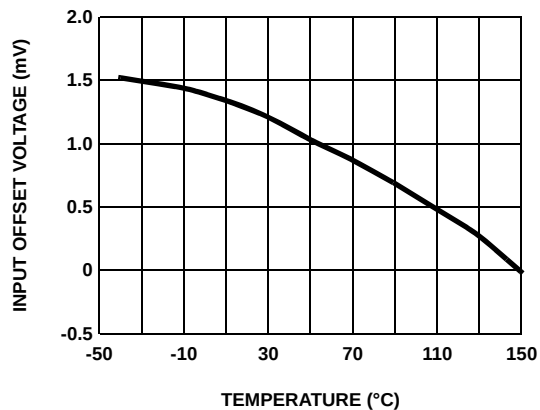


FIGURE 3. INPUT OFFSET VOLTAGE vs TEMPERATURE

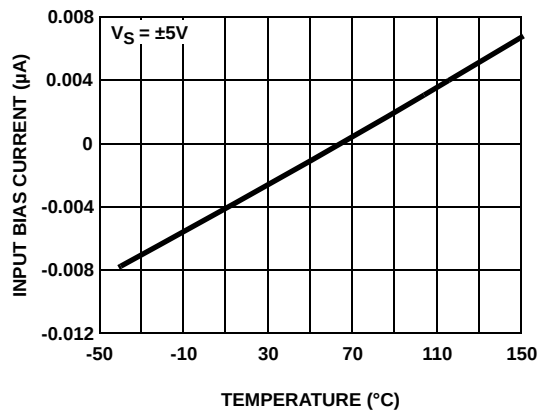


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

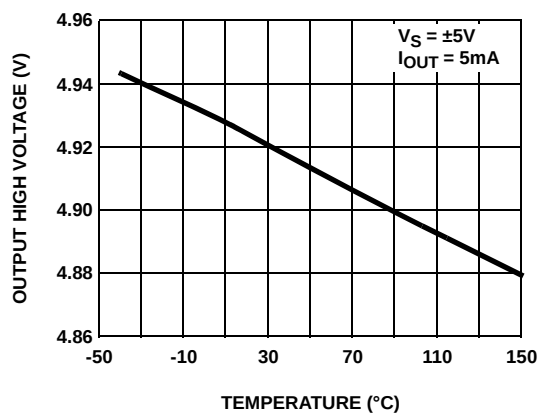


FIGURE 5. OUTPUT HIGH VOLTAGE vs TEMPERATURE

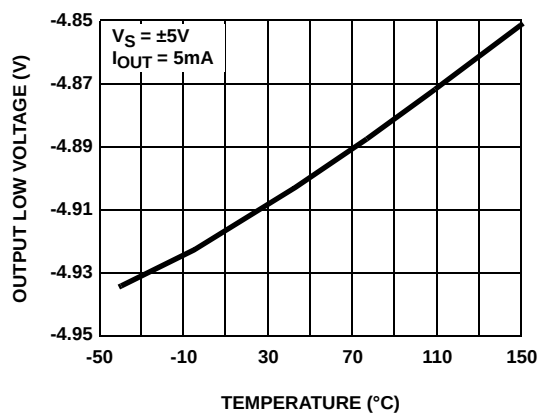


FIGURE 6. OUTPUT LOW VOLTAGE vs TEMPERATURE

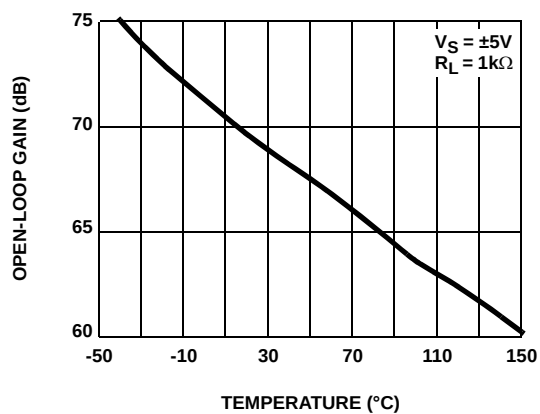


FIGURE 7. OPEN-LOOP GAIN vs TEMPERATURE

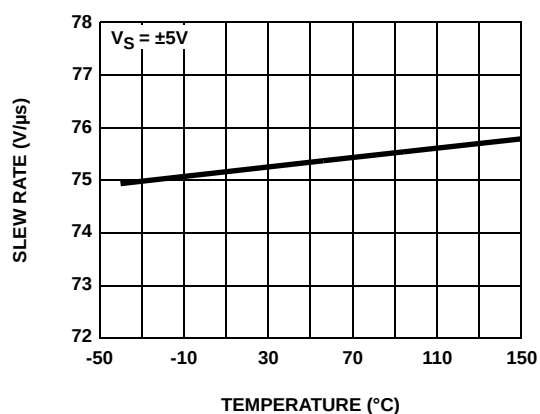


FIGURE 8. SLEW RATE vs TEMPERATURE

Typical Performance Curves (Continued)

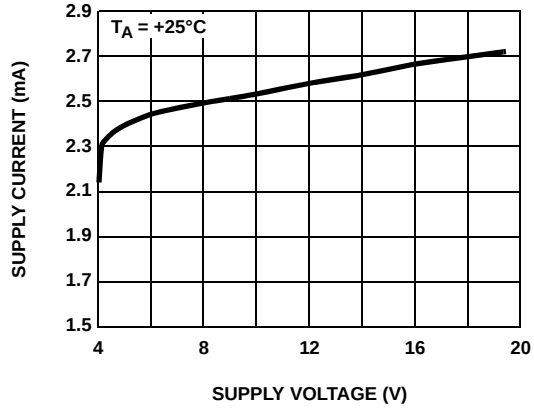


FIGURE 9. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

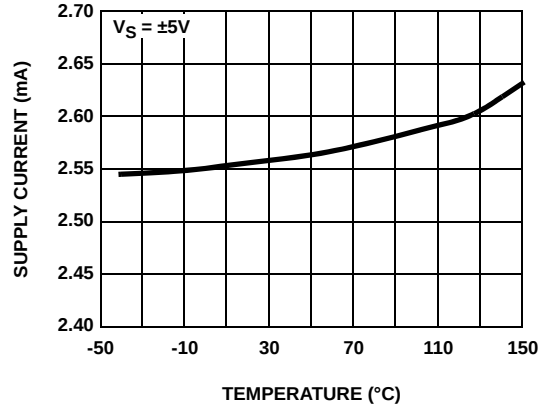


FIGURE 10. SUPPLY CURRENT PER AMPLIFIER vs TEMPERATURE

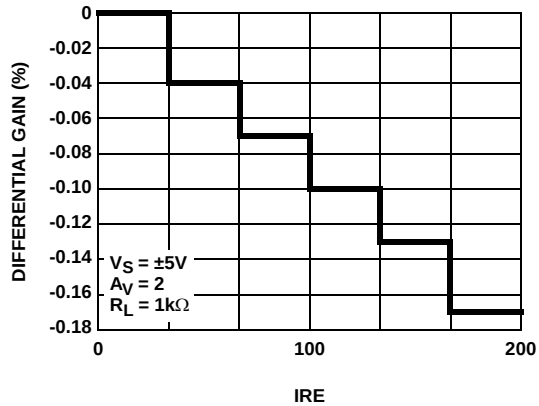


FIGURE 11. DIFFERENTIAL GAIN

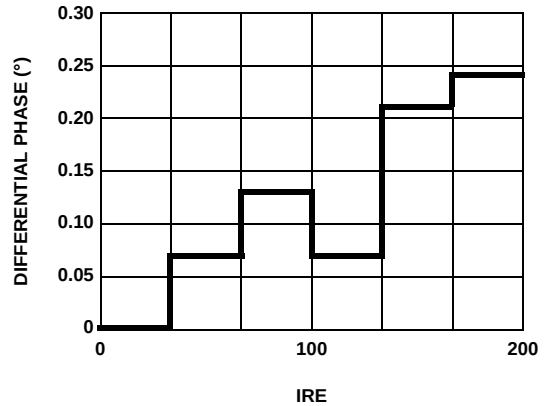


FIGURE 12. DIFFERENTIAL PHASE

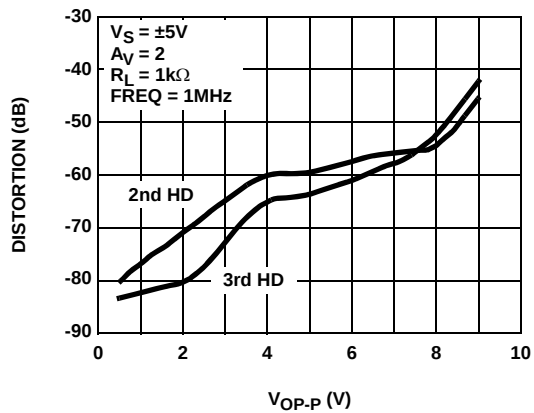


FIGURE 13. HARMONIC DISTORTION vs V_{OP-P}

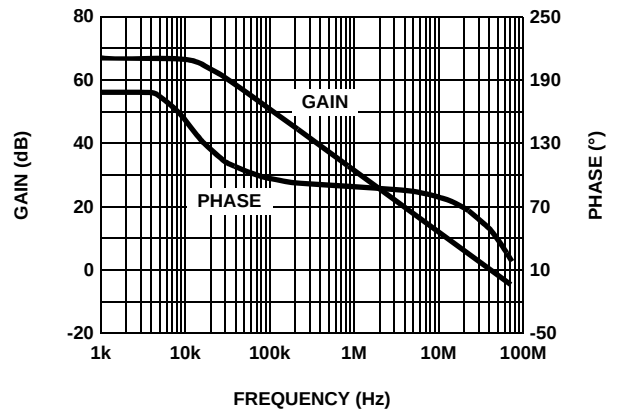


FIGURE 14. OPEN LOOP GAIN AND PHASE

Typical Performance Curves (Continued)

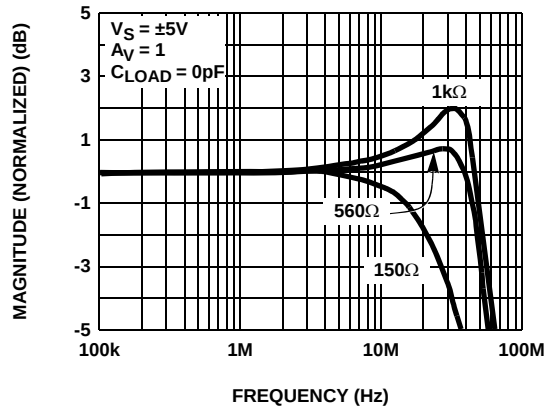
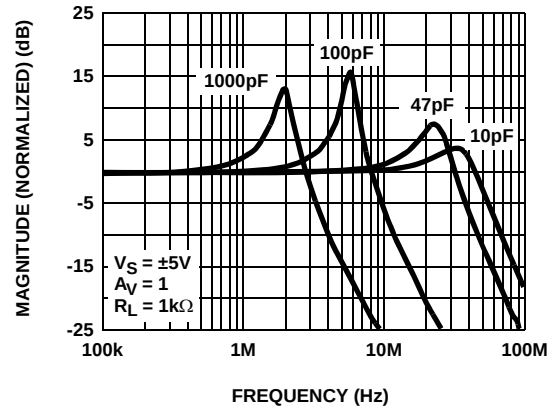
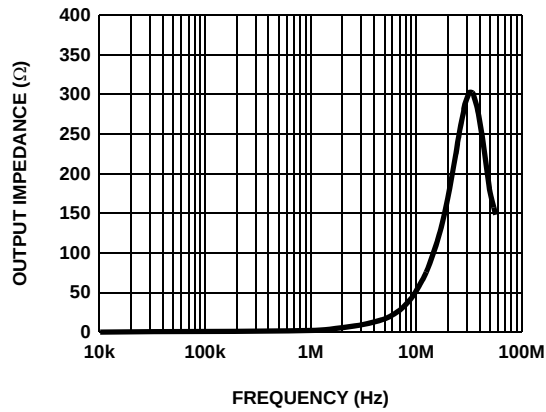
FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS R_L FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS C_L 

FIGURE 17. CLOSED LOOP OUTPUT IMPEDANCE

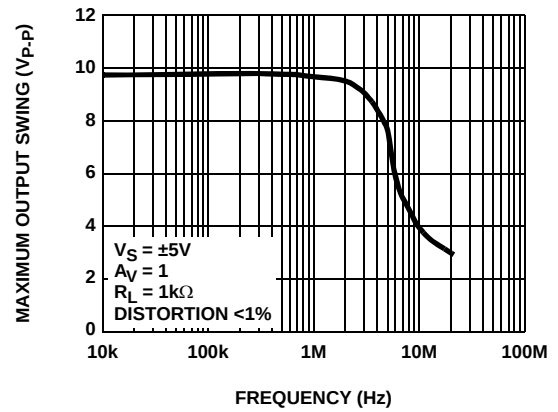


FIGURE 18. MAXIMUM OUTPUT SWING vs FREQUENCY

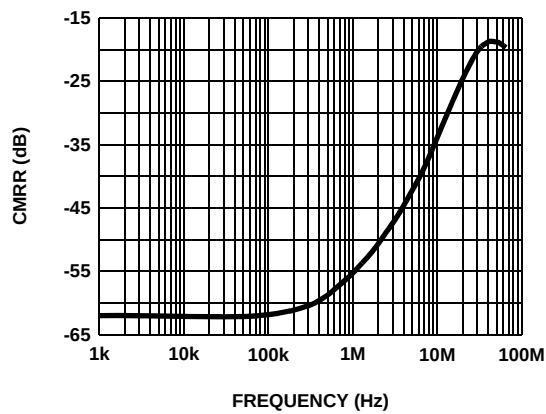


FIGURE 19. CMRR

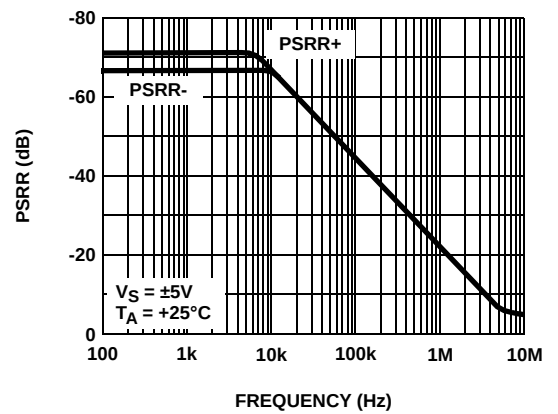


FIGURE 20. PSRR

Typical Performance Curves (Continued)

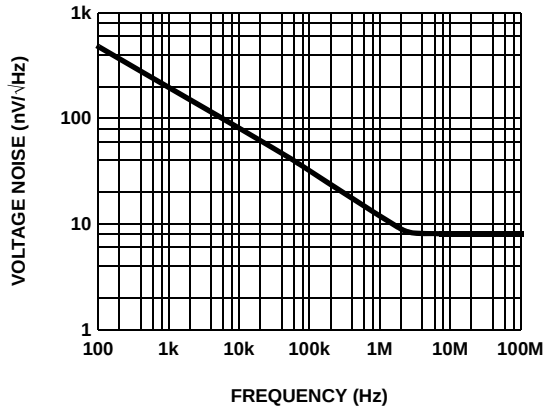


FIGURE 21. INPUT VOLTAGE NOISE SPECTRAL DENSITY

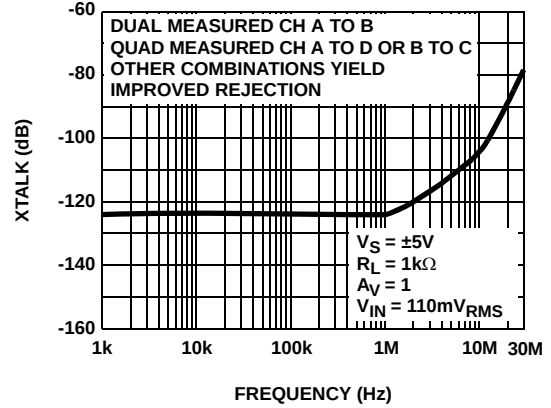


FIGURE 22. CHANNEL SEPARATION

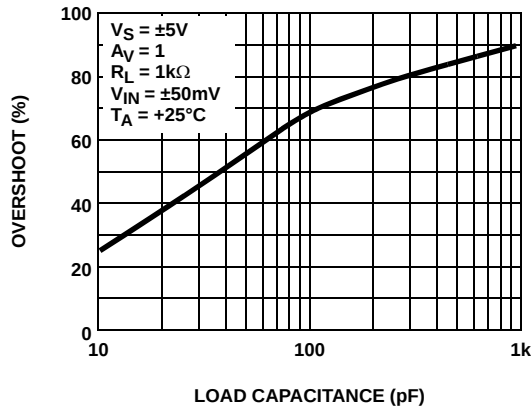


FIGURE 23. SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

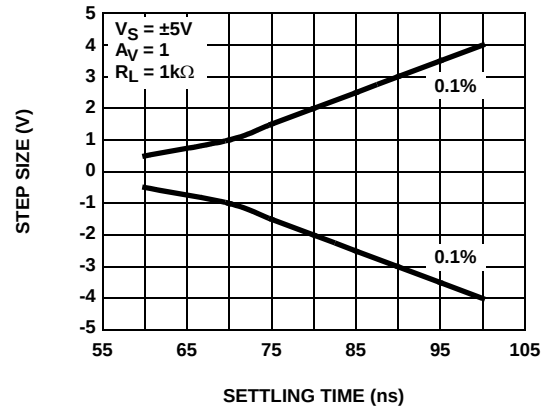


FIGURE 24. SETTLING TIME vs STEP SIZE

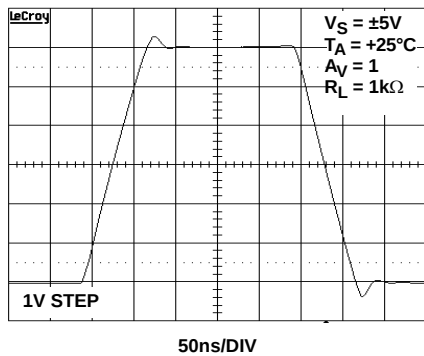


FIGURE 25. LARGE SIGNAL TRANSIENT RESPONSE

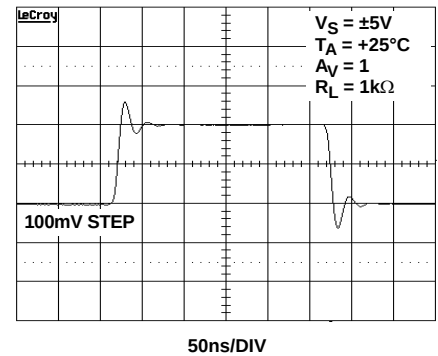


FIGURE 26. SMALL SIGNAL TRANSIENT RESPONSE

PIN NUMBER	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VOUTA	Amplifier A output	CIRCUIT 1
2	VINA-	Amplifier A inverting input	CIRCUIT 2
3	VINA+	Amplifier A non-inverting input	(Reference Circuit 2)
4	VS-	Negative power supply	
5	VINB+	Amplifier B non-inverting input	(Reference Circuit 2)
6	VINB-	Amplifier B inverting input	(Reference Circuit 2)
7	VOUTB	Amplifier B output	(Reference Circuit 1)
8	VS+	Positive power supply	

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Output Phase Reversal

The EL5211A is immune to phase reversal as long as the input voltage is limited from $V_S - 0.5V$ to $V_S + 0.5V$. Figure 28 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

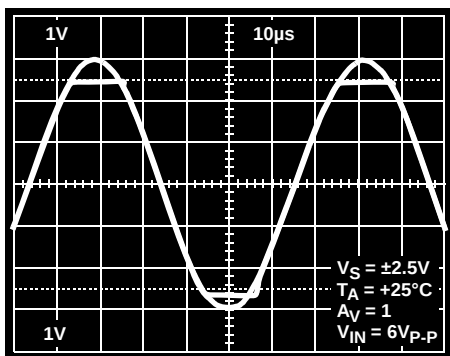


FIGURE 28. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the EL5211A amplifier, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad (EQ. 1)$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \sum i[V_S \times I_{SMAX} + (V_S^+ - V_{OUTi}) \times I_{LOADi}] \quad (EQ. 2)$$

when sourcing, and:

$$P_{DMAX} = \sum i[V_S \times I_{SMAX} + (V_{OUTi} - V_S^-) \times I_{LOADi}] \quad (EQ. 3)$$

when sinking,

where:

- $i = 1$ to 2 for dual and 1 to 4 for quad
- V_S = Total supply voltage
- I_{SMAX} = Maximum supply current per amplifier
- V_{OUTi} = Maximum output voltage of the application
- I_{LOADi} = Load current

If we set the two P_{DMAX} equations equal to each other, we can solve for R_{LOADi} to avoid device overheat. Figures 29 and 30 provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the Equation 3, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves. To ensure proper operation, it is important to observe the recommended derating curves shown in Figures 29 and 30.

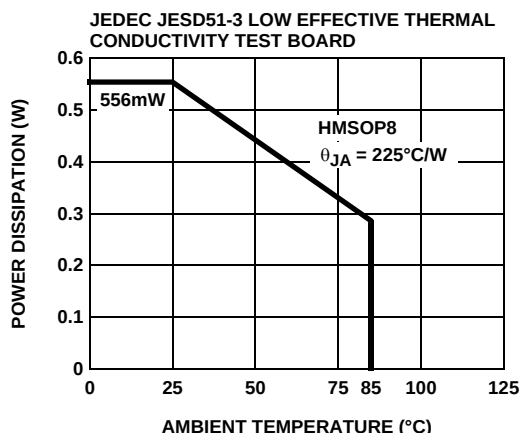


FIGURE 29. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

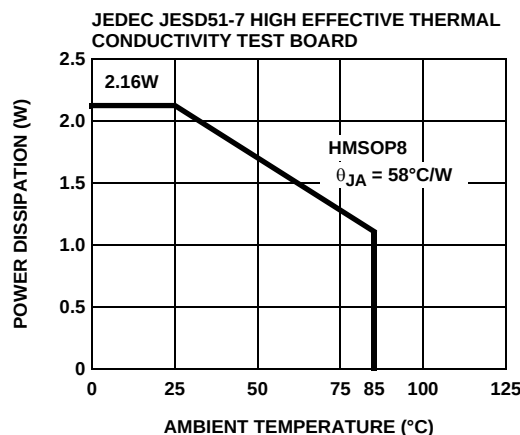


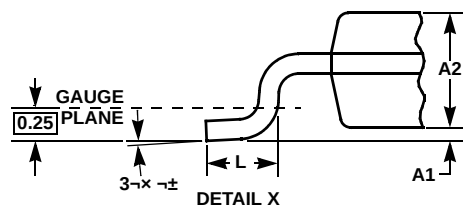
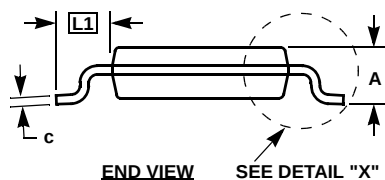
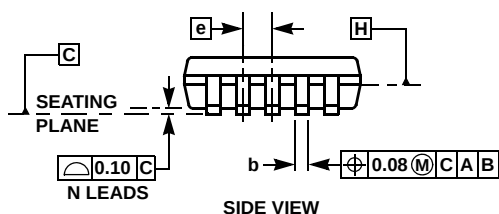
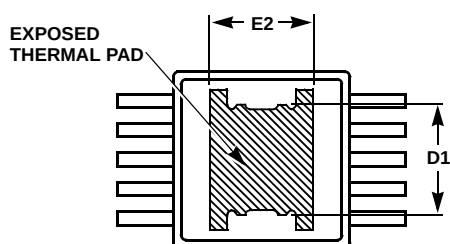
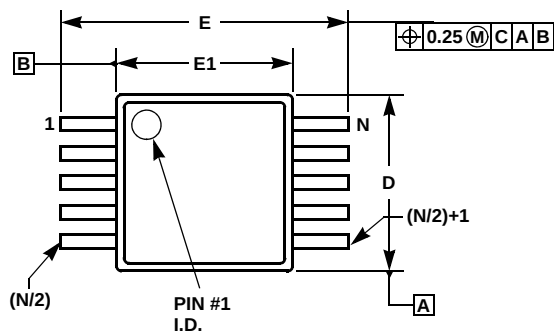
FIGURE 30. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Unused Amplifiers

It is recommended that any unused amplifiers be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground plane.

Power Supply Bypassing and Printed Circuit Board Layout

The EL5211A can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_{S-} pin is connected to ground, a 0.1 μ F ceramic capacitor should be placed from V_{S+} to pin to V_{S-} pin. A 4.7 μ F tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7 μ F capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

HMSOP (Heat-Sink MSOP) Package Family**MDP0050****HMSOP (HEAT-SINK MSOP) PACKAGE FAMILY**

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	HMSOP8	HMSOP10		
A	1.00	1.00	Max.	-
A1	0.075	0.075	+0.025/-0.050	-
A2	0.86	0.86	±0.09	-
b	0.30	0.20	+0.07/-0.08	-
c	0.15	0.15	±0.05	-
D	3.00	3.00	±0.10	1, 3
D1	1.85	1.85	Reference	-
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
E2	1.73	1.73	Reference	-
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

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NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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