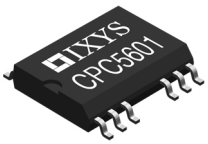
CPC5601 LITELINK™ Family
Auxiliary Programmable Driver IC



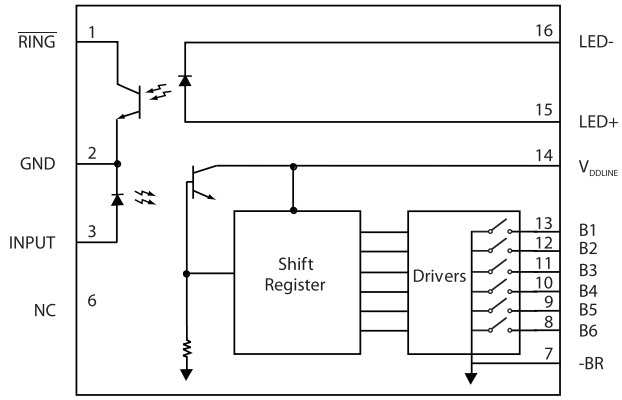
Features
- Meets PC Card (PCMCIA) height requirements
- Zero standby current
- PCB real estate and cost savings
- Can be used with LITELINK II and LITELINK III parts

Compliance
- TIA/EIA/IS-968 (FCC part 68)
- UL1950
- UL60950
- EN/IEC 60950-1 compliant
- EN55022B
- CISPR22B
- EN55024
- TBR-21

Ordering Information

Part Number	Description
CPC5601D	16-pin, 14-lead SOIC, 0.300” wide package, 50/Tube
CPC5601DTR	16-pin, 14-lead SOIC, 0.300” wide package, 1000/Reel

Figure 1. CPC5601 Block Diagram



Description
The CPC5601 is a serially-programmed driver IC for use with IXYS Integrated Circuits Division’s **LITELINK Silicon Data Access Arrangement (DAA) ICs**. The CPC5601 allows host-equipment control of DAA characteristics for worldwide DAA implementations, avoiding multiple implementations with discrete component changes or “stuff” options. The small, low-profile package makes the CPC5601 ideal for 56K PC Card (PCMCIA) modems, PC motherboards, and soft-modems.

The CPC5601 uses opto-electronics to maintain the isolation barrier required in the data access arrangement for connection of host devices to the public switched telephone network (PSTN).

The one-bit serial input of the CPC5601 recovers clocking information from the input signal to set bits in the shift register. The shift register outputs connect to open-drain FET latches that are used to switch in different external components to set V/I slope, DC termination current limit, gain, and AC termination value in LITELINK DAA implementations.The CPC5601 does not need a clock signal for shift register operation, but relies on internal timing instead.

The CPC5601 also includes an opto-coupler for ring detection applications where the AC coupled ring detector of the LITELINK DAA is not used.

1. Specifications

1.1 Absolute Minimum and Maximum Ratings

Parameter	Minimum	Maximum	Unit	Conditions
Isolation Voltage	1500	-	V_{RMS}	From pins 1, 2, and 3 to pins 7 through 16
Operating temperature	0	+85	°C	
Storage temperature	-40	+125	°C	
Soldering temperature	-	+220	°C	

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

1.2 Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit	Conditions
Data Input					
Input high threshold current	-	1	5	mA	
Input low threshold current	0.10	0.20	-	mA	
Input voltage drop	0.9	1.2	1.4	V	I_F = 5 mA
b1 Through b5 Output Driver					
Output Current	-	-	10	mA	
Output Breakdown Voltage	-	-	6	V	
On Resistance	-	10	11	Ω	Supply voltage >= 2.8 V
b6 Output Driver					
Output Current	-	-	120	mA	
Output Breakdown Voltage	-	-	6	V	
On Resistance	-	0.5	1.4	Ω	Supply voltage >= 2.8 V
Ring Detect Input					
Input Control Current	6	20	100	mA	I_C = 2 mA, V_{CE} = 0.5 V
Input Voltage drop	0.9	1.2	1.4	V	I_F = 5 mA
Ring Detect Output					
Blocking Voltage	20	50	-	V	I_C = 10 mA
Dark Current	-	50	500	nA	I_F = 0 mA
Saturation Voltage	-	0.3	0.5	V	I_C = 2 mA, I_F = 16 mA
Current transfer ratio	33	400	-	%	I_F = 6 mA, V_{CE} = 0.5 V
Power Requirements					
Supply Voltage	2.5	3.5	5.5	V	
Total supply current (input current low)	-	0.01	1	µA	
Total supply current (input current high)	-	10	20	µA	

Specifications subject to change without notice. All performance characteristics based on the use of IXYS Integrated Circuits Division application circuits. Functional operation of the device at conditions beyond those specified here is not implied. Specification conditions: V_{DD} = 5V, temperature = 25 °C, unless otherwise indicated.

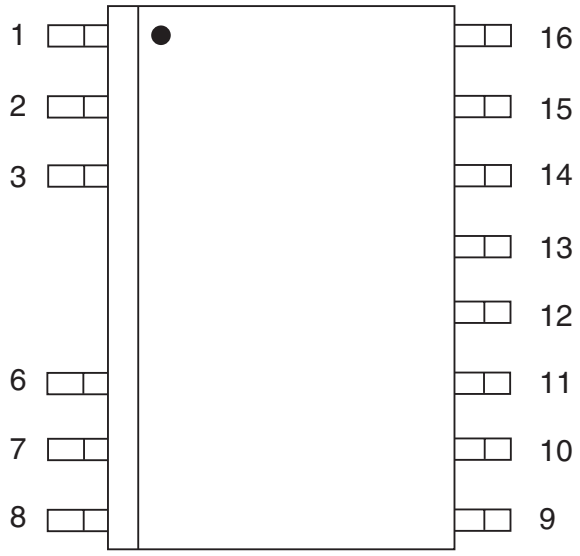
1.3 Timing Characteristics

Parameter	Minimum	Typical	Maximum	Unit	Conditions
Setup time	50	-	-	µS	logic low before positive timing transition on input (pin 3)
Data hold time	60	-	-	µS	hold time after internal 140 µS clock period
Data latch time	-	-	140	µS	from positive transition on input
Input hold time for output on	200	-	-	µS	
Input hold time for output off	-	-	50	µS	

1.4 Pinout

Pin	Name	Function
1	$\overline{\text{RING}}$	Opto-isolated ring output
2	GND	Analog host system ground
3	INPUT	Serial data input used to program outputs b1 through b6.
4	NC	No connection
5	NC	No connection
6	NC	No connection
7	BR-	Phone line side common
8	B6	Output b6
9	B5	Output b5
10	B4	Output b4
11	B3	Output b3
12	B2	Output b2
13	B1	Output b1
14	V_{DDLINE}	Telephone line side voltage source
15	LED+	Ring LED anode
16	LED-	Ring LED cathode

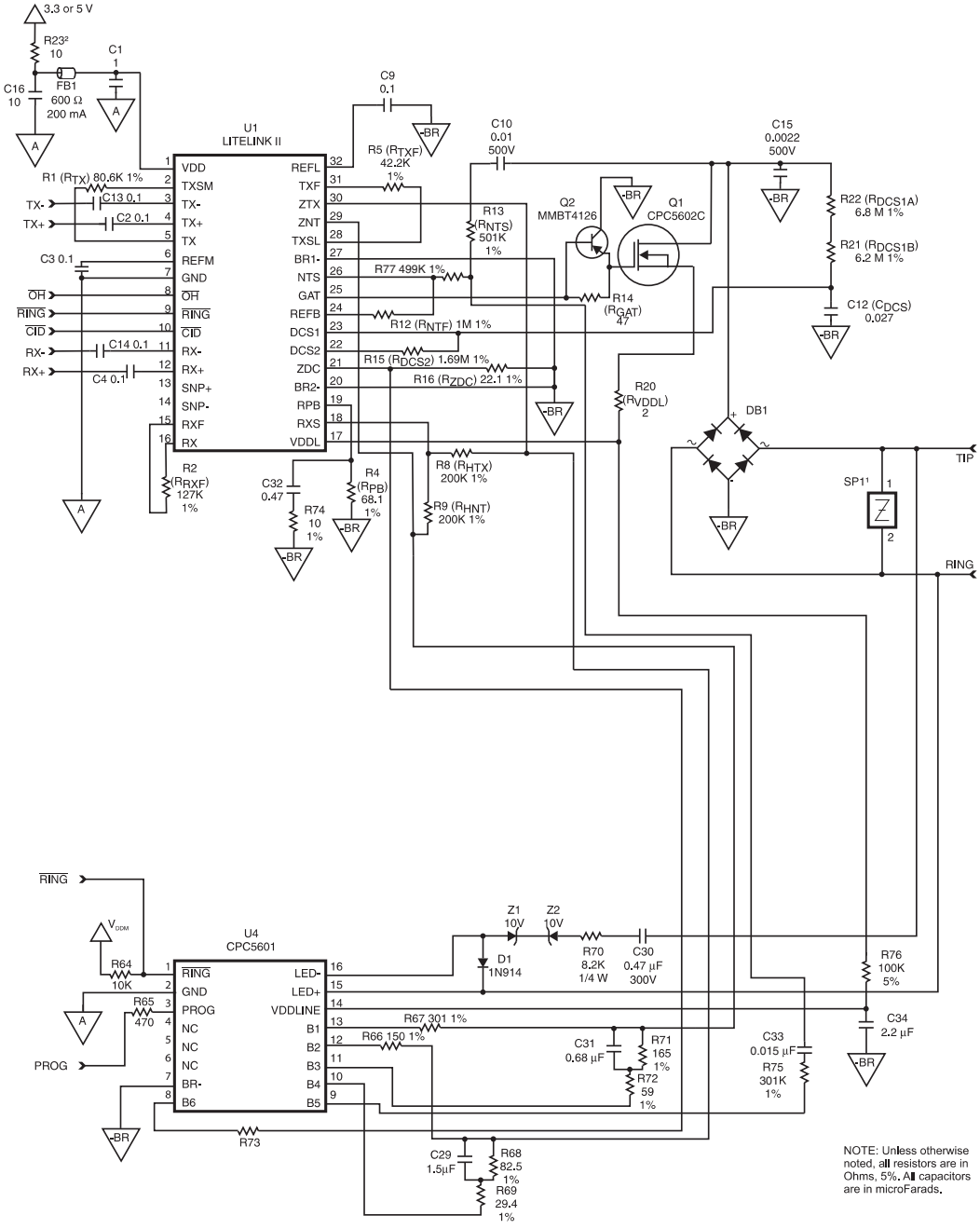
Figure 2. CPC5601 Pinout



2. Application

In the application circuits shown below, the CPC5601 is used to switch AC termination and gain. Loop-current limit switching is optional.

Figure 3. CPC5601 Application Circuit Using the LITELINK II and the Optical Snoop Circuit

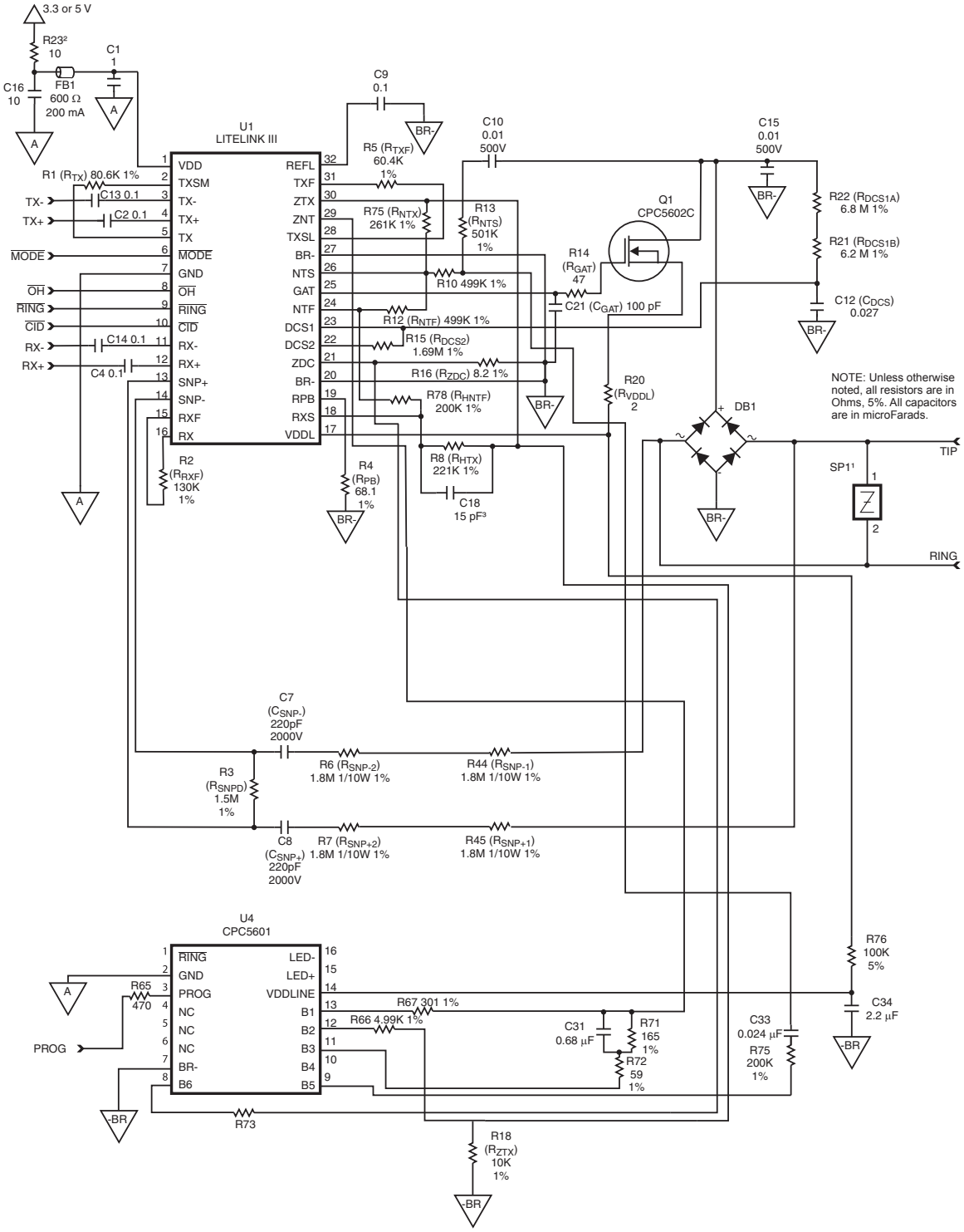


¹This design was tested and found to comply with FCC part 68 with this part. Other compliance requirements may require a different part.

*²Higher noise power supplies may require substitution of a 220 µH inductor, Toko 380HB-2215 or similar. See the power quality section of Clare application note AN-146, **Guidelines for Effective LITELINK Designs** for more information. Both application circuits use the same components for setting AC termination and the telephone line current limit.*

³Addition of this capacitor improves trans-hybrid loss.

Figure 4. CPC5601 Application Circuit Using the LITELINK III and the LITELINK Snoop Circuit



¹This design was tested and found to comply with FCC part 68 with this part. Other compliance requirements may require a different part.

*²Higher noise power supplies may require substitution of a 220 µH inductor, Toko 380HB-2215 or similar. See the power quality section of Clare application note AN-146, **Guidelines for Effective LITELINK Designs** for more information. Both application circuits use the same components for setting AC termination and the telephone line current limit.*

³Addition of this capacitor improves trans-hybrid loss.

2.1 Application Circuit Configurations

Figure 4 shows LITELINK II in circuit designed to use the optical snoop circuit in the CPC5601 for ring detection. Figure 5 shows LITELINK III in a circuit that uses the LITELINK snoop circuit ring detection and display feature (caller ID) signal processing. Note that either generation of LITELINK can be used with either signal monitoring scheme. Using the optical path on the CPC5601 for ring detect precludes on-hook display feature signal processing.

2.2 AC Termination

2.2.1 LITELINK II

The networks connected to outputs b1, b2, b3 and b4 provide selectable telephone line AC termination depending on which network is switched in place of R_{ZNT} (see the appropriate **LITELINK** data sheet and the application note **Understanding LITELINK** for more information).

In North American applications, turn outputs b1 and b2 on, and turn outputs b3 and b4 off to switch in the required 600 Ω AC termination. For European applications, turn outputs b1 and b2 off, and outputs b3 and b4 on to switch in the complex AC termination network.

2.2.2 LITELINK III

The networks connected to outputs b1 and b3 provide selectable telephone line AC termination depending on which network is switched in place of R_{ZNT} (see the appropriate **LITELINK** data sheet and the application note **Understanding LITELINK** for more information). The resistor connected to output b2 provides the required bias current for North American applications.

In North American applications, turn outputs b1 and b2 on, and turn output b3 off to switch in the required 600 Ω AC termination. For European applications, turn outputs b1 and b2 off, and output b3 on to switch in the complex AC termination network.

2.3 LITELINK III Gain

Turning output 5 on adds attenuation to the receive path, which is required for the complex termination. Asserting the $\overline{\text{MODE}}$ pin on LITELINK III corrects for the added attenuation.

2.4 Current Limiting

Clare recommends using the default value for RZDC to set the loop-current limit to 133 mA. You can, if required, adjust the current limit level by adding R73 and using output b6 to switch this value in parallel with RZDC. See the appropriate LITELINK datasheet for more information on setting loop-current limits.

2.5 Figure 3. Part List

Qty.	Reference	Value	Suppliers
1	U1	CPC561x LITELINK II	
1	U4	CPC5601 Auxiliary Programmable Driver	IXYS Integrated Circuits Division
1	Q1	CPC5602C N-Channel Depletion-Mode FET	
1	Q2	MMBT4126 PNP bipolar transistor	Fairchild
1	DB1	S1ZB60 or DB104 Bridge Rectifier	Sindengen Co., Diodes, Inc.
1	D1	1N914	
2	Z1, Z2	10V Zener Diode	
1	SP1	P3100SB Sidactor	Teccor, TI, ST Microelectronics
1	FB1	600 Ω, 200 mA ferrite bead	Murata BLM11A601S or similar
1	C1	1 µF, 16 V, ± 10%	
6	C2, C3, C4, C9, C13, C14	0.1 µF, 16 V, ± 10%	
1	C10	0.01 µF, 500 V, ± 10%[1]	
1	C12	0.027 µF, 16 V, ± 10%	
1	C15	0.0022 µF, 500 V, ± 10%[1]	
1	C16	10 µF, 16 V, ± 10%	Panasonic, AVX, Novacap, Murata, SMEC
1	C29	1.5 µF, 16 V, ± 10%	
1	C30	0.47 µF, 300 V, ± 10%	
1	C31	0.68 µF, 16 V, ± 10%	
1	C32	0.47 µF, 16 V, ± 10%	
1	C33	0.015 µF, 16 V, ± 10%	
1	C34	2.2 µF, 16 V, ± 10%	
1	R1	80.6 KΩ, 1/16W, ± 1%	
1	R2	127 KΩ, 1/16W, ± 1%	
1	R4	68.1 Ω, 1/16W, ± 1%	
1	R5	42.2 KΩ, 1/16W, ± 1%	
2	R8, R9	200 KΩ, 1/16W, ± 1%	
1	R13	501 KΩ, 1/16W, ± 1%	
1	R14	47 Ω, 1/16W, ± 1%	
1	R15	1.69 MΩ, 1/16W, ± 1%	
1	R20	2 Ω, 1/16W, ± 1%	
1	R21	6.2 MΩ, 1/4W, ± 1%	
1	R22	6.8 MΩ, 1/4W, ± 1%	
1	R23	10 Ω, 1/16W, ± 5% or 220 µH inductor	
1	R64	10 kΩ, 1/16W, ± 5%	Panasonic, Electro Films, FMI, Vishay, etc.
1	R65	470 Ω, 1/16W, ± 5%	
1	R66	150 Ω, 1/16W, ± 1%	
1	R67	301 Ω, 1/16W, ± 1%	
1	R68	82.5 Ω, 1/16W, ± 1%	
1	R69	29.4 Ω, 1/16W, ± 1%	
1	R70	8.2 kΩ, 1/4W, ± 5%	
1	R71	165 Ω, 1/16W, ± 1%	
1	R72	59 Ω, 1/16W, ± 1%	
1	R73	optional, see text	
1	R74	10 Ω, 1/16W, ± 1%	
1	R75	402 kΩ, 1/16W, ± 1%	
1	R76	100 kΩ, 1/16W, ± 5%	
1	R77	499 kΩ, 1/16W, ± 1%	

2.6 Figure 4. Part List

Qty.	Reference	Value	Suppliers
1	U1	CPC562x LITELINK III	IXYS Integrated Circuits Division
1	U4	CPC5601 Auxiliary Programmable Driver	
1	Q1	CPC5602C N-Channel Depletion-Mode FET	
1	DB1	S1ZB60 or DB104 Bridge Rectifier	Sindengen Co., Diodes, Inc.
1	SP1	P3100SB Sidactor	Teccor, TI, ST Microelectronics
1	FB1	600 Ω, 200 mA ferrite bead	Murata BLM11A601S or similar
1	C1	1 µF, 16 V, ± 10%	Panasonic, AVX, Novacap, Murata, SMEC
4	C2, C9, C13, C14	0.1 µF, 16 V, ± 10%	
2	C7, C8	220 pF, 2 kV, ±5%[1]	
2	C10, C15	0.01 µF, 500 V, ± 10%[1]	
1	C12	0.027 µF, 16 V, ± 10%	
1	C15	0.0022 µF, 500 V, ± 10%[1]	
1	C16	10 µF, 16 V, ± 10%	
1	C18	15 pF, 50 V, ± 10%	
1	C21	100 pF, 50 V, ± 10%	
1	C29	1.5 µF, 16 V, ± 10%	
1	C30	0.47 µF, 300 V, ± 10%	
1	C31	0.68 µF, 16 V, ± 10%	
1	C32	0.47 µF, 16 V, ± 10%	
1	C33	0.024 µF, 16 V, ± 10%	
1	C34	2.2 µF, 16 V, ± 10%	
1	R1	80.6 KΩ, 1/16W, ± 1%	Panasonic, Electro Films, FMI, Vishay, etc.
1	R2	130 KΩ, 1/16W, ± 1%	
1	R3	1.5 MΩ, 1/16W, ± 1%	
1	R4	68.1 Ω, 1/16W, ± 1%	
1	R5	60.4 KΩ, 1/16W, ± 1%	
4	R6, R7, R44, R45	1.8 MΩ, 1/10W, ± 1%	
1	R8	221 KΩ, 1/16W, ± 1%	
2	R10, R12	499 KΩ, 1/16W, ± 1%	
1	R13	501 KΩ, 1/16W, ± 1%	
1	R14	47 Ω, 1/16W, ± 1%	
1	R15	1.69 MΩ, 1/16W, ± 1%	
1	R16	8.2 Ω, 1/16W, ± 1%	
1	R18	10 KΩ, 1/16W, ± 1%	
1	R20	2 Ω, 1/16W, ± 1%	
1	R21	6.2 MΩ, 1/4W, ± 1%	
1	R22	6.8 MΩ, 1/4W, ± 1%	
1	R23	10 Ω, 1/16W, ± 5% or 220 µH inductor	
1	R64	10 kΩ, 1/16W, ± 5%	
1	R65	470 Ω, 1/16W, ± 5%	
1	R66	150 Ω, 1/16W, ± 1%	
1	R67	301 Ω, 1/16W, ± 1%	
1	R71	165 Ω, 1/16W, ± 1%	
1	R72	59 Ω, 1/16W, ± 1%	
1	R73	optional, see text	
1	R75	402 kΩ, 1/16W, ± 1%	
1	R76	100 kΩ, 1/16W, ± 5%	
1	R77	499 kΩ, 1/16W, ± 1%	
1	R78	200 kΩ, 1/16W, ± 1%	

2.7 Operational Sequence

In the application circuits above, the CPC5601 is powered from the telephone line only when the LITELINK is off-hook. This requires that you set the telephone line characteristics controlled by the CPC5601 under host system control immediately after taking the DAA off-hook or after pulse dialing is complete, using the following sequence:

1. For incoming calls, validate a ring signal by having the host system poll or read the output of $\overline{\text{RING}}$ (ring detect via snoop circuit on the LITELINK) or $\overline{\text{RING}}$ (ring detect via opto-isolated ring circuit in the CPC5601).
2. Assert $\overline{\text{OH}}$ to complete the connection.
3. Set the telephone line characteristics of the DAA using the CPC5601 via the programming method (see “Programming” on page 10).

With this circuit, you must program the CPC5601 as soon as possible after asserting off hook. Leaving the CPC5601 unprogrammed leaves open the possibility of LITELINK instability due to lack of AC termination.

2.8 Output Current Ratings

Output b6 is the only output that can be used for the current limiting function of a DAA. The FET on output b6 can sink up to 120 mA of current, while the other outputs can sink up to 10 mA.

The other outputs can be used for any of the other switchable functions on the telephone line side of a DAA, as long as the current does not exceed the 10 mA limit.

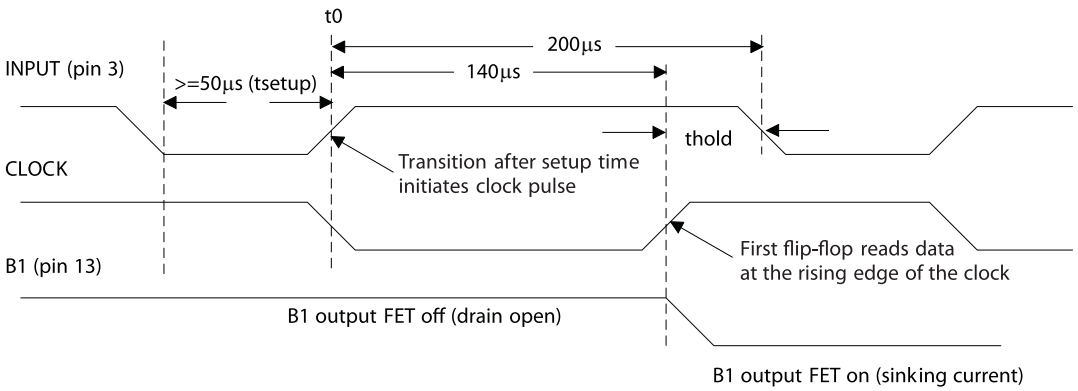
3. Programming

3.1 Latch Circuit Description

Data applied to the input pin is optically coupled to the shift register through a pulse generator. Each low-to-high transition in the pulse generator triggers a clock pulse. Clock pulses are applied to the CLK input of six rising-edge-triggered flip-flops. The non-inverted input data is fed to the flip-flops at all times, but the flip-flops are only clocked on receipt of a pulse from the pulse generator. The flip-flops drive six FET switches.

3.2 Programming Protocol

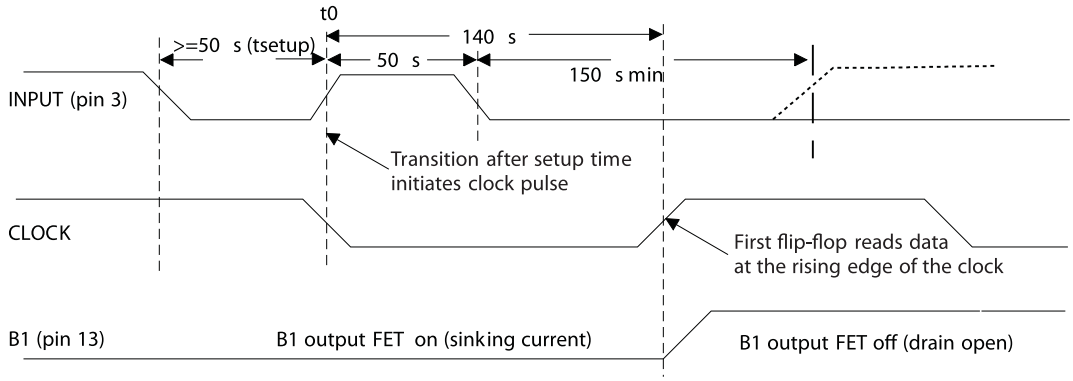
Figure 5. Latch Circuit Timing to Turn an Output On



A setup pulse on the input of at least 50 µS starts the bit programming sequence. The trailing edge of the setup pulse starts a timer on the CPC5601 (t0). After 140 µS, the value of the input is latched into the shift register.

To set an output, hold the input high for 200 µS from the leading edge after the setup pulse. This turns on the corresponding open-drain FET to sink current.

Figure 6. Latch Circuit Timing to Turn an Output Off



To clear an output, hold the input high for 50 µS after the setup pulse, then take the input low for at least 150 µS.

Repeat the sequence of the setup pulse followed by the appropriate input condition for each successive bit.

Bear the following in mind while programming the CPC5601:

- All bits must be set in each programming sequence, even to change just one of the outputs.
- Data is placed in least-significant bit (output 1) first.
- After setting all the bits, take the input low. In the absence of low-to-high transitions on the input, the internal CPC5601 clock is held high, preventing any output changes.
- The CPC5601 does not employ a shift register load function. As new data is shifted into the flip-flops, the outputs (starting with b1) change throughout the data input sequence.

3.3 Programming Example

This programming example sets the following CPC5601 output state, suitable for a European DAA:

3.3.1 LITELINK III

b1 (LSB)	b2	b3	b4	b5	b6 (MSB)
off	off	on	off	on	off

3.3.2 LITELINK II

b1 (LSB)	b2	b3	b4	b5	b6 (MSB)
off	off	on	on	on	off

1. Hold the input low for 50 μS.
2. Set the input high for 50 μS to trigger the timer.
3. Set the input low for 150 μS to set output b1 to off.
4. Repeat the steps as shown in the programming waveform below to program all six outputs to the desired pattern.

Figure 7. LITELINK III European Programming Sample Input Waveform

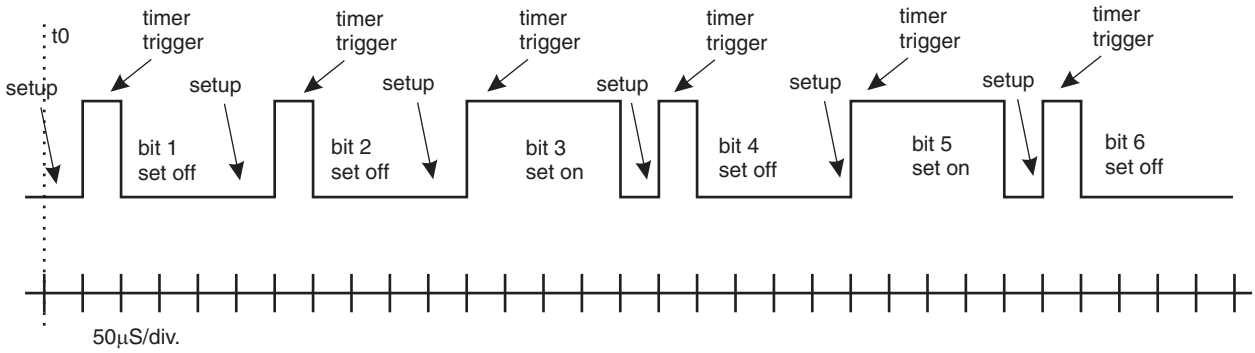
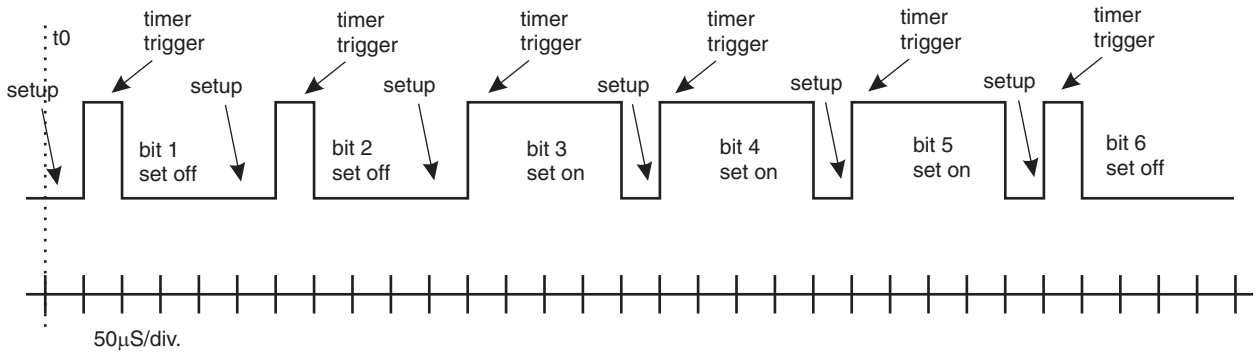


Figure 8. LITELINK II European Programming Sample Input Waveform



4. Regulatory Information

CPC5601 can be used to build products that comply with the requirements of TIA/EIA/IS-968 (formerly FCC part 68), FCC part 15B, TBR-21, EN60950, UL1950, EN55022B, IEC950/IEC60950, CISPR22B, EN55024, and many other standards. CPC5601 complies with the requirements of UL1577. CPC5601 provides supplementary isolation. Metallic surge requirements are met through the inclusion of a Sidactor in the application circuit. Longitudinal surge protection is provided by CPC5601's optical-across-the-barrier technology and the use of high-voltage components in the application circuit as needed.

The information provided in this document is intended to inform the equipment designer but it is not sufficient to assure proper system design or regulatory compliance. Since it is the equipment manufacturer's responsibility to have their equipment properly designed to conform to all relevant regulations, designers using CPC5601 are advised to carefully verify that their end-product design complies with all applicable safety, EMC, and other relevant standards and regulations. Semiconductor components are not rated to withstand electrical overstress or electro-static discharges resulting from inadequate protection measures at the board or system level.

5. LITELINK Design Resources

5.1 Clare Design Resources

The IXYS Integrated Circuits Division web site has a wealth of information useful for designing with LITELINK, including application notes and reference designs that already meet all applicable regulatory requirements. LITELINK data sheets also contains additional application and design information. See the following links:

LITELINK datasheets and reference designs

Application note AN-107 **LOCxx Series - Isolated Amplifier Design Principles**

Application note AN-114 **ITC117P**

Application note AN-117 **Customize Caller-ID Gain and Ring Detect Voltage Threshold for CPC5610/11**

Application note AN-140, **Understanding LITELINK**

Application note AN-141, **Enhanced Pulse Dialing with LITELINK**

Application note AN-143, **Loop Reversal Detection with LITELINK**

Application note AN-146, **Guidelines for Effective LITELINK Designs**

Application note AN-147, **Worldwide Application of LITELINK**

Application note AN-149, **Increased LITELINK II Transmit Power**

Application note AN-150, **Ground-start Supervision Circuit Using IAA110**

5.2 Third Party Design Resources

The following also contain information useful for LITELINK designs. All of the books are available on **amazon.com**.

Understanding Telephone Electronics, Stephen J. Bigelow, et. al., Butterworth-Heinenman; ISBN: 0750671750.

Newton's Telecom Dictionary, Harry Newton, CMP Books; ISBN: 1578200695.

Photodiode Amplifiers: Op Amp Solutions, Jerald Graeme, McGraw-Hill Professional Publishing; ISBN: 007024247X

Teccor, Inc. Surge Protection Products

United States Code of Federal Regulations, CFR 47 Part 68.3.

6. Manufacturing Information

6.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC5601D	MSL 3

6.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

6.3 Reflow Profile

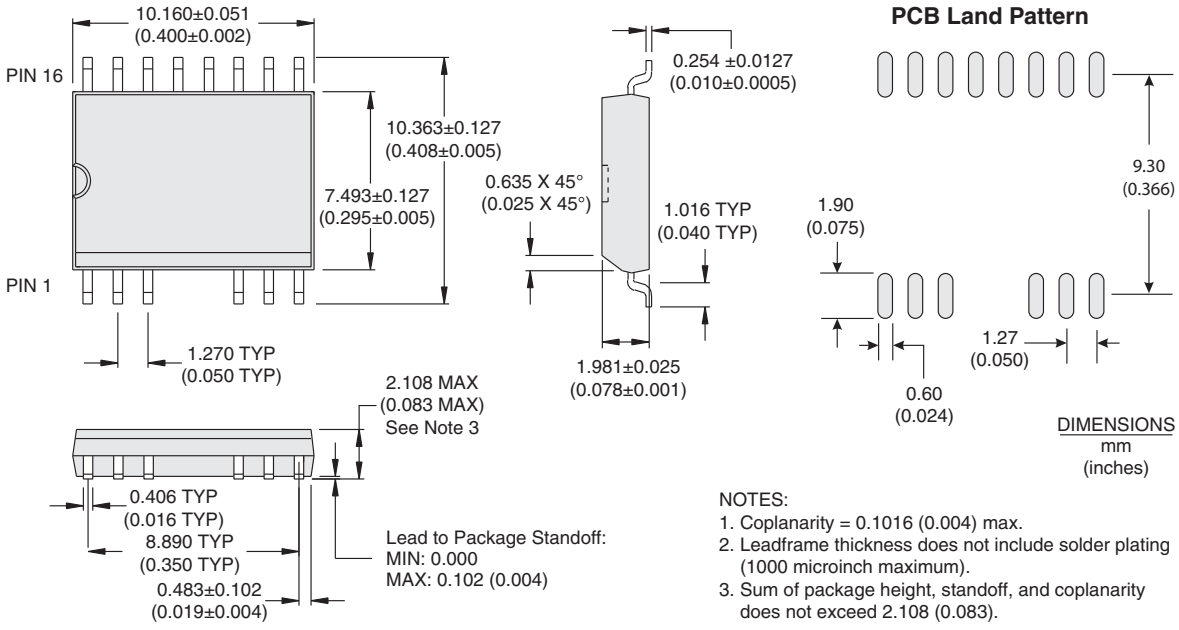
This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC5601D	260°C for 30 seconds

6.4 Board Wash

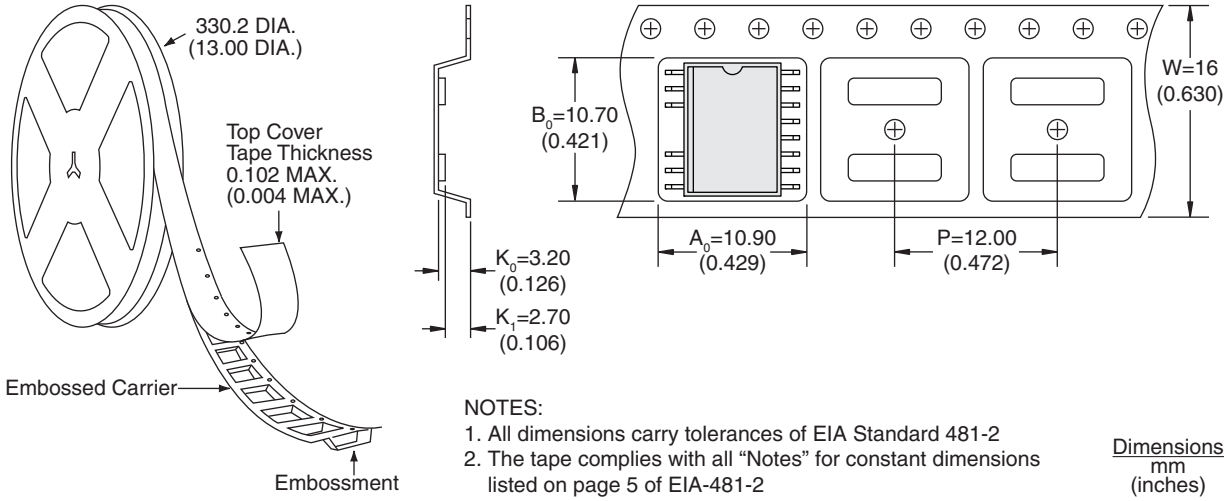
IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

6.5 CPC5601D Package



NOTES:
1. Coplanarity = 0.1016 (0.004) max.
2. Leadframe thickness does not include solder plating (1000 microinch maximum).
3. Sum of package height, standoff, and coplanarity does not exceed 2.108 (0.083).

6.6 CPC5601DTR Tape and Reel Specifications



NOTES:
1. All dimensions carry tolerances of EIA Standard 481-2
2. The tape complies with all “Notes” for constant dimensions listed on page 5 of EIA-481-2

Dimensions
mm
(inches)

For additional information please visit our website at: www.ixysic.com

Specification: DS-CPC5601-R04

12/22/2012