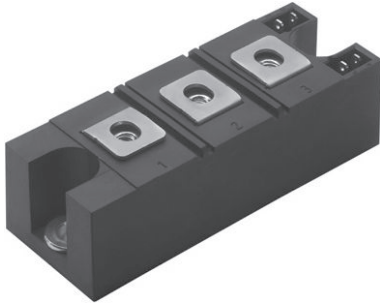



## Thyristor/Thyristor, 150 A (New INT-A-PAK Power Module)



New INT-A-PAK

### FEATURES

- Electrically isolated by DBC ceramic ( $\text{Al}_2\text{O}_3$ )
- 3500  $V_{\text{RMS}}$  isolating voltage
- Industrial standard package
- High surge capability
- Glass passivated chips
- Simple mounting
- UL approved file E78996 
- Designed and qualified for multiple level
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT

### PRODUCT SUMMARY

$I_{\text{T(AV)}}$	150 A
Type	Modules - Thyristor, Standard
Package	INT-A-PAK
Circuit	Two SCRs doubler circuit

### APPLICATIONS

- Battery charges
- Welders
- Power converters

### MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{\text{T(AV)}}$	85 °C	150	A
$I_{\text{T(RMS)}}$		330	A
$I_{\text{TSM}}$	50 Hz	4000	
	60 Hz	4200	
$I^2t$	50 Hz	80	$\text{kA}^2\text{s}$
	60 Hz	73	
$I^2\sqrt{t}$		800	$\text{kA}^2\sqrt{\text{s}}$
$V_{\text{RRM}}$		400	V
$T_{\text{Stg}}$	Range	-40 to 150	°C
$T_{\text{J}}$	Range	-40 to 125	

### ELECTRICAL SPECIFICATIONS

#### VOLTAGE RATINGS

TYPE NUMBER	$V_{\text{RRM}}/V_{\text{DRM}}$ , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	$V_{\text{RSM}}/V_{\text{DSM}}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{\text{RRM}}/I_{\text{DRM}}$ AT 125 °C mA
VS-VSKT152/04PbF	400	500	50



ON-STATE CONDUCTION							
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS	
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction half sine wave			150	A	
					85	°C	
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch			330	A	
Maximum peak, one-cycle on-state, non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reapplied	Sine half wave, initial $T_J$ = $T_J$ maximum	4000		
		t = 8.3 ms			4200		
		t = 10 ms	100 % $V_{RRM}$ reapplied		3350		
		t = 8.3 ms			3500		
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reapplied		80		kA <sup>2</sup> s
		t = 8.3 ms			73		
		t = 10 ms	100 % $V_{RRM}$ reapplied		56		
		t = 8.3 ms			51		
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			800	kA <sup>2</sup> $\sqrt{s}$	
Value of threshold voltage	$V_{T(TO)}$	$T_J$ maximum			0.82	V	
On-state slope resistance	$r_t$				1.44	mΩ	
Maximum on-state voltage drop	$V_{TM}$	$I_{pk} = \pi \times I_{T(AV)}$ , $T_J = 25\text{ °C}$			1.48	V	
Maximum holding current	$I_H$	$T_J = 25\text{ °C}$ , anode supply = 6 V, resistive load, gate open circuit			200	mA	
Maximum latching current	$I_L$	$T_J = 25\text{ °C}$ , anode supply = 6 V, resistive load			400		

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Typical delay time	$t_{gd}$	$T_J = 25\text{ }^{\circ}\text{C}$	Gate current = 1 A, $di_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\text{ \% }V_{\text{DRM}}$	1	$\mu\text{s}$
Typical rise time	$t_{gr}$			2	
Typical turn-off time	$t_q$	$I_{\text{TM}} = 300\text{ A}$ , $-di/dt = 15\text{ A}/\mu\text{s}$ ; $T_J = T_J$ maximum $V_R = 50\text{ V}$ ; $dV/dt = 20\text{ V}/\mu\text{s}$ ; gate 0 V, 100 $\Omega$		50 to 200	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = 125\text{ }^{\circ}\text{C}$	50	mA
RMS insulation voltage	$V_{INS}$	50 Hz, circuit to base, all terminals shorted, t = 1 s	3500	V
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, exponential to 67 % rated $V_{DRM}$	1000	V/μs



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum peak gate power	P <sub>GM</sub>	t <sub>p</sub> ≤ 5 ms, T <sub>J</sub> = T <sub>J</sub> maximum		12	W	
Maximum average gate power	P <sub>G(AV)</sub>	f = 50 Hz, T <sub>J</sub> = T <sub>J</sub> maximum		3		
Maximum peak gate current	I <sub>GM</sub>	t <sub>p</sub> ≤ 5 ms, T <sub>J</sub> = T <sub>J</sub> maximum		3	A	
Maximum peak negative gate voltage	- V <sub>GT</sub>			10	V	
Maximum required DC gate voltage to trigger	V <sub>GT</sub>	T <sub>J</sub> = - 40 °C	Anode supply = 6 V, resistive load; R <sub>a</sub> = 1 Ω	4		
		T <sub>J</sub> = 25 °C		2.5		
		T <sub>J</sub> = T <sub>J</sub> maximum		1.7		
Maximum required DC gate current to trigger	I <sub>GT</sub>	T <sub>J</sub> = - 40 °C		270	mA	
		T <sub>J</sub> = 25 °C		150		
		T <sub>J</sub> = T <sub>J</sub> maximum		80		
Maximum gate voltage that will not trigger	V <sub>GD</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, rated V <sub>DRM</sub> applied		0.3	V	
Maximum gate current that will not trigger	I <sub>GD</sub>			10	mA	
Maximum rate of rise of turned-on current	di/dt	T <sub>J</sub> = T <sub>J</sub> maximum, I <sub>TM</sub> = 400 A rated V <sub>DRM</sub> applied		300	A/μs	

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range		T <sub>J</sub>		- 40 to 125	°C
Maximum storage temperature range		T <sub>Stg</sub>		- 40 to 150	
Maximum thermal resistance, junction to case per junction		R <sub>thJC</sub>	DC operation	0.18	K/W
Maximum thermal resistance, case to heatsink per module		R <sub>thCS</sub>	Mounting surface smooth, flat and greased	0.05	
Mounting torque ± 10 %	IAP to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	4 to 6	Nm
	busbar to IAP				
Approximate weight				200	g
				7.1	oz.
Case style				INT-A-PAK	

$\Delta R$ CONDUCTION PER JUNCTION											
DEVICES	SINUSOIDAL CONDUCTION AT T <sub>J</sub> MAXIMUM					RECTANGULAR CONDUCTION AT T <sub>J</sub> MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSKT152/04PbF	0.007	0.010	0.013	0.016	0.017	0.009	0.012	0.014	0.016	0.017	K/W

**Note**

- Table shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC

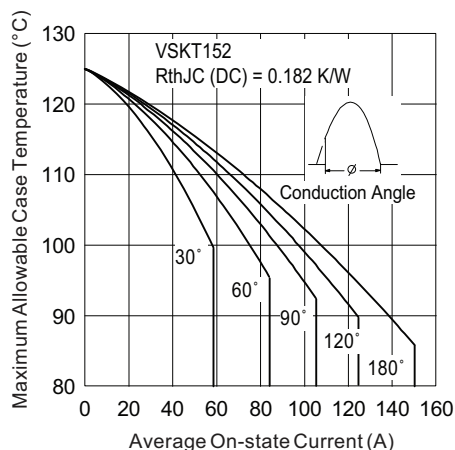


Fig. 1 - Current Ratings Characteristics

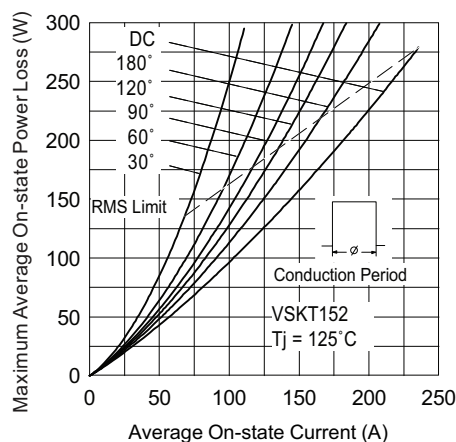


Fig. 4 - Forward Power Loss Characteristics

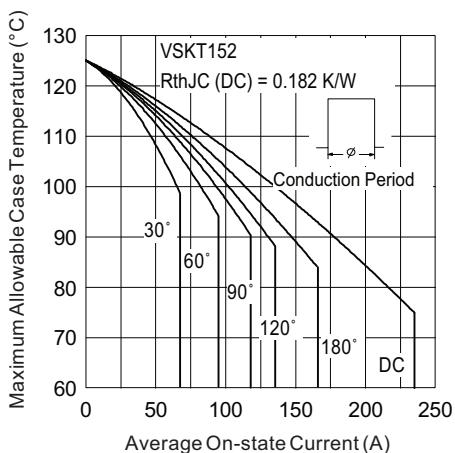


Fig. 2 - Current Ratings Characteristics

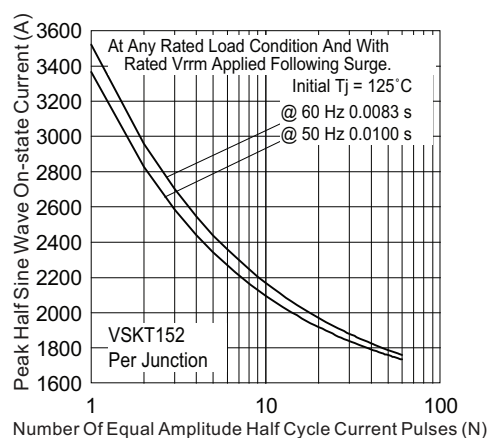


Fig. 5 - Maximum Non-Repetitive Surge Current

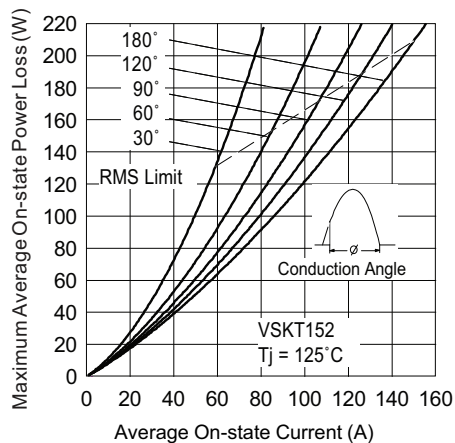


Fig. 3 - Forward Power Loss Characteristics

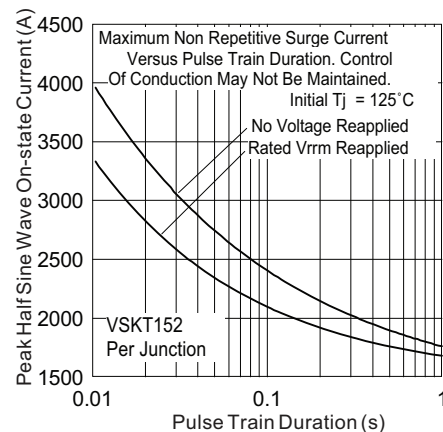


Fig. 6 - Maximum Non-Repetitive Surge Current

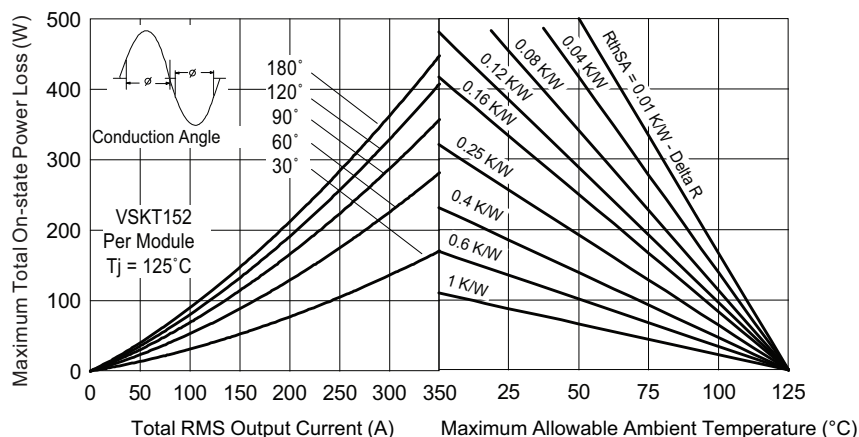


Fig. 7 - On-State Power Loss Characteristics

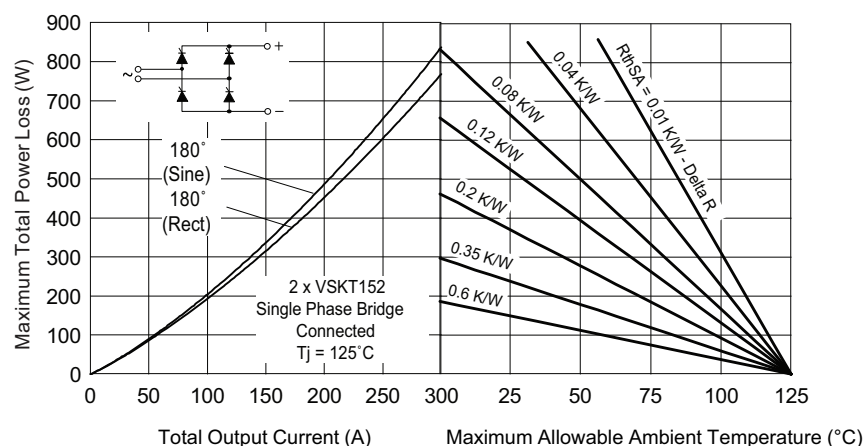


Fig. 8 - On-State Power Loss Characteristics

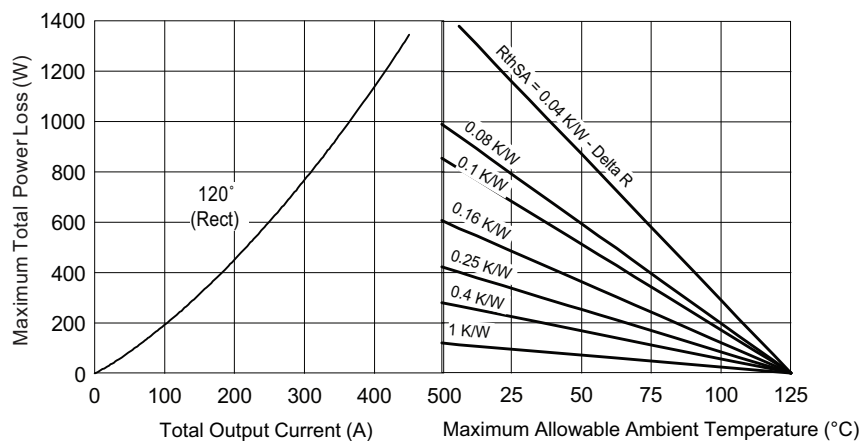


Fig. 9 - On-State Power Loss Characteristics

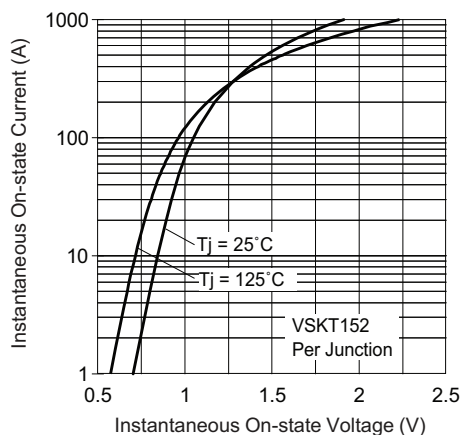


Fig. 10 - On-State Voltage Drop Characteristics

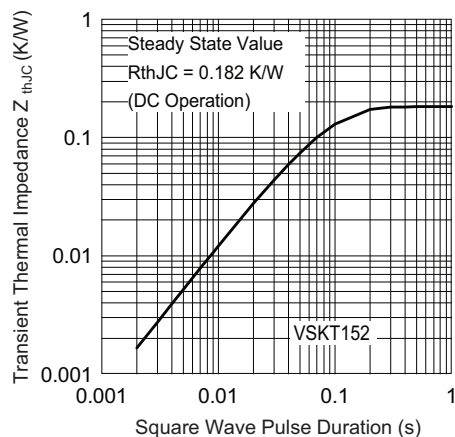
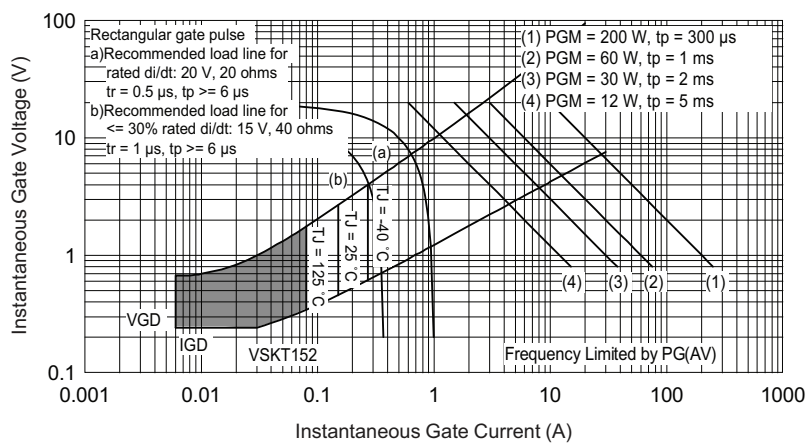

Fig. 11 - Thermal Impedance  $Z_{thJC}$  Characteristics


Fig. 12 - Gate Characteristics



**ORDERING INFORMATION TABLE**

Device code	VS-VS	KT	152	04	PbF
	1	2	3	4	5
1	- Vishay Semiconductors product				
2	- Circuit configuration				
3	- Current rating				
4	- Voltage rating (04 = 400 V)				
5	- PbF = Lead (Pb)-free				

**Note**

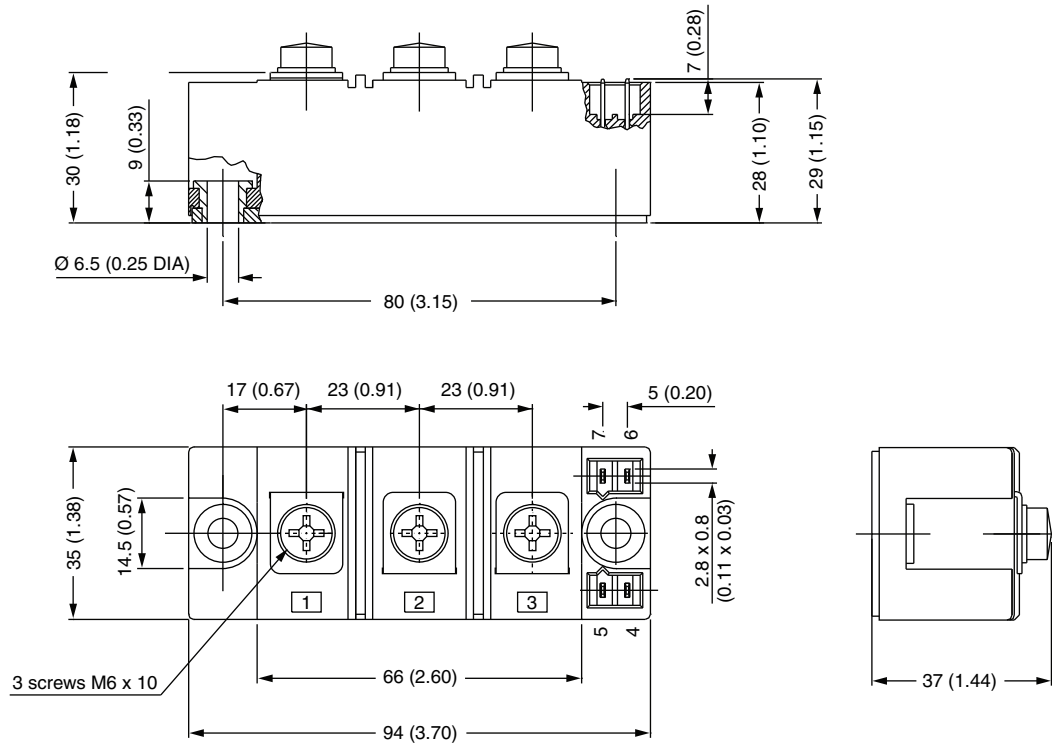
- To order the optional hardware go to [www.vishay.com/doc?95172](http://www.vishay.com/doc?95172)

CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs doubler circuit	T	

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95067">www.vishay.com/doc?95067</a>

## INT-A-PAK IGBT/Thyristor

**DIMENSIONS** in millimeters (inches)







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