

16-Channel Wideband Video Multiplexers

DESCRIPTION

The DG535/536 are 16-channel multiplexers designed for routing one of 16 wideband analog or digital input signals to a single output. They feature low input and output capacitance, low on-resistance, and n-channel DMOS "T" switches, resulting in wide bandwidth, low crosstalk and high "off" isolation. In the on state, the switches pass signals in either direction, allowing them to be used as multiplexers or as demultiplexers.

On-chip address latches and decode logic simplify microprocessor interface. Chip Select and Enable inputs simplify addressing in large matrices. Single-supply operation and a low 75 μ W power consumption vastly reduces power supply requirements.

These devices are built on a proprietary D/CMOS process which creates low-capacitance DMOS FETs and high-speed, low-power CMOS logic on the same substrate.

For more information please refer to Vishay Siliconix Application Note AN501 (FaxBack document number 70608).

FEATURES

- Crosstalk: -100 dB at 5 MHz
- 300 MHz Bandwidth
- Low Input and Output Capacitance
- Low Power: 75 μ W
- Low $r_{DS(on)}$: 50 Ω
- On-Board Address Latches
- Disable Output



RoHS*
COMPLIANT

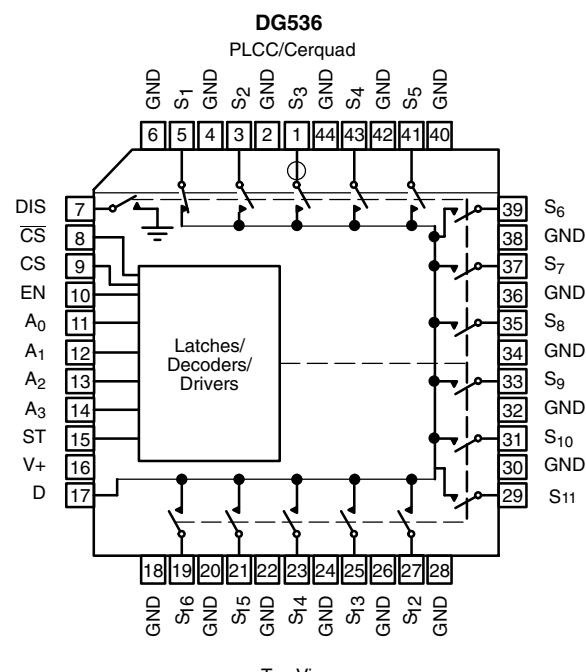
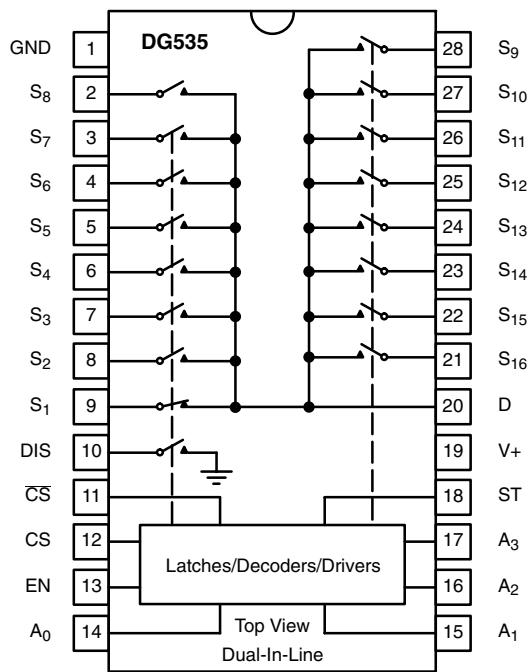
BENEFITS

- High Video Quality
- Reduced Insertion Loss
- Reduced Input Buffer Requirements
- Minimizes Power Consumption
- Simplifies Bus Interface

APPLICATIONS

- Video Switching/Routing
- High Speed Data Routing
- RF Signal Multiplexing
- Precision Data Acquisition
- Crosspoint Arrays
- FLIR Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



* Pb containing terminations are not RoHS compliant, exemptions may apply

ORDERING INFORMATION

Temperature Range	Package	Part Number
- 40 to 85 °C	28-Pin Plastic DIP	DG535DJ DG535DJ-E3
	44-Pin PLCC	DG536DN DG536DN-E3

TRUTH TABLE

EN	CS	\bar{CS}	ST ^a	A ₃	A ₂	A ₁	A ₀	Channel Selected	Disable ^b
0	X	X							
X	0	X							
X	X	1							
1	1	0	1	0	0	0	0	S ₁	Low Z
				0	0	0	1	S ₂	
				0	0	1	0	S ₃	
				0	0	1	1	S ₄	
				0	1	0	0	S ₅	
				0	1	0	1	S ₆	
				0	1	1	0	S ₇	
				0	1	1	1	S ₈	
				1	0	0	0	S ₉	
				1	0	0	1	S ₁₀	
				1	0	1	0	S ₁₁	
				1	0	1	1	S ₁₂	
				1	1	0	0	S ₁₃	
				1	1	0	1	S ₁₄	
				1	1	1	0	S ₁₅	
				1	1	1	1	S ₁₆	
X	X	X	0	X	X	X	X	Maintains previous switch condition	High Z or Low Z

Logic "0" = $V_{AL} \leq 4.5 \text{ V}$ Logic "1" = $V_{AH} \geq 10.5 \text{ V}$

X = Do not Care

Notes:

a. Strobe input (ST) is level triggered.

b. Low Z, High Z = impedance of Disable Output to GND. Disable output sinks current when any channel is selected.

ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
V+ to GND	- 0.3 to + 18	V
Digital Inputs	(GND - 0.3) to (V+) + 2 or 20 mA, whichever occurs first	
V_S, V_D	(GND - 0.3) to (V+) + 2 or 20 mA, whichever occurs first	
Current (any terminal) Continuous	20	mA
	40	
Storage Temperature	(A Suffix)	°C
	(D Suffix)	
Power Dissipation (Package) ^a	28-Pin Plastic DIP ^b	mW
	28-Pin Sidebrazed ^c	
	44-Pin PLCC ^d	
	44-Pin Cerquad ^e	

Notes:

a. All leads soldered or welded to PC board.

b. Derate 8.6 mW/°C above 75 °C.

c. Derate 16 mW/°C above 75 °C.

d. Derate 6 mW/°C above 75 °C.

e. Derate 11 mW/°C above 75 °C.

SPECIFICATIONS ^a											
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, ST, CS = 10.5 V CS = 4.5 V, V _A = 4.5 or 10.5 V ^f			Temp ^b	Typ ^c	A Suffix - 55 to 125 °C		D Suffix - 40 to 85 °C		Unit
							Min ^c	Max ^c	Min ^c	Max ^c	
Analog Switch											
Analog Signal Range ^e	V _{ANALOG}		Full		0	10	0	10	V		
Drain-Source On-Resistance	r _{DS(on)}	I _S = - 1 mA, V _D = 3 V, EN = 10.5 V Sequence Each Switch On	Room	55		90		90	Ω		
Resistance Match	Δr _{DS(on)}		Full			120		120			
Source Off Leakage Current	I _{S(off)}	V _S = 3 V, V _D = 0 V, EN = 4.5 V	Room		- 10	10	- 10	10	nA		
Drain On Leakage Current	I _{D(on)}	V _S = V _D = 3 V, EN = 10.5 V	Room		- 100	100	- 100	100			
Disable Output	R _{DISABLE}	I _{DISABLE} = 1 mA, EN = 10.5 V	Room	100		200		200	Ω		
Digital Control											
Input Voltage High	V _{AIH}		Full		10.5		10.5		V		
Input Voltage Low	V _{AIL}		Full			4.5		4.5			
Address Input Current	I _{AI}	V _A = GND or V ₊	Room	< 0.01	- 1	1	- 1	1	μA		
Address Input Capacitance	C _A		Full	5					pF		
Dynamic Characteristics											
On State Input Capacitance ^e	C _{S(on)}	V _D = V _S = 3 V	PLCC	Room	32		45		pF		
			Cerquad	Room	35						
			DIP	Room	40		55				
Off State Input Capacitance ^e	C _{S(off)}	V _S = 3 V	PLCC	Room	2		8				
			Cerquad	Room	5						
			DIP	Room	3						
Off State Output Capacitance ^e	C _{D(off)}	V _D = 3 V	PLCC	Room	8		20		ns		
			Cerquad	Room	12						
			DIP	Room	9						
Multiplexer Switching Time	t _{TRANS}	See Figure 4	Full			300		300	ns		
Break-Before-Make Interval	t _{OPEN}		Full		25		25				
EN, CS, CS, ST, t _{ON}	t _{ON}	See Figure 2 and 3	Full			300		300			
EN, CS, CS, ST, t _{OFF}	t _{OFF}	See Figure 2	Full			150		150			
Charge Injection	Q	See Figure 5	Room	- 35					pC		
Single-Channel Crosstalk	X _{TALK(SC)}	R _{IN} = 75 Ω, R _L = 75 Ω f = 5 MHz See Figure 9	PLCC	Room	- 100				dB		
			Cerquad	Room	- 93						
			DIP	Room	- 60						
Chip Disabled Crosstalk	X _{TALK(CD)}	R _{IN} = R _L = 75 Ω, f = 5 MHz EN = 4.5 V See Figure 8	PLCC	Room	- 85						
			Cerquad	Room	- 84						
			DIP	Room	- 60						
Adjacent Input Crosstalk	X _{TALK(AI)}	R _{IN} = 10 Ω, R _L = 10 kΩ f = 5 MHz See Figure 10	PLCC	Room	- 92						
			Cerquad	Room	- 87						
			DIP	Room	- 72						
All Hostile Crosstalk ^e	X _{TALK(AH)}	R _{IN} = 10 Ω, R _L = 10 kΩ f = 5 MHz See Figure 7	PLCC	Room	- 74	- 60		- 60			
			Cerquad	Room	- 74						
			DIP	Room	- 60						
Bandwidth	BW	R _L = 50 Ω, See Figure 6	Room	500					MHz		

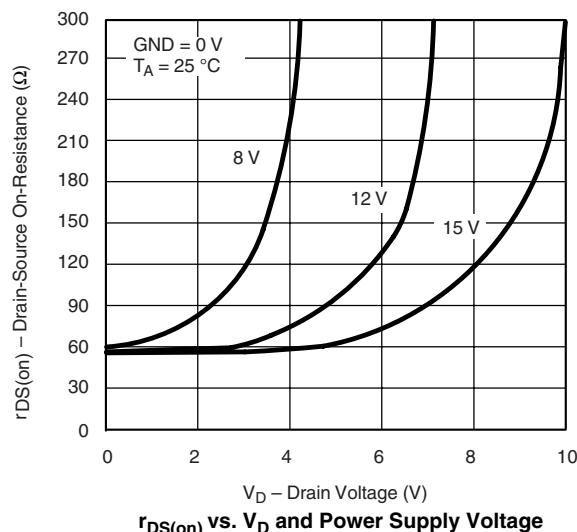
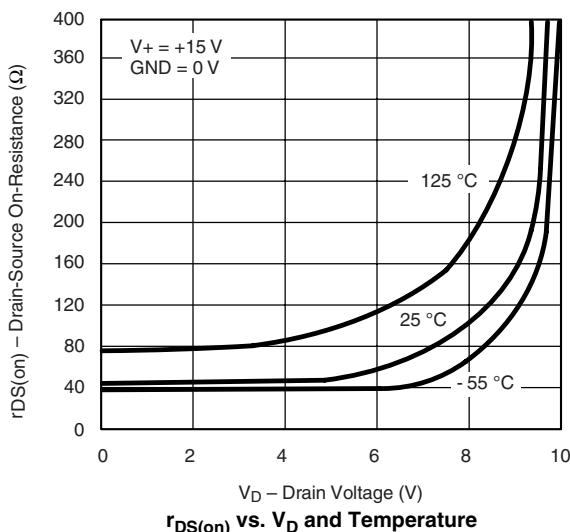
SPECIFICATIONS^a

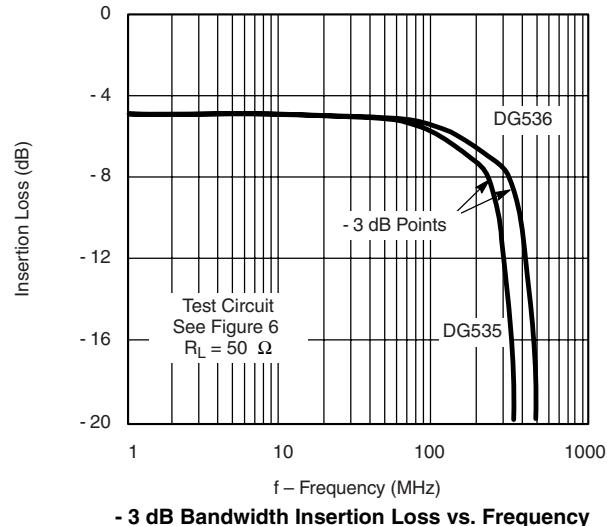
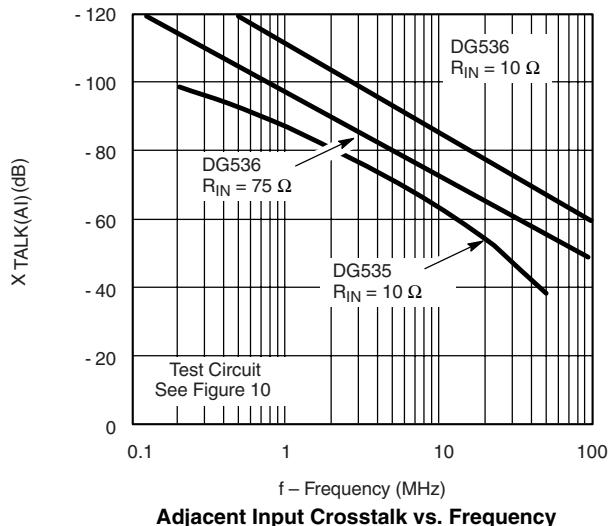
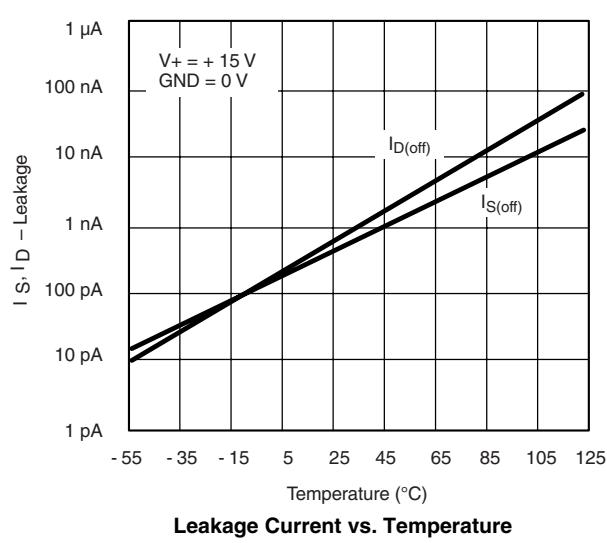
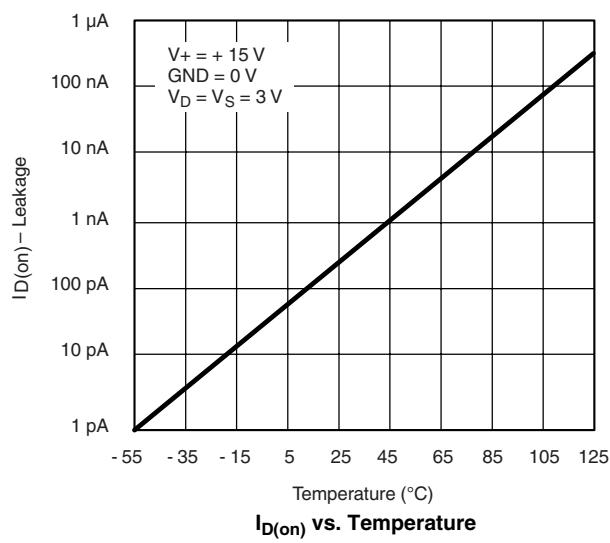
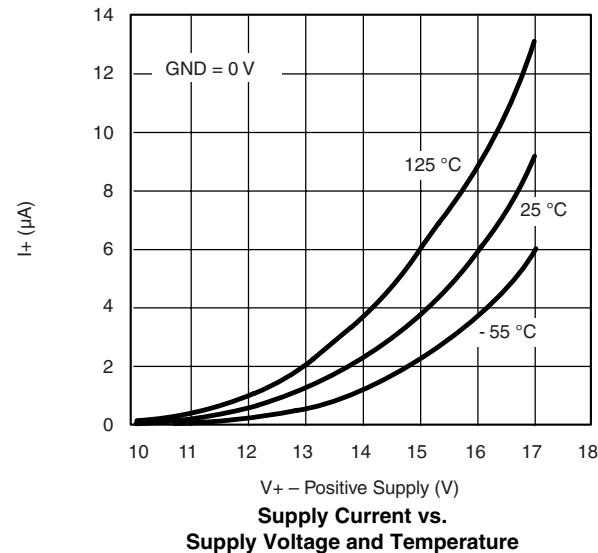
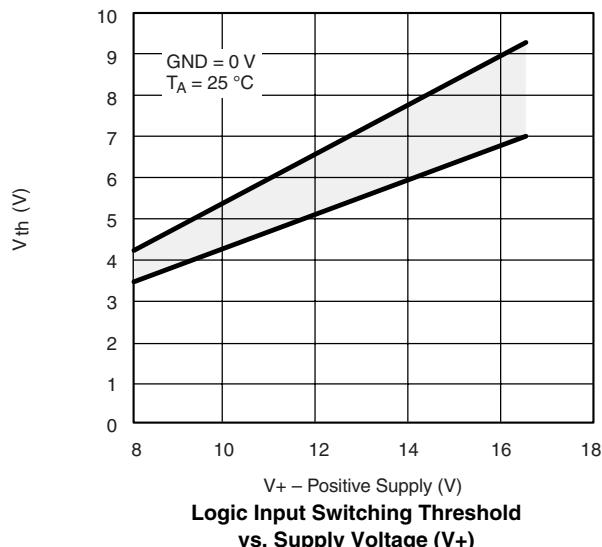
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					Min ^c	Max ^c	Min ^c	Max ^c	
Power Supplies									
Positive Supply Current	I ₊	Any One Change I Selected with All Logic Inputs at GND or V ₊	Room Full	5		50 100		50 100	μA
Supply Voltage Range	V ₊		Full		10	16.5	10	16.5	V
Minimum Input Timing Requirements									
Strobe Pulse Width	t _{SW}	See Figure 1	Full		200		200		ns
A ₀ , A ₁ , A ₂ , A ₃ CS, CS, EN Data Valid to Strobe	t _{DW}		Full		100		100		
A ₀ , A ₁ , A ₂ , A ₃ CS, CS, EN Data Valid after Strobe	t _{WD}		Full		50		50		

Notes:

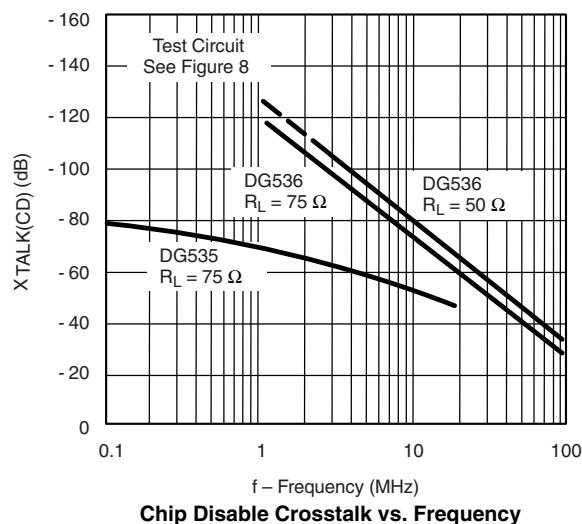
- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. V_A = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

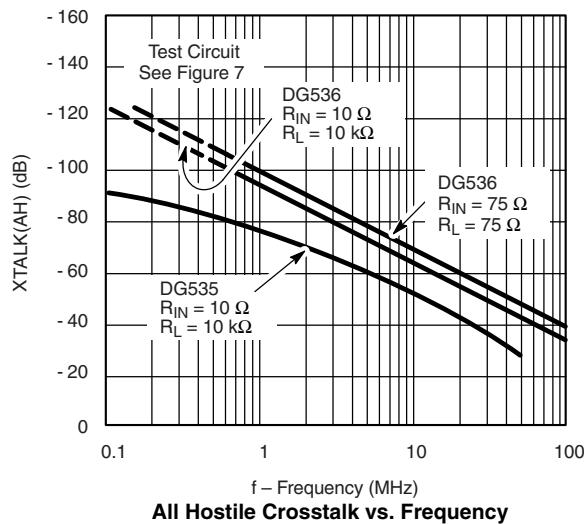
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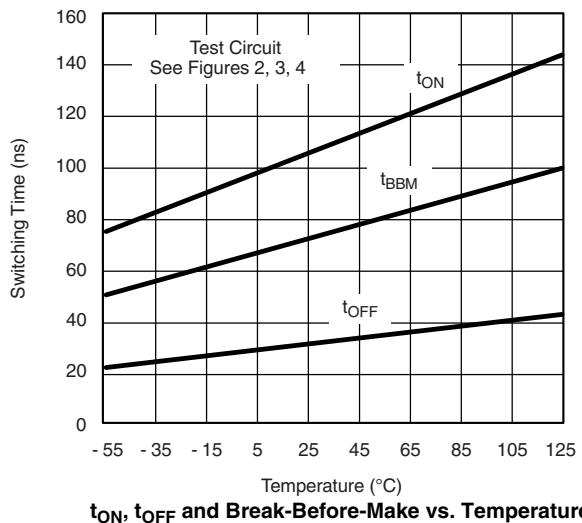
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



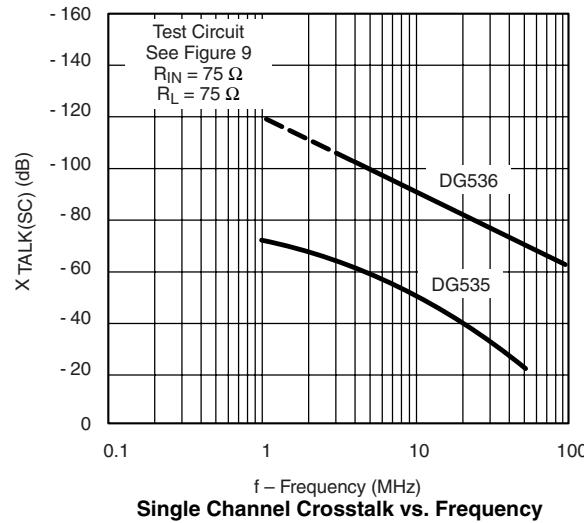
Chip Disable Crosstalk vs. Frequency



All Hostile Crosstalk vs. Frequency



t_{ON} , t_{OFF} and Break-Before-Make vs. Temperature



Single Channel Crosstalk vs. Frequency

INPUT TIMING REQUIREMENTS

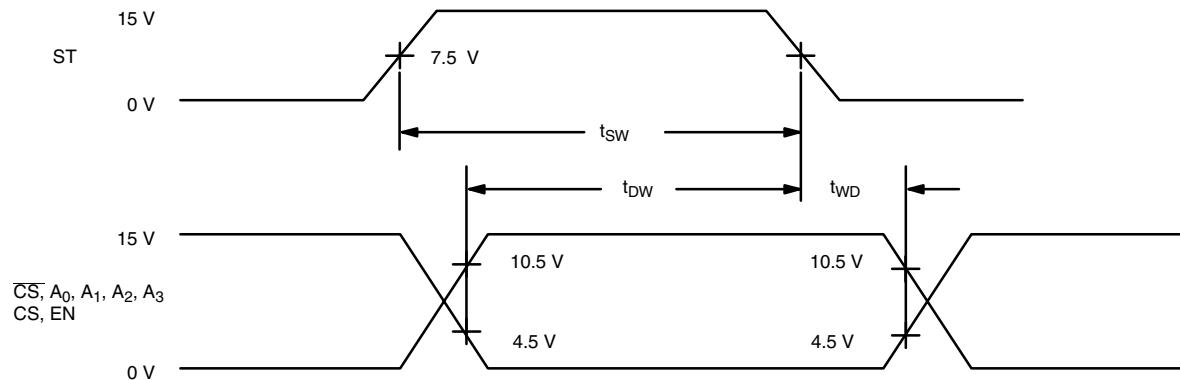
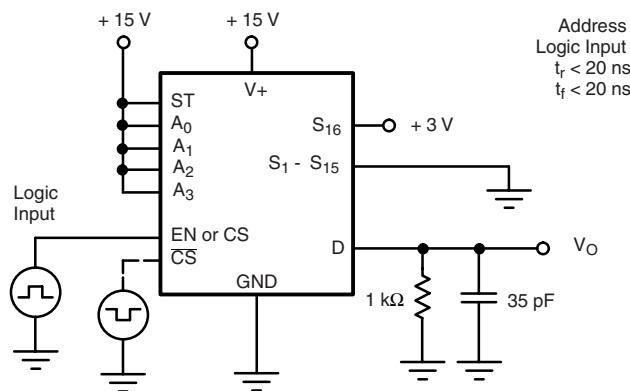
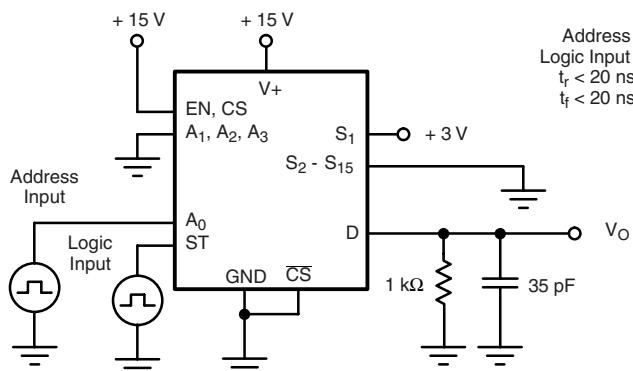
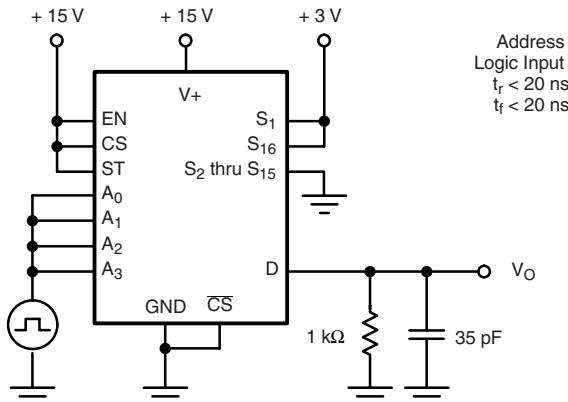
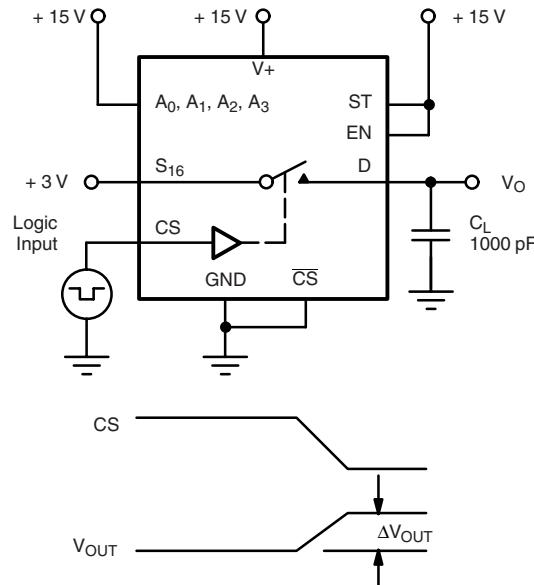


Figure 1.

TEST CIRCUITS

Figure 2. EN, CS, $\overline{\text{CS}}$, Turn On/Off Time

Figure 3. Strobe ST Turn On Time

Figure 4. Transition Time and Break-Before-Make Interval

TEST CIRCUITS



ΔV_{OUT} is the measured voltage error due to charge injection.
The charge injection in Coulombs is $Q = C_L \times \Delta V_{OUT}$

Figure 5. Charge Injection

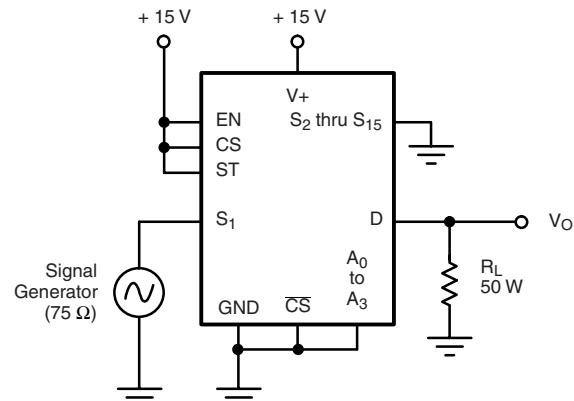


Figure 6. Bandwidth

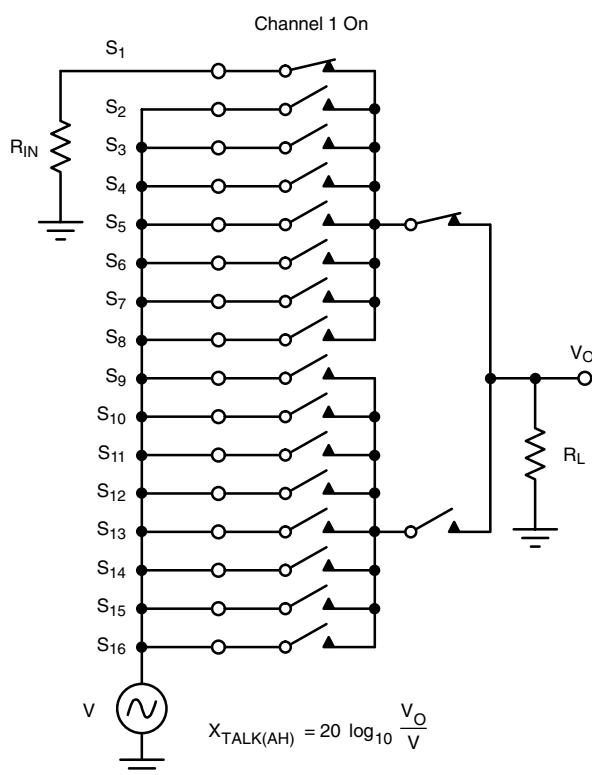


Figure 7. All Hostile Crosstalk

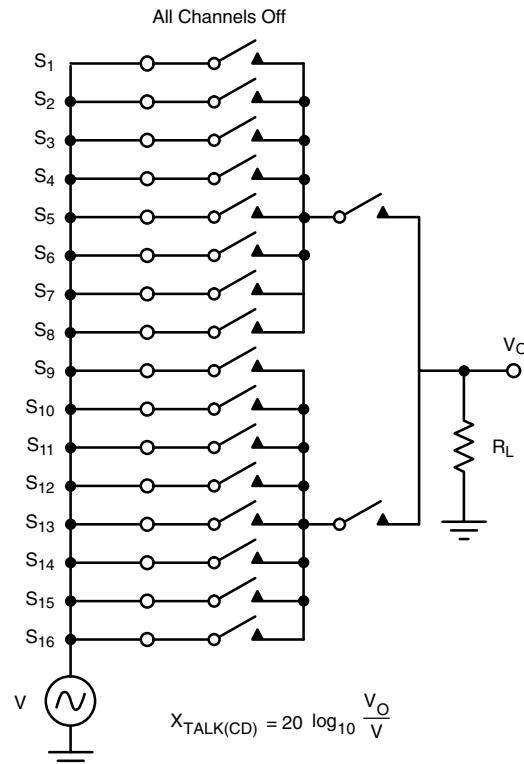
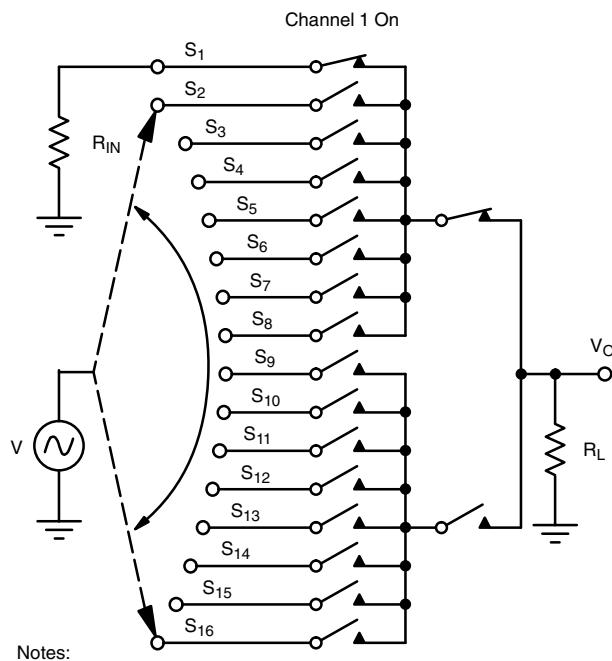
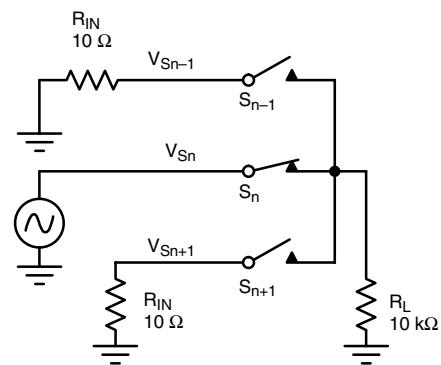


Figure 8. Chip Disabled Crosstalk

TEST CIRCUITS

Figure 9. Single Channel Crosstalk

Figure 10. Adjacent Input Crosstalk

$$X_{TALK(AI)} = 20 \log_{10} \frac{V_{Sn-1}}{V_{Sn}} \text{ or } 20 \log_{10} \frac{V_{Sn+1}}{V_{Sn}}$$

PIN DESCRIPTION	
Symbol	Description
S_1 thru S_{16}	Analog inputs/outputs
D	Multiplexer output/demultiplexer input
DIS	Open drain low impedance to analog ground when any channel is selected
\overline{CS} , CS, EN	Logic inputs to selected desired multiplexer(s) when using several multiplexers in a system
A_0 thru A_3	Binary address inputs to determine which channel is selected
ST	Strobe input that latches A_0 , A_1 , A_2 , A_3 , \overline{CS} , CS, EN
V+	Positive supply voltage input
GND	Analog signal ground and most negative potential All ground pins should be connected externally to ensure dynamic performance

DETAILED DESCRIPTION

The DG535/536 are 16-channel single-ended multiplexers with on-chip address logic and control latches.

The multiplexer connects one of sixteen inputs (S_1 , S_2 through S_{16}) to a common output (D) under the control of a 4-bit binary address (A_0 to A_3). The specific input channel selected for each address is given in the Truth Table.

All four address inputs have on-chip data latches which are controlled by the Strobe (ST) input. These latches are transparent when Strobe is high but they maintain the chosen address when Strobe goes low. To facilitate easy microprocessor control in large matrices a choice of three independent logic inputs (EN, CS and \bar{CS}) are provided on chip. These inputs are gated together (see Figure 11) and only when $EN = CS = 1$ and $\bar{CS} = 0$ can an output switch be selected. This necessary logic condition is then latched-in when Strobe (ST) goes low.

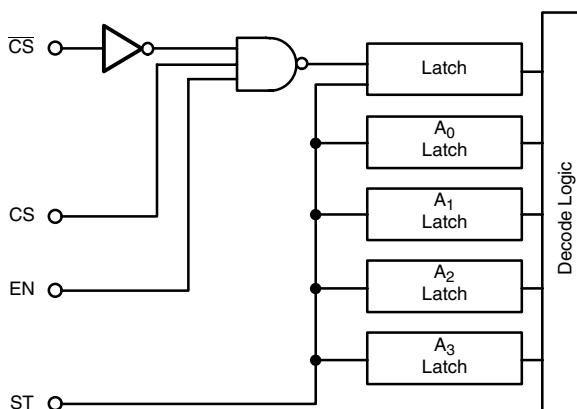


Figure 11. \bar{CS} , CS, EN, ST Control Logic

Break-before-make switching prevents momentary shorting when changing from one input to another.

The devices feature a two-level switch arrangement whereby two banks of eight switches (first level) are connected via two series switches (second level) to a common DRAIN output.

In order to improve crosstalk all sixteen first level switches are configured as "T" switches (see Figure 12).

With this method SW₂ operates out of phase with SW₁ and SW₃. In the on condition SW₁ and SW₃ are closed with SW₂ open whereas in the off condition SW₁ and SW₃ are open and SW₂ closed. In the off condition the input to SW₃ is effectively the isolation leakage of SW₁ working into the on-resistance of SW₂ (typically 200 Ω).

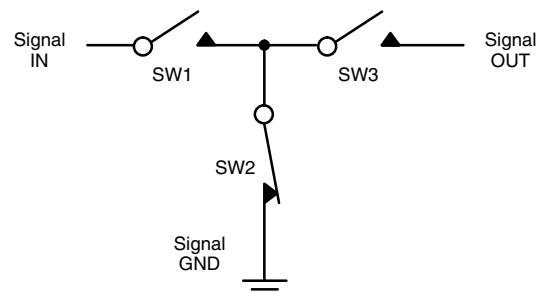


Figure 12. "T" Switch Arrangement

The two second level series switches further improve crosstalk and help to minimize output capacitance.

The DIS output can be used to signal external circuitry. DIS is a high impedance to GND when no channel is selected and a low impedance to GND when any one channel is selected.

The DG535/536 have extensive applications where any high frequency video or digital signals are switched or routed. Exceptional crosstalk and bandwidth performance is achieved by using n-channel DMOS FETs for the "T" and series switches.

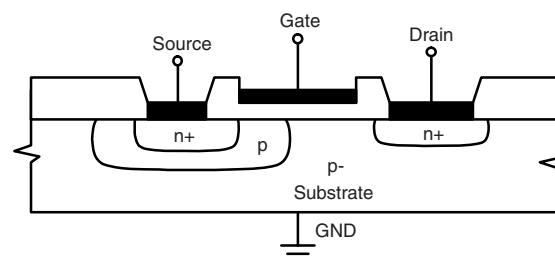


Figure 13. Cross-Section of a Single DMOS Switch

It can clearly be seen from Figure 13 that there exists a PN junction between the substrate and the drain/source terminals.

Should a signal which is negative with respect to the substrate (GND pin) be connected to a source or drain terminal, then the PN junction will become forward biased and current will flow between the signal source and GND. This effective shorting of the signal source to GND will not necessarily cause any damage to the device, provided that the total current flowing is less than the maximum rating, (i.e., 20 mA).

DETAILED DESCRIPTION

Since no PN junctions exist between the signal path and V+, positive overvoltages are not a problem, unless the breakdown voltage of the DMOS drain terminal (see Figure 13) (+ 18 V) is exceeded. Positive overvoltage conditions must not exceed + 18 V with respect to the GND pin. If this condition is possible (e.g. transients in the signal), then a diode or Zener clamp may be used to prevent breakdown.

The overvoltage conditions described may exist if the supplies are collapsed while a signal is present on the inputs. If this condition is unavoidable, then the necessary steps outlined above should be taken to protect the device

DC Biasing

To avoid negative overvoltage conditions and subsequent distortion of ac analog signals, dc biasing may be necessary. Biasing is not required, however, in applications where signals are always positive with respect to the GND or substrate connection, or in applications involving multiplexing of low level (up to \pm 200 mV) signals, where forward biasing of the PN substrate-source/drain terminals would not occur.

Biasing can be accomplished in a number of ways, the simplest of which is a resistive potential divider and a few dc blocking capacitors as shown in Figure 14.

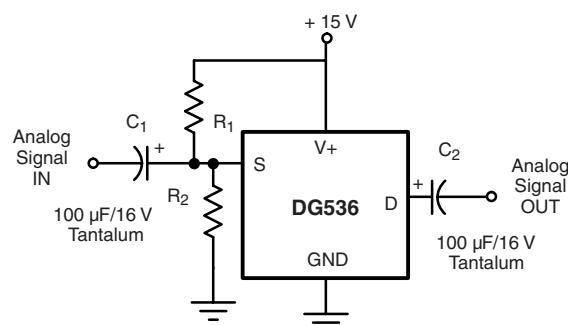


Figure 14. Simple Bias Circuit

R₁ and R₂ are chosen to suit the appropriate biasing requirements. For video applications, approximately 3 V of bias is required for optimal differential gain and phase performance. Capacitor C₁ blocks the dc bias voltage from being coupled back to the analog signal source and C₂ blocks the dc bias from the output signal. Both C₁ and C₂ should be tantalum or ceramic disc type capacitors in order to operate efficiently at high frequencies. Active bias circuits are recommended if rapid switching time between channels is required.

An alternative method is to offset the supply voltages (see Figure 15).

Decoupling would have to be applied to the negative supply to ensure that the substrate is well referenced to signal ground. Again the capacitors should be of a type offering good high frequency characteristics.

Level shifting of the logic signals may be necessary using this offset supply arrangement.

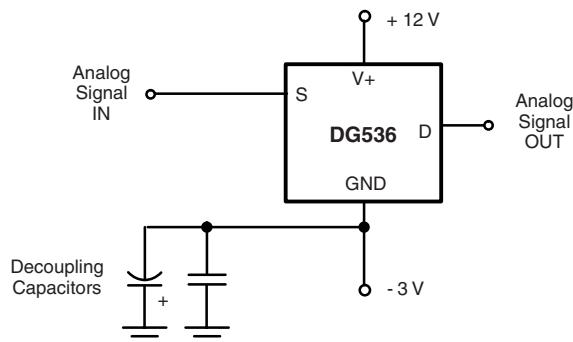


Figure 15. DG536 with Offset Supply

TTL to CMOS level shifting is easily obtained by using a MC14504B.

Circuit Layout

Good circuit board layout and extensive shielding is essential for optimizing the high frequency performance of the DG536. Stray capacitances on the PC board and/or connecting leads will considerably degrade the ac performance. Hence, signal paths must be kept as short as practically possible, with extensive ground planes separating signal tracks.

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