CD74FCT651, CD74FCT652

BiCMOS FCT Interface Logic, Octal Bus Transceivers/Registers, Three-State

Data sheet acquired from Harris Semiconductor
SCHS262

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- **Buffered Inputs**
- **Typical Propagation Delay: 6.8ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF**
- **CD75FCT651**
  - **Inverting**
- **CD74FCT652**
  - **Noninverting**
- **Family Features**
  - **SCR Latchup Resistant BiCMOS Process and Circuit Design**
  - **Speed of Bipolar FAST™/AS/S**
  - **64mA Output Sink Current**
  - **Output Voltage Swing Limited to 3.7V at V_{CC} = 5V**
  - **Controlled Output Edge Rates**
  - **Input/Output Isolation to V_{CC}**
  - **BiCMOS Technology with Low Quiescent Power**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT651EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT652EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT651M	0 to 70	24 Ld SOIC	M24.3
CD74FCT652M	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

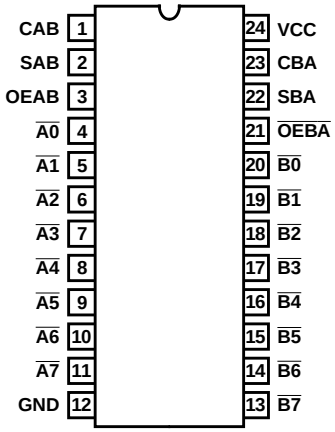
The CD74FCT651 and CD74FCT652 three-state, octal bus transceivers/registers use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 milliamperes.

These devices consist of bus transceiver circuits, D-Type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OEAB and $\overline{OEBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data. The following examples demonstrate the four fundamental bus management functions that can be performed with the octal bus transceivers and registers.

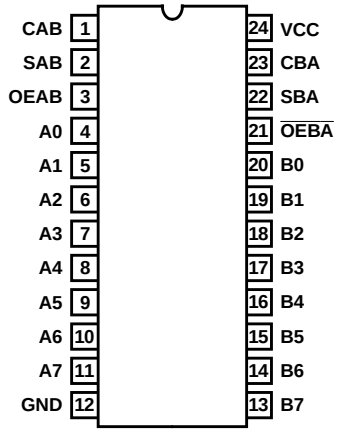
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low to high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-Type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

Pinouts

CD74FCT651 (PDIP, SOIC)
TOP VIEW



CD74FCT652 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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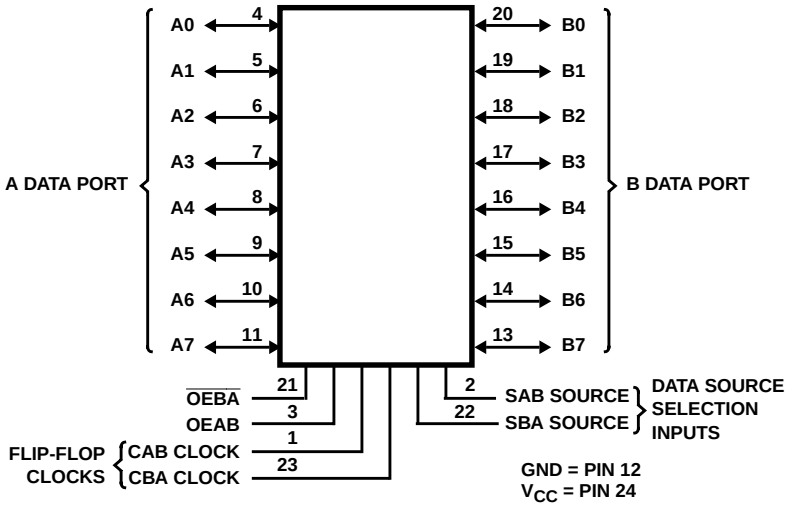
File Number **2394.2**

Functional Diagram



TRUTH TABLE

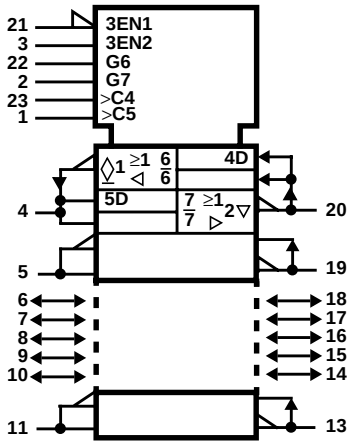
INPUTS						DATA I/O		OPERATION OR FUNCTION	
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD74FCT651	CD74FCT652
L L	H H	H or L ↑	H or L ↑	X X	X X	Input Input	Input Input	Isolation (Note 1) Store A and B Data	Isolation (Note 1) Store A and B Data
X H	H H	↑ ↑	H or L ↑	X X (3)	X X	Input Input	Unspecified (2) Output	Store A, Hold B Store A in both registers	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X X (3)	Unspecified (2) Output	Input Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output Output	Input Input	Real-Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input Input	Output Output	Real-Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus Stored B Data to A Bus

NOTES:

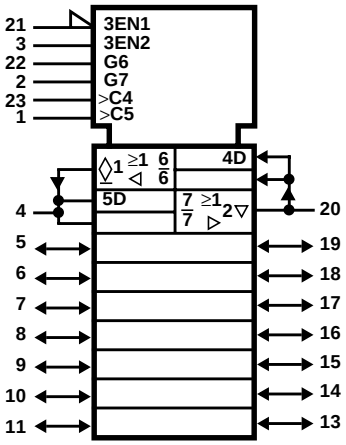
1. To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.
2. The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
3. Select control = L; clocks can occur simultaneously. Select control = H; clocks must be staggered in order to load both registers.

IEC Logic Symbol

CD74FCT651



CD74FCT652



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} ($^oC/W$)
PDIP Package	75
SOIC Package	75

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC-Lead Tips Only)

Operating Conditions

Operating Temperature Range (T_A) . . . . . 0^oC to 70^oC
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Commercial Temperature Range 0^oC to 70^oC, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25^oC		0^oC TO 70^oC		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 5)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 6)		Max	-	1.6	-	1.6	mA

NOTES:

5. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
6. Inputs that are not measured are at V_{CC} or GND.
7. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70^oC.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 4)

PARAMETER		SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays							
Stored $\overline{An}$ → Bn	CD74FCT651	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Stored An → Bn	CD74FCT652	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Stored $\overline{Bn}$ → An	CD74FCT651	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Stored Bn → An	CD74FCT652	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
$\overline{An}$ → Bn	CD74FCT651	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
An → Bn	CD74FCT652	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
$\overline{Bn}$ → An	CD74FCT651	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Bn → An	CD74FCT652	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Select to Data	CD74FCT651, CD74FCT652	t_{PLH}, t_{PHL}	5	8.3	2	11	ns
Three-State Enabling Time, Bus to Output or Register to Output	CD74FCT651, CD74FCT652	t_{PZL}, t_{PZH}	5	7.5	2	10	ns
Three-State Disabling Time, Bus to Output or Register to Output	CD74FCT651, CD74FCT652	t_{PLZ}, t_{PHZ}	5	7.5	2	10	ns
Power Dissipation Capacitance		C_{PD} (Note 8)	–				pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV}	5	0.5 Typical at 25°C			V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP}	5	1 Typical at 25°C			V
Input Capacitance		C_I	-	-	-	10	pF
Input/Output Capacitance		$C_{I/O}$	-	-	-	15	pF

NOTE:

8. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_I C_{PD} + V_O^2 f_O C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

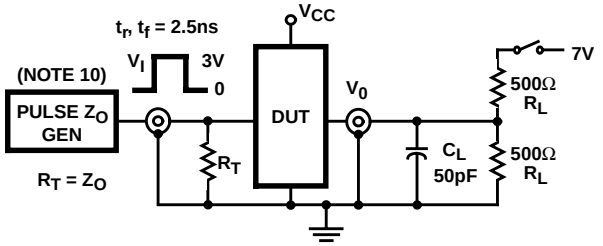
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Maximum Frequency	f_{MAX}	5 (Note 9)	-	85	-	MHz
Data to Clock Setup Time	t_{SU}	5	-	4	-	ns
Data to Clock Hold Time	t_H	5	-	2	-	ns
Clock Pulse Width	t_W	5	-	6	-	ns

NOTE:

9. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

10. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: t_r = t_f = 2.5ns (10% to 90%), unless otherwise specified

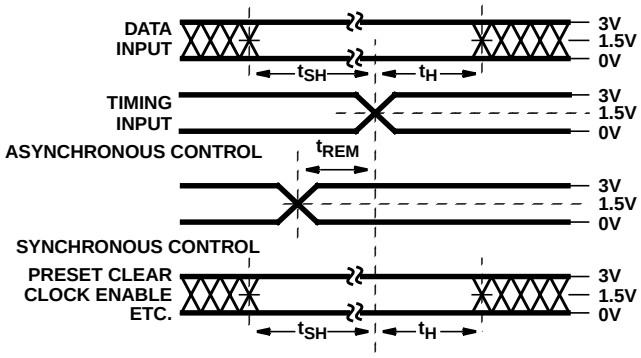


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

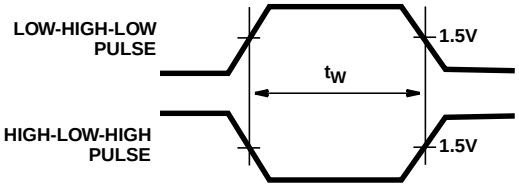


FIGURE 3. PULSE WIDTH

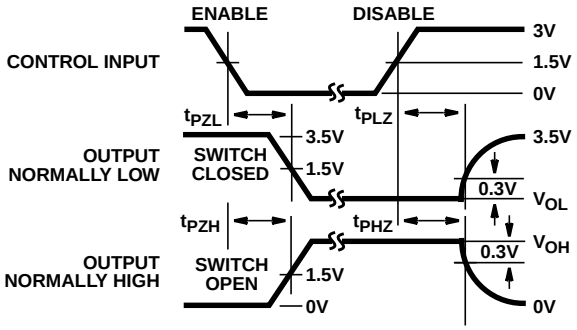


FIGURE 4. ENABLE AND DISABLE TIMING

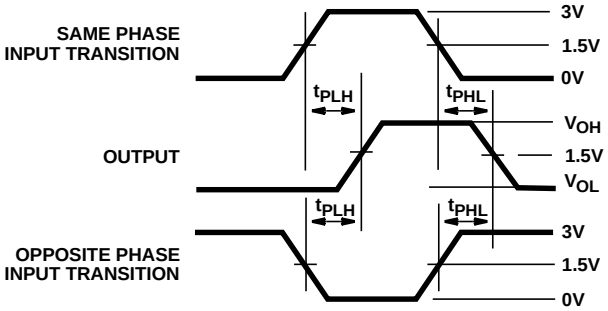
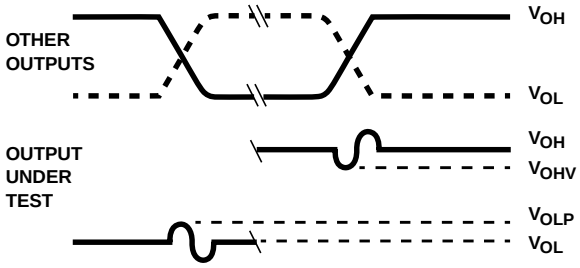


FIGURE 5. PROPAGATION DELAY

Test Circuits and Waveforms (Continued)



NOTES:

11. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
12. Input pulses have the following characteristics:
    $P_{RR} \leq 1MHz$, $t_r = 2.5ns$, $t_f = 2.5ns$, skew 1ns.
13. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD74FCT651EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
CD74FCT651M	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
CD74FCT652EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
CD74FCT652M	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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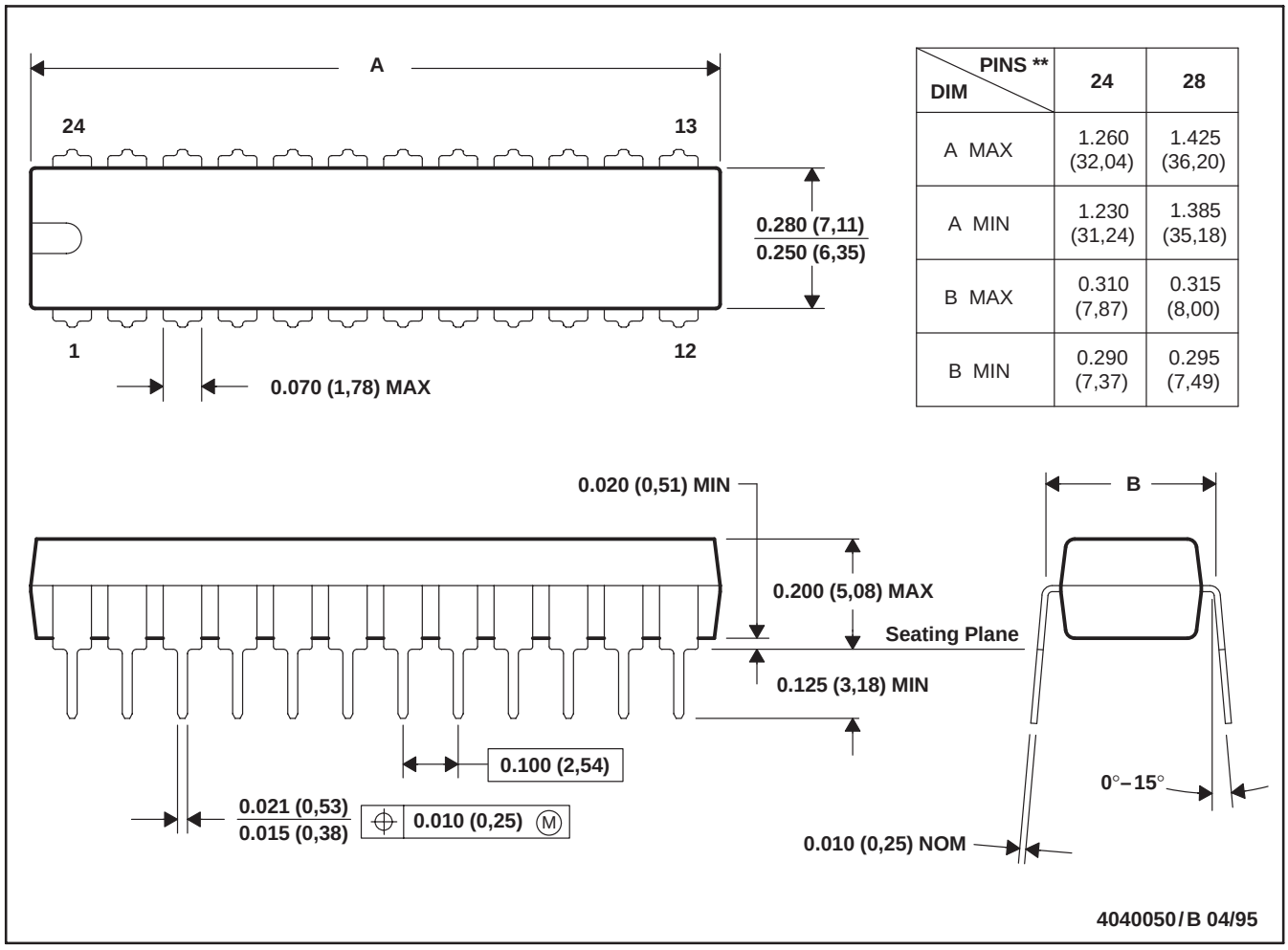
NT (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

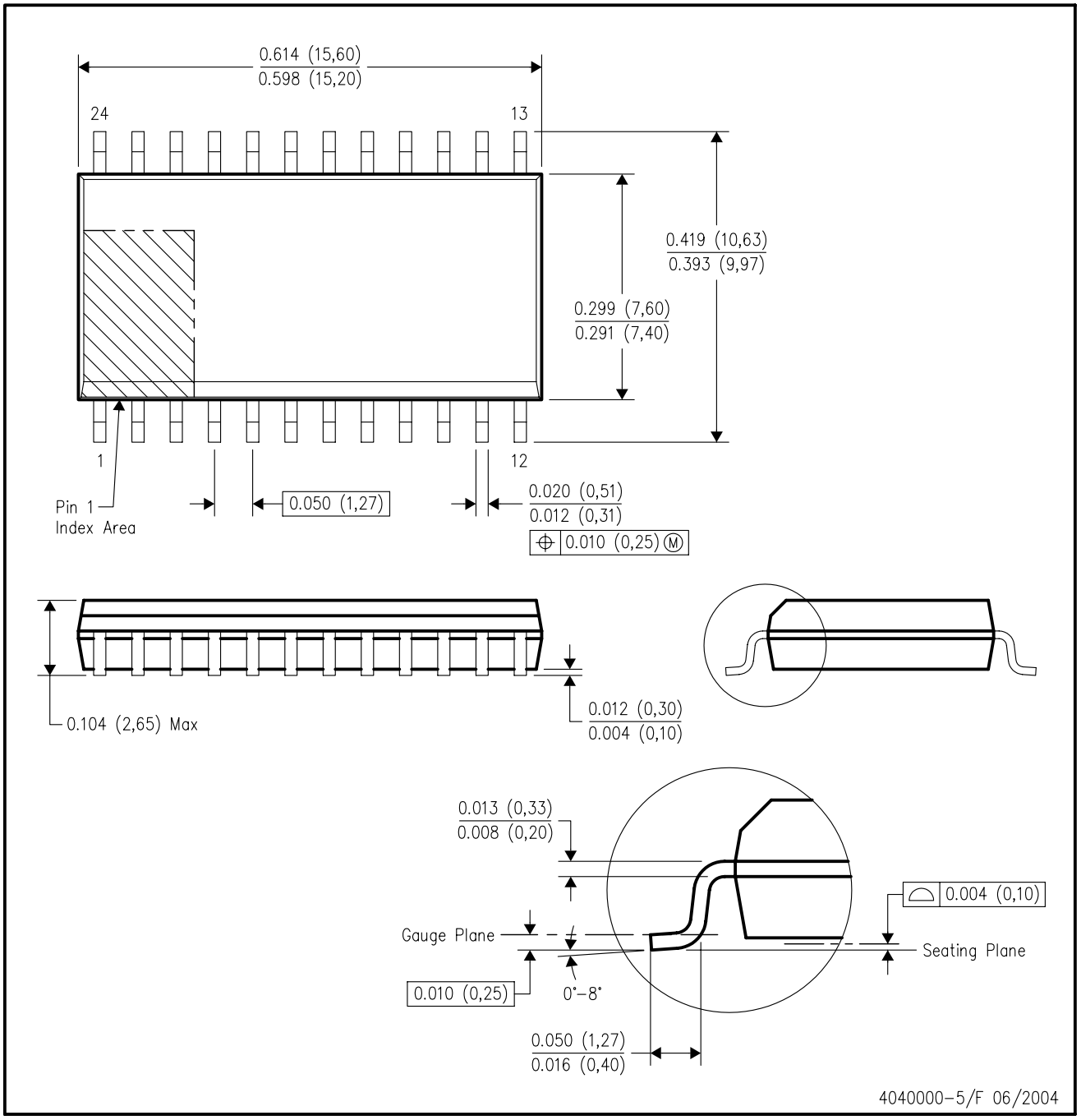
24 PINS SHOWN



DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

DW (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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