FAIRCHILD SEMICONDUCTOR®

October 2012

FT3001
Reset Timer with Configurable Delay

Features

- Delay Times: 3.0, 3.75, 4.5, 6.0 Seconds
- ≤ 1 µA I_{CC} Current Consumption in Standby
- Primary and Secondary Input Reset Pins
- Push-Pull and Open-Drain Output Pins
- 1.65 V to 5.0 V Operation at T_A = 0°C to +85°C
- 1.7 V to 5.0 V Operation at T_A = 0°C to +85°C
- 1.8 V to 5.0 V Operation at T_A = -40°C to +85°C
- Available in 8-Lead MLP and 10-Lead UMLP Packages
- ESD Protection Exceeds:
  - 4 kV HBM (per JESD22-A114 & Mil Std 883e 3015.7)
  - 2 kV CDM (per ESD STM 5.3)

Description

The FT3001 is a timer for resetting a mobile device where long reset times are needed. The long delay helps avoid unintended resets caused by accidental key presses. Four timer values can be selected by hard-wiring the DSR0 and DSR1 pins.

The FT3001 has two inputs for single- or dual-button resetting capability. The device has two outputs: a push-pull output with 0.5 mA drive and an open-drain output with 0.5 mA pull-down drive.

The FT3001 draws minimal supply current when inactive and functions over a power supply range of 1.65 V to 5.0 V.

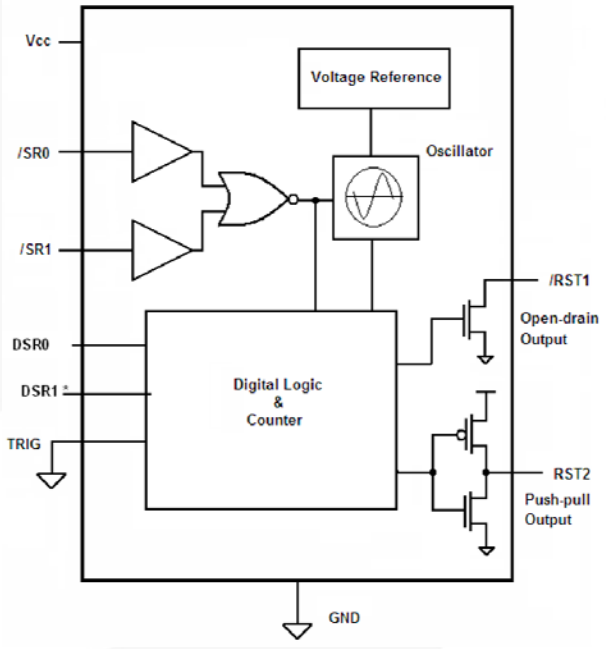

Figure 1. Block Diagram

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FT3001UMX	-40°C to +85°C	10-Lead, Ultrathin MLP, 1.4 x 1.8 x 0.55mm Package, 0.40 mm Pitch	5000 Units Tape and Reel
FT3001MPX	-40°C to +85°C	8-Lead, Molded Leadless Package (MLP), Dual JEDEC, MO-229 2.0 x 2.0 mm	3000 Units Tape and Reel

Pin Configurations

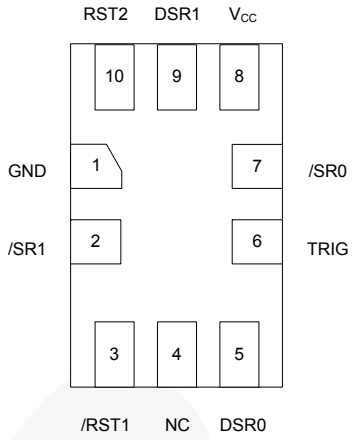

Figure 2. UMLP (Top Through View)

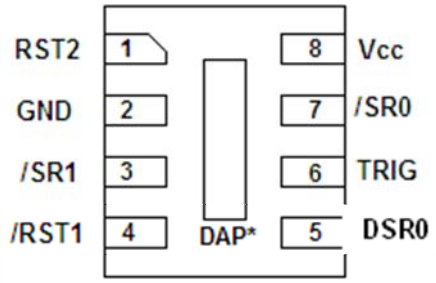

Figure 3. MLP (Top Through View)

Pin Definitions

UMLP Pin#	MLP Pin#	Name	Description
1	2	GND	Ground
2	3	/SR1	Secondary Reset Input, Active LOW
3	4	/RST1	Open-Drain Output, Active LOW
4		NC	No Connect
5	5	DSR0	Delay Selection Input (Must be tied directly to GND or V_{CC}; do not use pull-up or pull-down resistors.)
6	6	TRIG	Test Pin; tied to ground in normal use
7	7	/SR0	Primary Reset Input, Active LOW
8	8	V_{CC}	Power Supply
9		DSR1	Delay Selection Input (Must be tied directly to GND or V_{CC}; do not use pull-up or pull-down resistors.)
10	1	RST2	Push-Pull Output, Active HIGH

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage	/SR0, /SR1, TRIG, DSR0	-0.5	7.0	V
V_{OUT}	Output Voltage[1]	/RST1, RST2 HIGH or LOW	-0.5	V_{CC}+0.5	V
		/RST1, RST2, V_{CC}=0 V	-0.5	7.0	
I_{IK}	DC Input Diode Current	V_{IN} < 0 V		-50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V		-50	mA
		V_{OUT} > V_{CC}		+50	
I_{OH}/I_{OL}	DC Output Source/Sink Current		-50	+50	mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin			±100	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
V_{CC}	Junction Temperature Under Bias			+150	°C
V_{IN}	Junction Lead Temperature, Soldering 10 Seconds			+260	°C
P_D	Power Dissipation			5	mW
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4	kV
		Charged Device Model, JESD22-C101		2	

Note:

1. I_O absolute maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage	T_A = 0°C to +85°C	1.65	5.00	V
		T_A = -25°C to +85°C	1.7	5.0	
		T_A = -40°C to +85°C	1.8	5.0	
t_{VCC_REC}	Vcc Recovery Time After Power Down	Vcc = 0 V after power down, then rising to 0.5 V	5		ms
V_{IN}	Input Voltage(2)	/SR0, /SR1	0	5.0	V
V_{OUT}	Output Voltage	/RST1, RST2 High or Low	0	V_{CC}	V
		/RST1, RST2, V_{CC} = 0 V	0	5.0	
I_{OH}	DC Output Source Current	RST2, 1.8 V ≤ V_{CC} ≤ 3.0 V	-100		µA
		RST2, 3.0 V ≤ V_{CC} ≤ 5.0 V	-500		
I_{OL}	DC Output Sink Current	/RST1, RST2, V_{CC} = 1.8V to 5.0 V	+500		
T_A	Free Air Operating Temperature		-40	+85	°C
Θ_{JA}	Thermal Resistance	MLP-8		245	°C/W
		UMLP-10		200	

Notes:
2. All unused inputs must be held at V_{CC} or GND.

DC Electrical Characteristics

Unless otherwise specified, conditions of T_A=-40 to 80C with V_{CC}=1.8 - 5.0V OR T_A=-25 to 85C with V_{CC}=1.7 – 5V OR T_A=0 to 85C with V_{CC}=1.65 – 5V produce the performance characteristics below.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IH}	Input High Voltage(3)	/SR0, /SR1	0.8 x V_{CC}		V
V_{IL}	Input Low Voltage	/SR0, /SR1		0.2 x V_{CC}	V
V_{IH}	Input High Voltage	DSR0, DSR1	0.8 x V_{CC}		V
V_{IL}	Input Low Voltage	DSR0, DSR1		0.2 x V_{CC}	V
V_{OH}	High Level Output Voltage	RST2, I_{OH}=-100 µA	0.8 x V_{CC}		V
		RST2, I_{OH}=-500 µA, V_{CC}=3.0 to 5.0V	0.8 x V_{CC}		
V_{OL}	Low Level Output Voltage	RST2, I_{OL}=500 µA		0.3	V
		/RST1, I_{OL}=500 µA		0.3	
I_{IN}	Input Leakage Current	V_{IN} =0.0 V or 5.0 V		±1	µA
I_{CC}	Quiescent Supply Current (Timer Inactive)	/SR0 or /SR1=V_{CC}		1	µA
I_{CC}	Dynamic Supply Current (Timer Active)	/SR0 and /SR1=0 V		100	µA

Note:
3. /SR0 and /SR1 HIGH levels should be referenced to the same V_{CC} rail supplying the FT3001.

AC Electrical Characteristics

Unless otherwise specified, conditions of T_A=-40 to 80°C with V_{cc}=1.8 - 5.0 V OR T_A=-25 to 85°C with V_{CC}=1.7 – 5 V OR T_A=0 to 85°C with V_{cc}=1.65 – 5 V produce the performance characteristics below.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{PHL1}, t_{PLH1}	Timer Delay, /SRn to /RST1 (DSR0=0, DSR1=0)	C_L=5 pF, R_L=5 kΩ, Figure 9, Figure 4, Figure 5	2.40	3.00	3.60	s
	Timer Delay, /SRn to /RST1 (DSR0=0, DSR1=1)	C_L=5 pF, R_L=5 kΩ, Figure 9, Figure 4, Figure 5	3.00	3.75	4.50	
	Timer Delay, /SRn to RST2 (DSR0=1, DSR1=0)	C_L=5 pF, R_L=10 kΩ, Figure 6, Figure 7	3.60	4.50	5.40	
	Timer Delay, /SRn to RST2 (DSR0=1, DSR1=1),	C_L=5 pF, R_L=10 kΩ, Figure 6, Figure 7	4.80	6.00	7.20	
t_{REC}	Reset Timeout Delay, /RST1 and RST2	Figure 4, Figure 5, Figure 6, Figure 7		400		ms

Capacitance Specifications

T_A = +25°C.

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC}=GND	4.0	pF
C_{OUT}	Output capacitance	V_{CC}=5.0 V	5.0	pF

AC Test Circuits and Waveforms

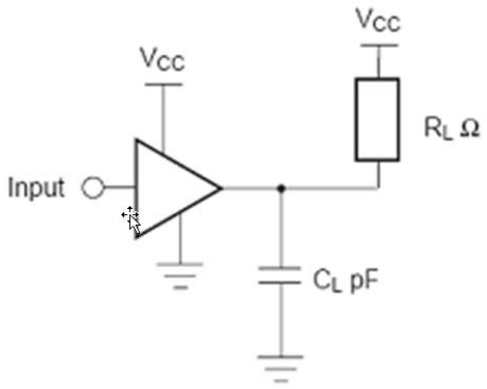

Figure 4. AC Test Circuit, RST1 Output

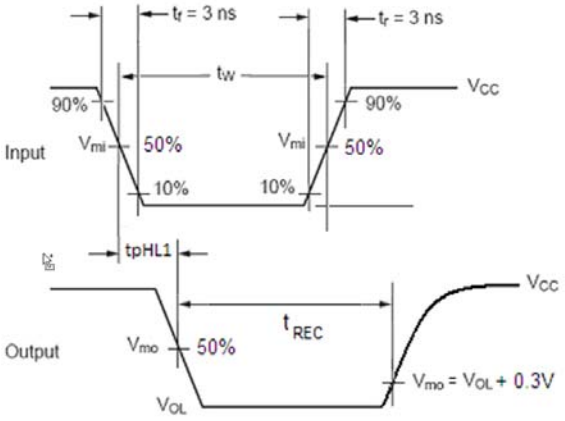

Figure 5. RST1 Output Waveform

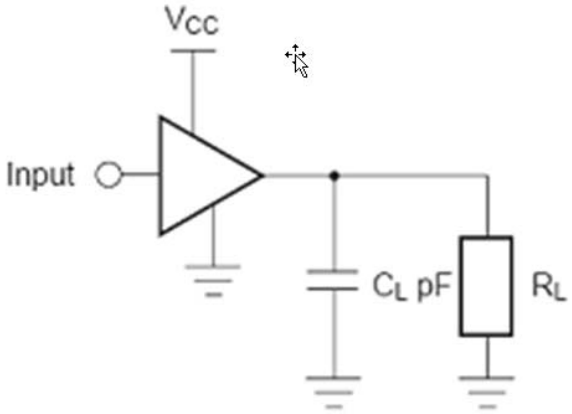

Figure 6. AC Test Circuit, RST2 Output

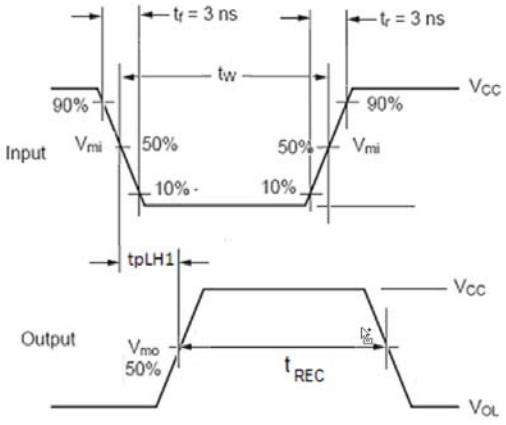

Figure 7. RST2 Output Waveform

Functional Description

The reset timer uses an internal oscillator and a two-stage 21-bit counter to determine when the output pins switch. The time, *n*, is set by the hard-wired logic level of the DSR0 and DSR1 pins. *See Table 1 & 2.*

Table 1. FT3001UMX Truth Table

DSR0	DSR1	Reset Time (±20%) in Seconds
0	0	3.00
0	1	3.75
1	0	4.50
1	1	6.00

Table 2. FT3001MPX Truth Table

DSR0	Reset Time (±20%) in Seconds
0	3.0
1	4.5

The two CMOS input pins, /SR0 and /SR1, control the reset function. A low input signal on both /SR0 and /SR1 starts the oscillator. Both /SR0 and /SR1 pins must be held LOW for time *n* before the /RST1 and RST2 outputs are activated. The TRIG pin should be tied LOW during normal operation. The TRIG pin is used for SCAN testing.

Application Information

IMPORTANT: The DSR0 and DSR1 pins must be tied directly to V_{CC} or GND to provide a HIGH or LOW voltage level. The voltage level on the DSR pin determines the length of the configurable delay. The voltage level on the DSR pins must not change during normal operation. Do not use pull-up or pull-down resistors on DSR pins.

Short Duration (Button Press Time < *n*)

In this case, both input /SR0 and /SR1 are LOW for a duration (t_W) that is shorter than time *n*. When an input goes LOW, the internal timer starts counting. If the input goes HIGH before time *n*, the timer stops counting and resets and no changes occur on the outputs.

Long Duration (t_W > *n*)

In this case, both input /SR0 and /SR1 are LOW for a duration (t_W) that is longer than time *n*. When an input goes LOW, the internal timer starts counting.

After time *n*, the outputs switch and the timer stops counting. After time t_{REC}, the outputs return to their original states.

Table 3. Short Duration

/SR0	/SR1	/RST1	RST2	Description
⎍	L	H	L	The timer starts counting when both inputs go LOW. The timer stops counting and resets when either input goes high. No changes occur on the outputs. Both /SR0 and /SR1 need to be LOW to activate (start) the timer.

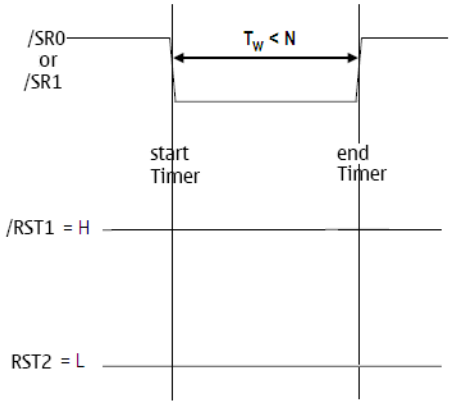

Figure 8. Short Duration

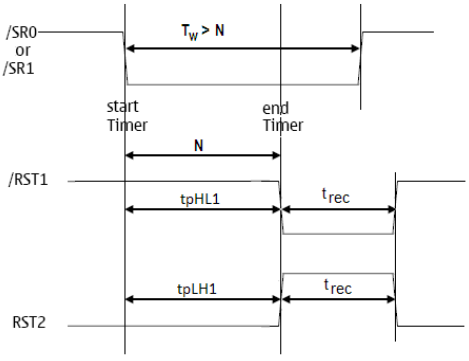

Figure 9. Long Duration

Table 4. Long Duration

/SR0	/SR1	/RST1	RST2	Description
⎍	L	⎍	⎍	The timer starts counting when both inputs go LOW. After time *n*, the outputs switch. After time t_{REC}, the outputs return to their original states. Both /SR0 and /SR1 need to be LOW to activate (start) the timer.
L	⎍	⎍	⎍	

Physical Dimensions

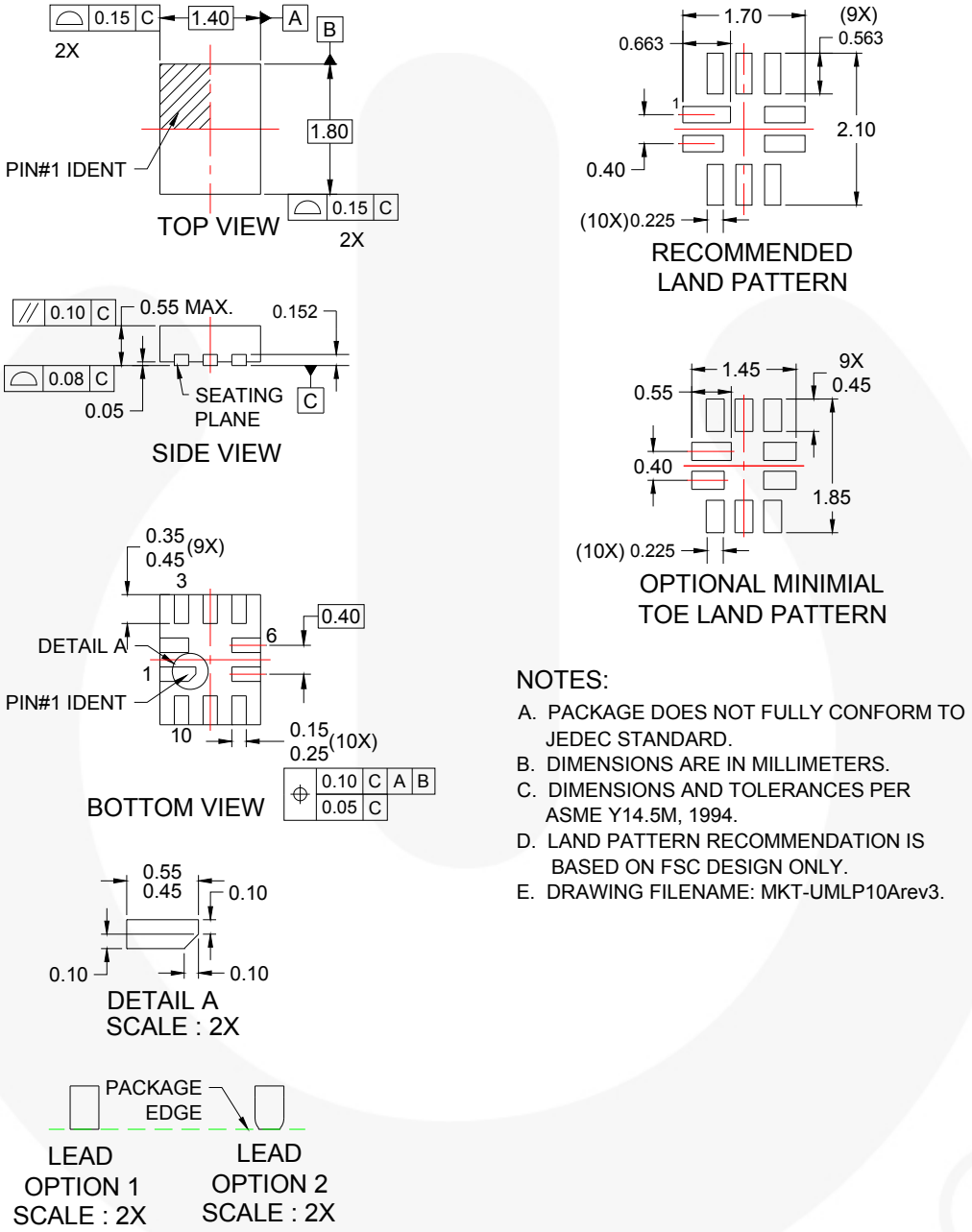

Figure 10. 10-Lead, Ultrathin MLP, 1.4 x 1.8 x 0.55 mm Package, 0.40 mm Pitch

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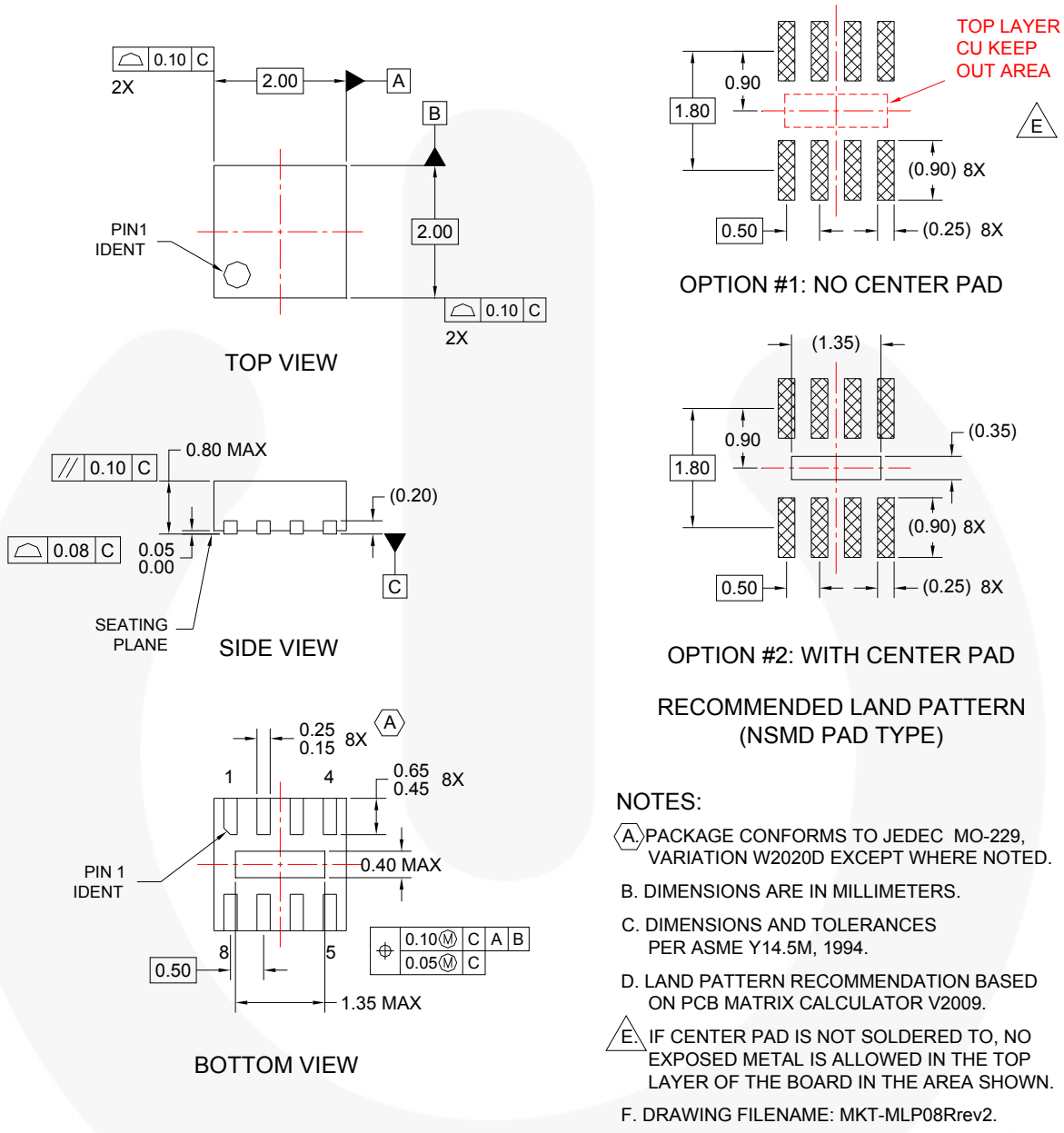
Physical Dimensions (Continued)



NOTES:

A. PACKAGE CONFORMS TO JEDEC MO-229, VARIATION W2020D EXCEPT WHERE NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. LAND PATTERN RECOMMENDATION BASED ON PCB MATRIX CALCULATOR V2009.

E. IF CENTER PAD IS NOT SOLDERED TO, NO EXPOSED METAL IS ALLOWED IN THE TOP LAYER OF THE BOARD IN THE AREA SHOWN.

F. DRAWING FILENAME: MKT-MLP08Rrev2.

Figure 11. 8-Lead, Molded Leadless Package (MLP), Dual JEDEC, MO-229 2.0 x 2.0 mm

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