

FDS7064SN3

30V N-Channel PowerTrench® SyncFET™

General Description

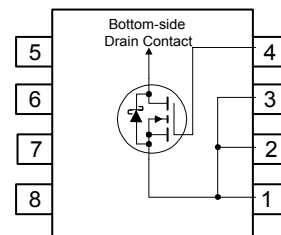
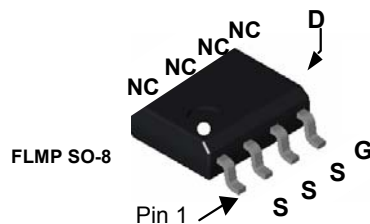
The FDS7064SN3 is designed to improve the efficiency of Buck Regulators. Used as the Synchronous rectifier, (Low side MOSFET), losses can be reduced, not only in this device, but also in the Control switch, (High side MOSFET). After the low side MOSFET turns off, reverse recovery current in the body diode is dissipated in the High Side device. A Discrete Schottky diode in parallel with the Low Side MOSFET can lower the reverse recovery current, but parasitic PCB and Package Inductance reduce the effectiveness of the Schottky. SyncFET™ technology reduces this inductance to a minimum by providing a monolithic solution (MOSFET and Schottky in the same die), resulting in optimum performance.

Applications

- Synchronous Rectifier

• Features

- 16 A, 30 V $R_{DS(ON)} = 8.0 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 9.5 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- High performance trench technology for extremely low $R_{DS(ON)}$
- No inductance between MOSFET and Schottky
- 40% reduction in Body Diode Forward Voltage
- Optimized to reduce losses in Synchronous Buck Regulators
- FLMP SO-8 package for enhanced thermal performance.



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	30	V
V _{GSS}	Gate-Source Voltage	±16	V
I _D	Drain Current – Continuous (Note 1a)	16	A
	– Pulsed	60	
P _D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	3.13	W
		1.5	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	0.5	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS7064SN3	FDS7064SN3	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C		26		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			500	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	1	1.4	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C		–2		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 16\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 14\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 16\text{ A}, T_J = 125^\circ\text{C}$		6.5 7.5 9.1	8.0 9.5 11.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 16\text{ A}$		70		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2800		pF
C_{oss}	Output Capacitance			530		pF
C_{rss}	Reverse Transfer Capacitance			190		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.4		Ω

Switching Characteristics (Note 2)

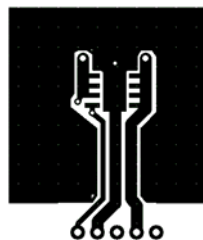
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		11	20	ns
t_r	Turn–On Rise Time			20	22	ns
$t_{d(off)}$	Turn–Off Delay Time			50	80	ns
t_f	Turn–Off Fall Time			18	33	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 16\text{ A},$ $V_{GS} = 5.0\text{ V}$		25	35	nC
Q_{gs}	Gate–Source Charge			6		nC
Q_{gd}	Gate–Drain Charge			6		nC

Drain–Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain–Source Schottky Diode Forward Current				4.3	A
V _{SD}	Drain–Source Schottky Diode Forward Voltage	V _{GS} = 0 V, I _S = 4.3 A (Note 2)		0.4	0.7	V
t _{RR}	Reverse Recovery Time	I _F = 16 A dI _F /dt = 300 A/us		22		ns
Q _{RR}	Reverse Recovery Charge			20		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 40°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 85°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

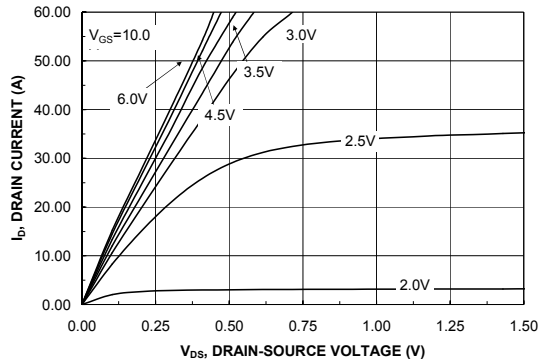


Figure 1. On-Region Characteristics.

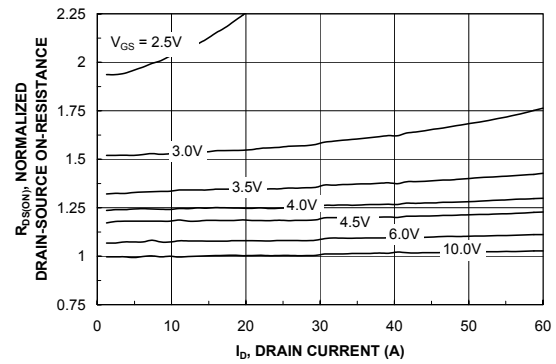


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

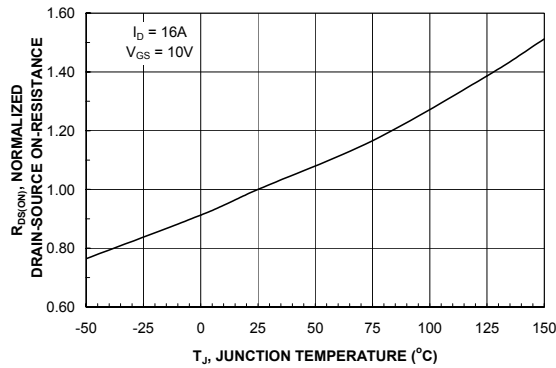


Figure 3. On-Resistance Variation with Temperature.

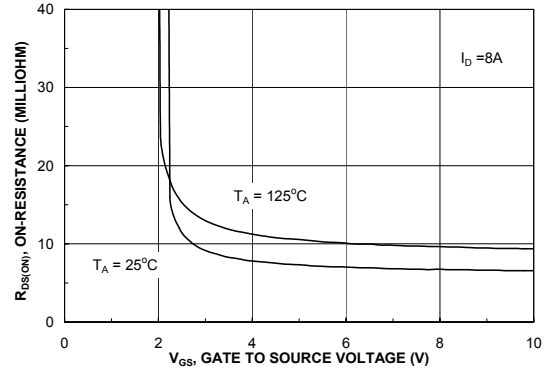


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

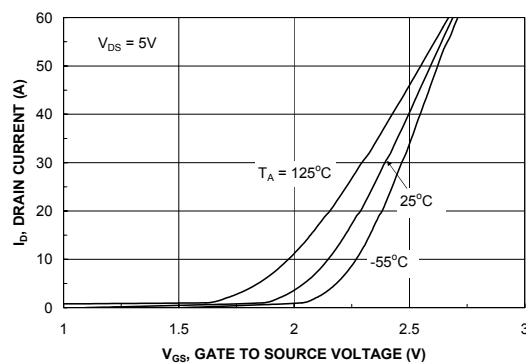


Figure 5. Transfer Characteristics.

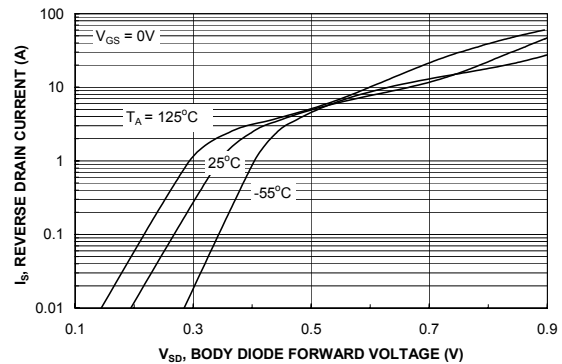


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

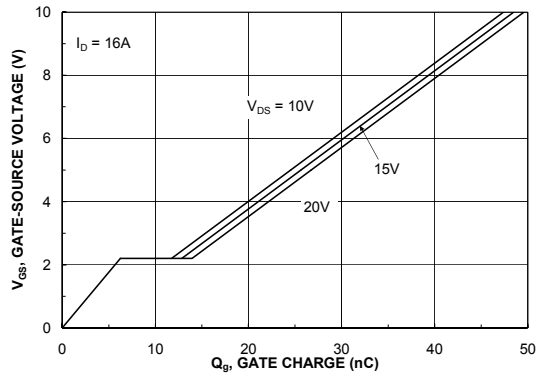


Figure 7. Gate Charge Characteristics.

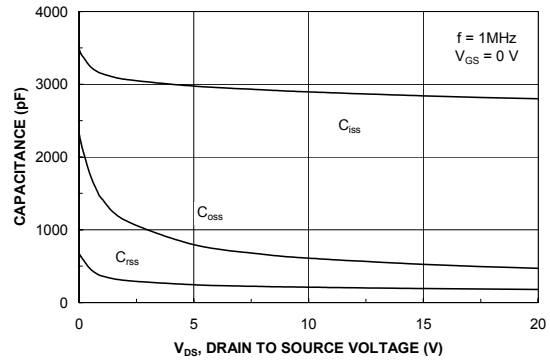


Figure 8. Capacitance Characteristics.

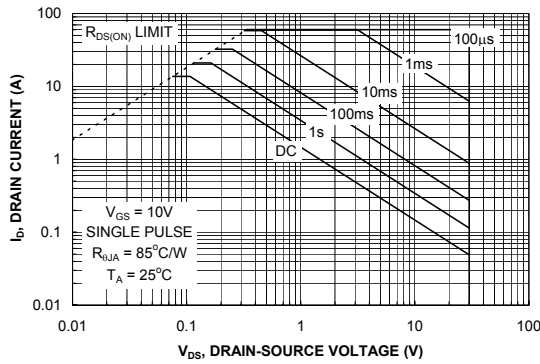


Figure 9. Maximum Safe Operating Area.

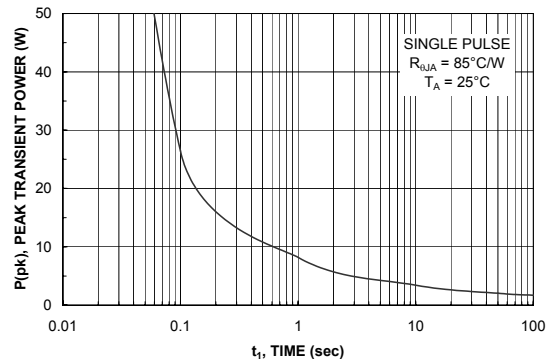


Figure 10. Single Pulse Maximum Power Dissipation.

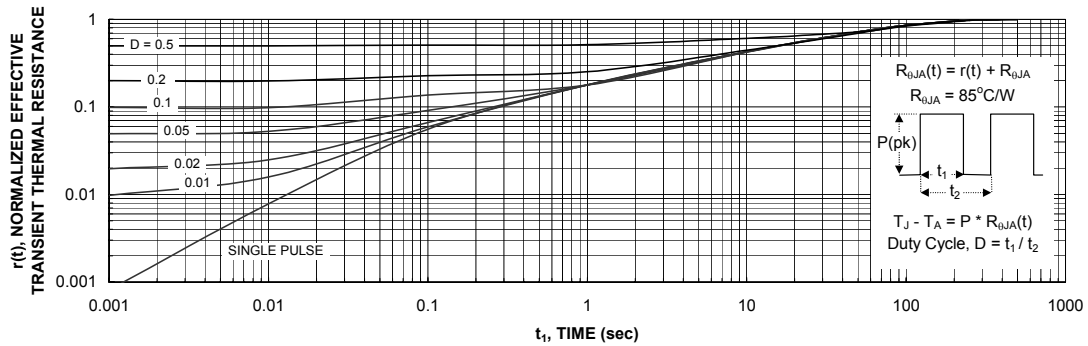


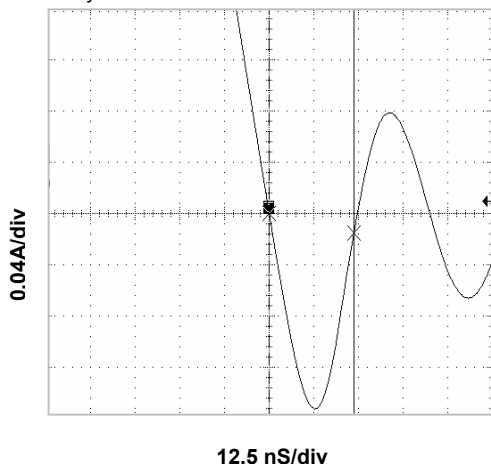
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics (continued)

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDS7064SN3.



Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

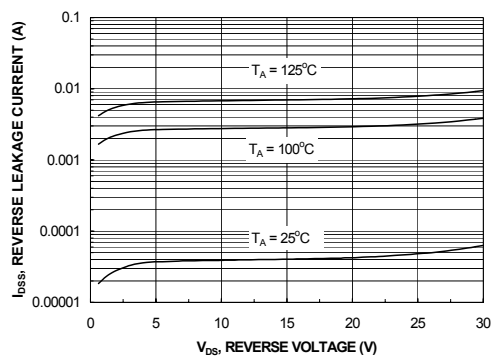
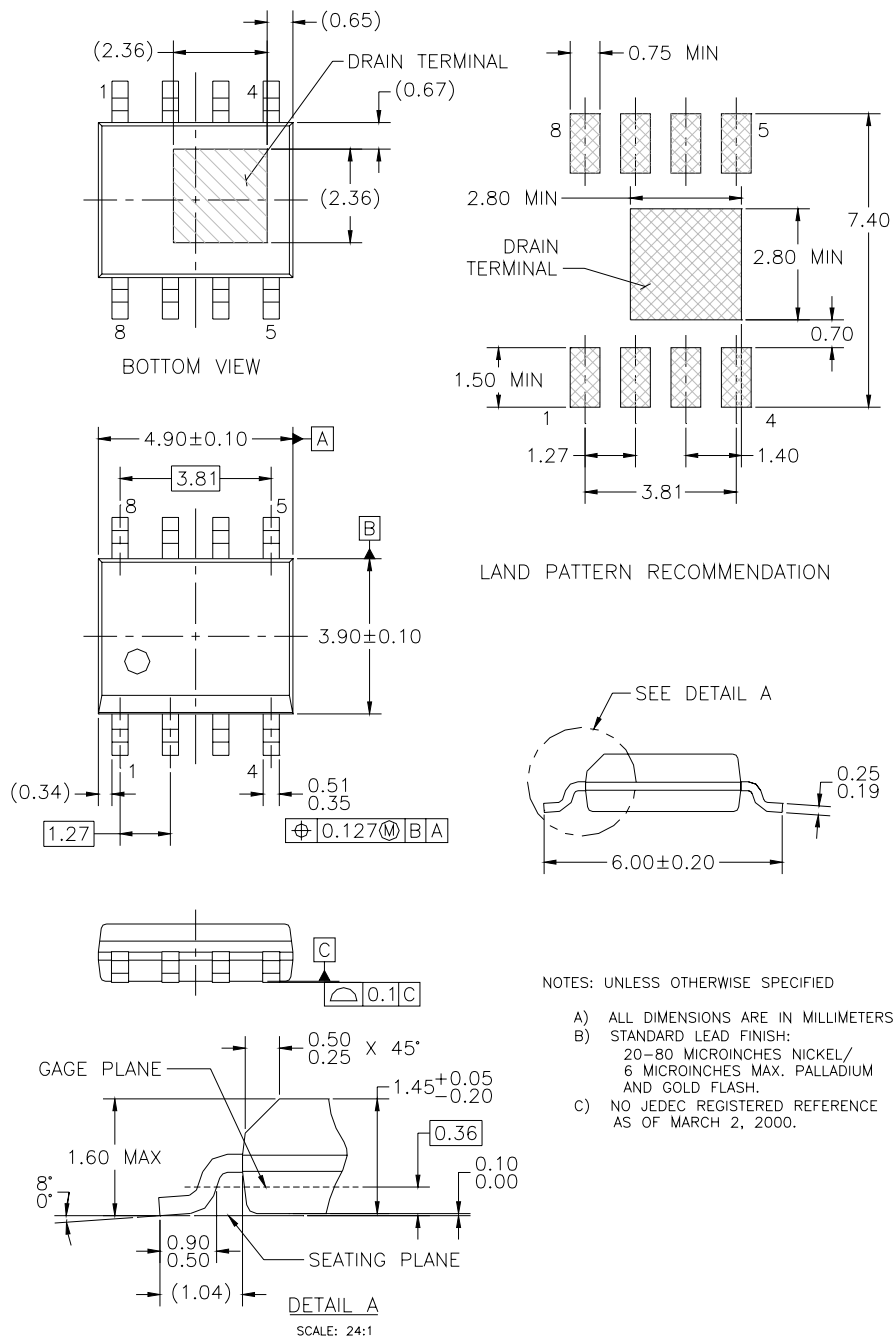


Figure 13. SyncFET body diode reverse leakage versus drain-source voltage and temperature

Dimensional Outline and Pad Layout



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