

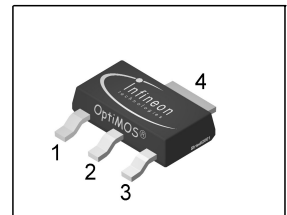
OptiMOS® Power-Transistor
Feature

- N-Channel
- Enhancement mode
- Logic Level

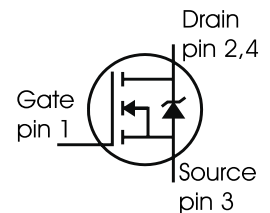
Product Summary

V_{DS}	55	V
$R_{DS(on)}$	90	mΩ
I_D	2.8	A

SOT 223



Type	Package	Ordering Code	Marking
BSP615S2L	SOT 223	Q67060-S7211	2N615L


Maximum Ratings, at $T_j = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current	I_D		A
$T_A = 25\text{ °C}$		2.8	
$T_A = 70\text{ °C}$		2.3	
Pulsed drain current	$I_{D\text{ puls}}$	11	
$T_A = 25\text{ °C}$			
Gate source voltage	V_{GS}	± 20	V
Power dissipation	P_{tot}	1.8	W
$T_A = 25\text{ °C}$			
Operating and storage temperature	T_j, T_{stg}	-55... +150	°C
IEC climatic category; DIN IEC 68-1		55/150/00	

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - soldering point (Pin 4)	R_{thJS}	-	19	23	K/W
Thermal resistance, chip to ambient air:	R_{thJA}				
@ min. footprint		-	-	120	
@ 6 cm ² cooling area ¹⁾		-	-	70	

Electrical Characteristics, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$	$V_{(BR)DSS}$	55	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D=12\mu A$	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current $V_{DS}=55V, V_{GS}=0V, T_j=25^{\circ}C$ $V_{DS}=55V, V_{GS}=0V, T_j=125^{\circ}C$	I_{DSS}	- -	0.1 10	1 100	μA
Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$	I_{GSS}	-	10	100	
Drain-source on-state resistance $V_{GS}=4.5V, I_D=1.4A$	$R_{DS(on)}$	-	86	150	m Ω
Drain-source on-state resistance $V_{GS}=10V, I_D=1.4A$	$R_{DS(on)}$	-	67	90	

¹⁾ Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic Characteristics

Transconductance	g_{fs}	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$, $I_D = 2.3A$	2.7	5.4	-	S
Input capacitance	C_{iss}	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1MHz$	-	249	330	pF
Output capacitance	C_{oss}		-	58	78	
Reverse transfer capacitance	C_{rss}		-	22	33	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30V$, $V_{GS} = 4.5V$, $I_D = 2.8A$, $R_G = 24\Omega$	-	7.8	12	ns
Rise time	t_r		-	24	36	
Turn-off delay time	$t_{d(off)}$		-	22	33	
Fall time	t_f		-	23	34	

Gate Charge Characteristics

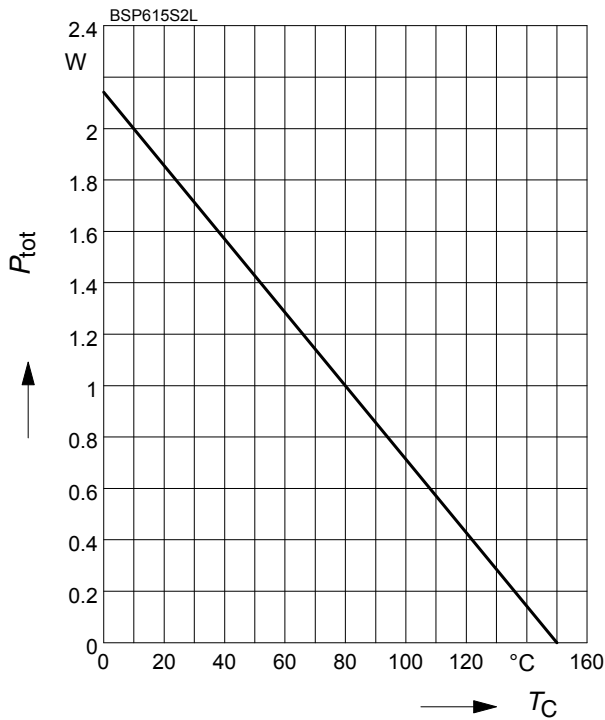
Gate to source charge	Q_{gs}	$V_{DD} = 40V$, $I_D = 2.8A$	-	0.8	1.1	nC
Gate to drain charge	Q_{gd}		-	2.5	3.8	
Gate charge total	Q_g	$V_{DD} = 40V$, $I_D = 2.8A$, $V_{GS} = 0$ to $10V$	-	7.5	10	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 40V$, $I_D = 2.8A$	-	3	-	V

Reverse Diode

Inverse diode continuous forward current	I_S	$T_A = 25^\circ C$	-	-	2.8	A
Inv. diode direct current, pulsed	I_{SM}		-	-	11	
Inverse diode forward voltage	V_{SD}	$V_{GS} = 0V$, $I_F = 2.8A$	-	0.8	1.1	V
Reverse recovery time	t_{rr}	$V_R = 30V$, $I_F = I_S$, $di_F/dt = 100A/\mu s$	-	30	38	ns
Reverse recovery charge	Q_{rr}		-	30	38	nC

1 Power dissipation

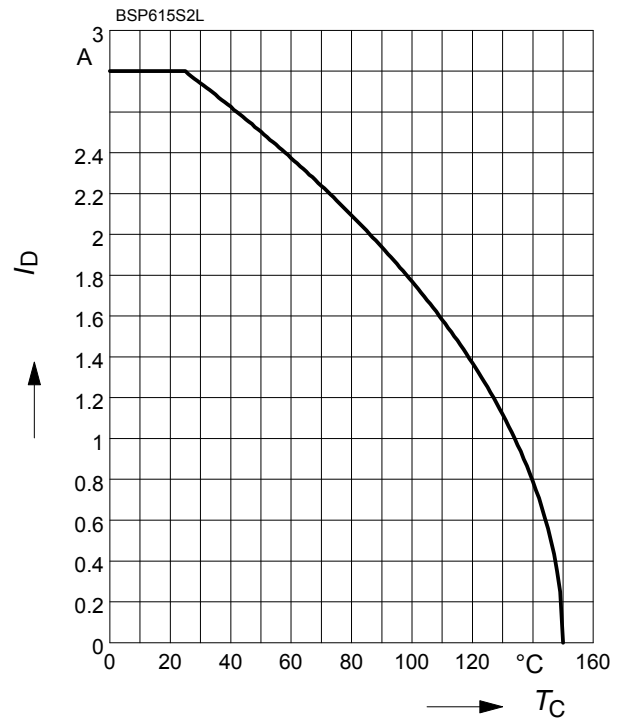
$$P_{\text{tot}} = f(T_C)$$



2 Drain current

$$I_D = f(T_C)$$

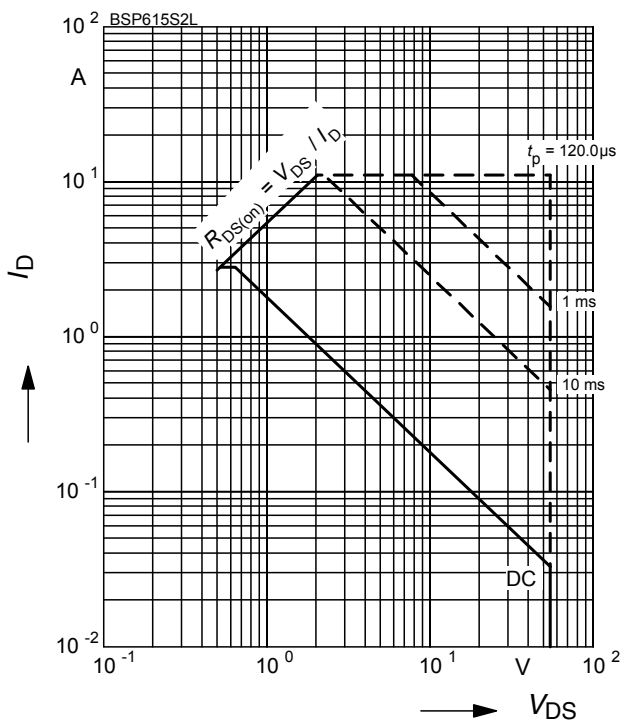
parameter: $V_{GS} \geq 10 \text{ V}$



3 Safe operating area

$$I_D = f(V_{DS})$$

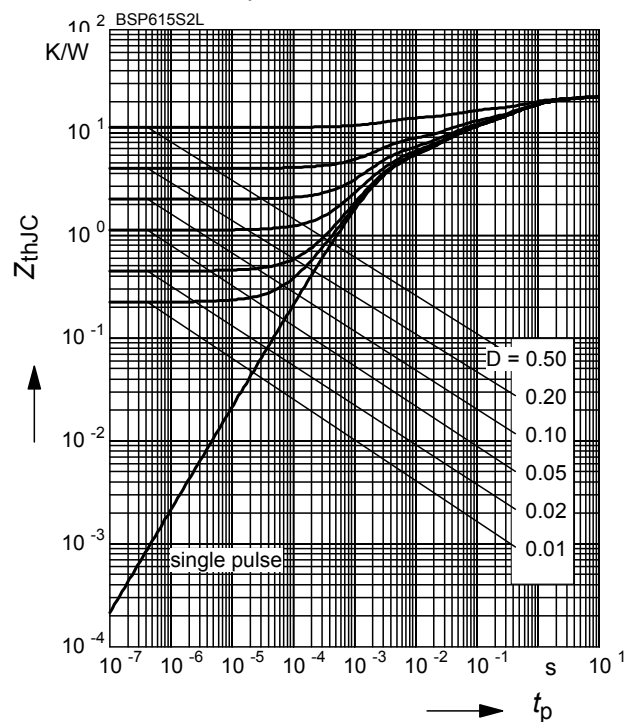
parameter: $D = 0$, $T_C = --$



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

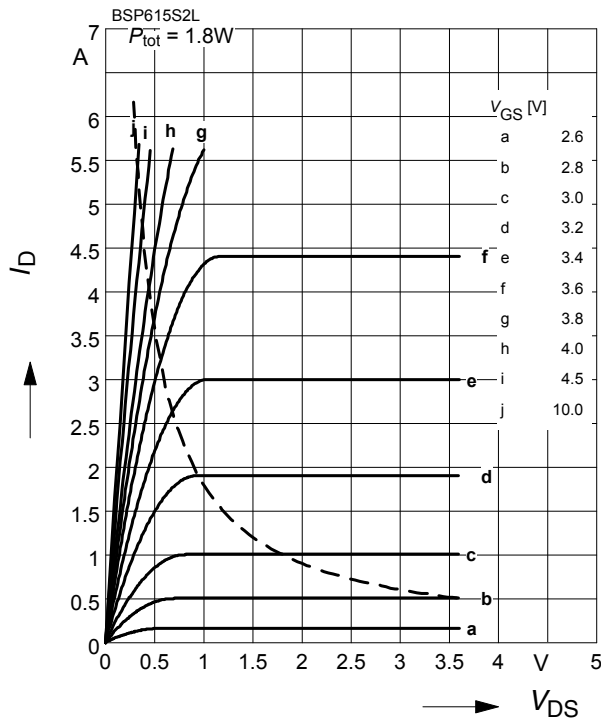
parameter: $D = t_p / T$



5 Typ. output characteristic

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

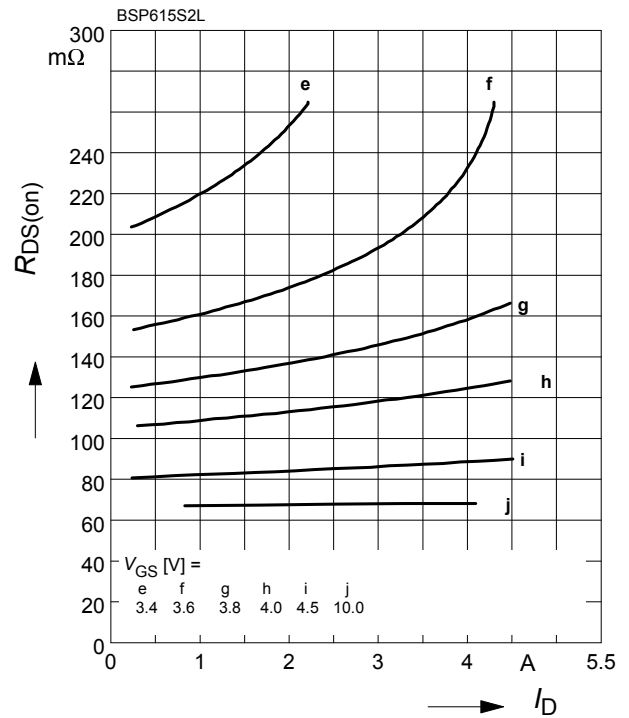
parameter: $t_p = 80 \mu\text{s}$



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D)$$

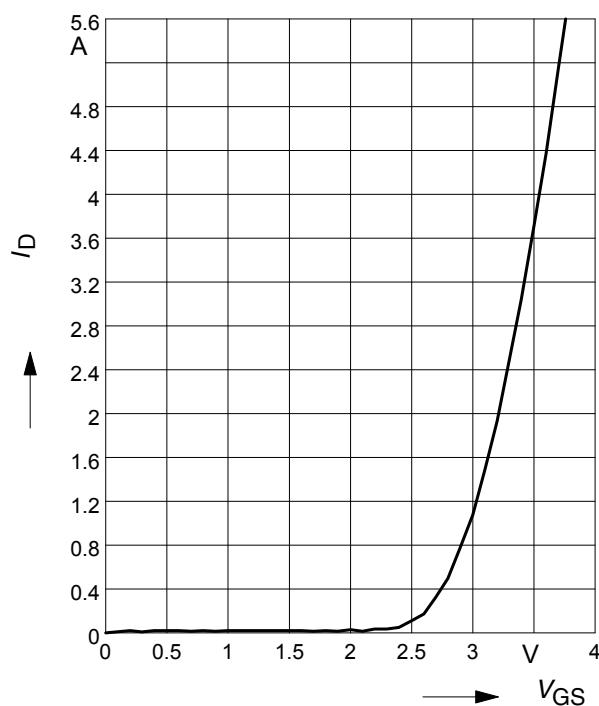
parameter: V_{GS}



7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$$

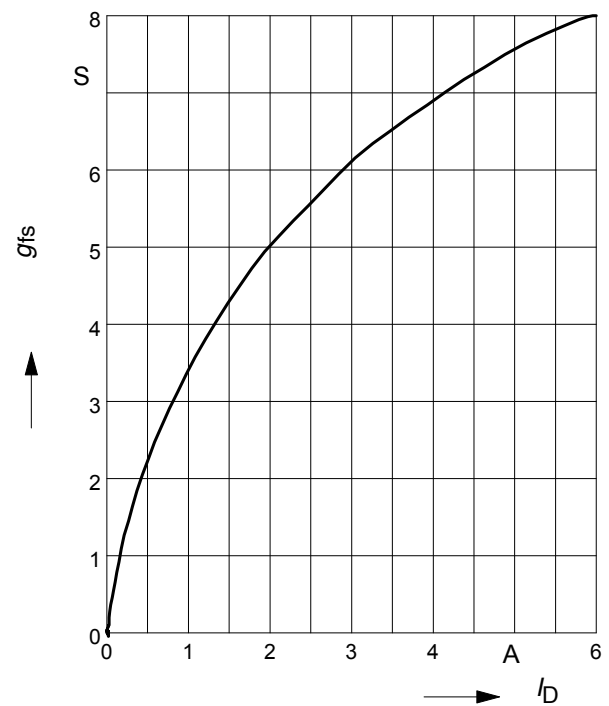
parameter: $t_p = 80 \mu\text{s}$



8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$

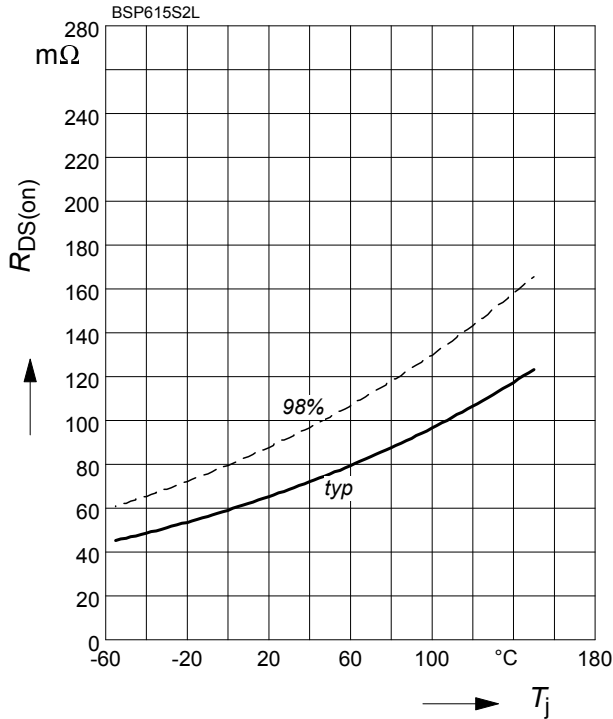
parameter: g_{fs}



9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

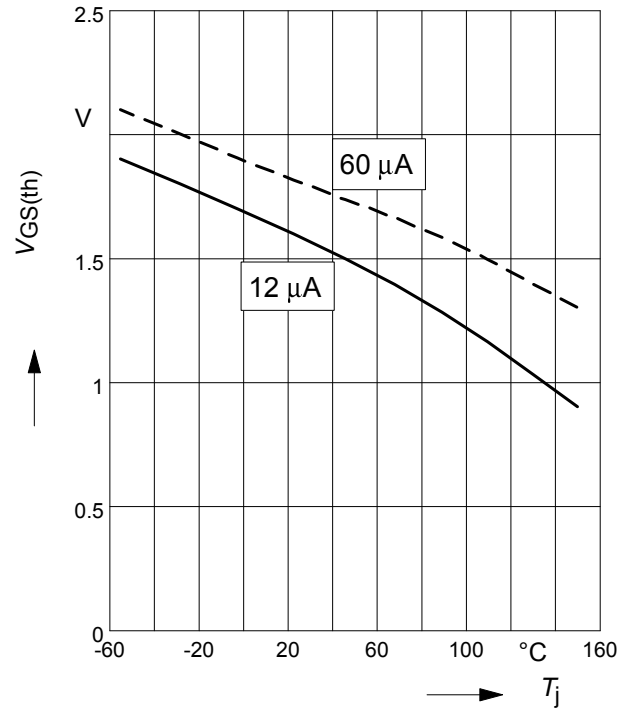
parameter: $I_D = 1.4 \text{ A}$, $V_{GS} = 10 \text{ V}$



10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j)$$

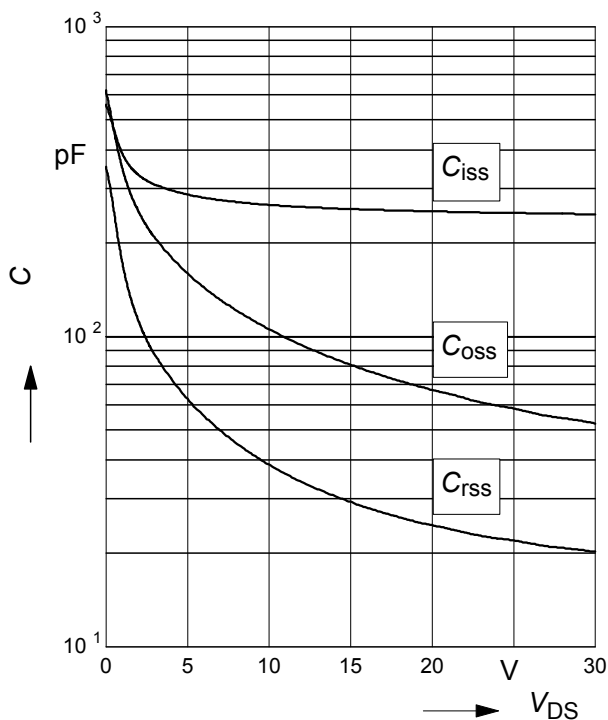
parameter: $V_{GS} = V_{DS}$



11 Typ. capacitances

$$C = f(V_{DS})$$

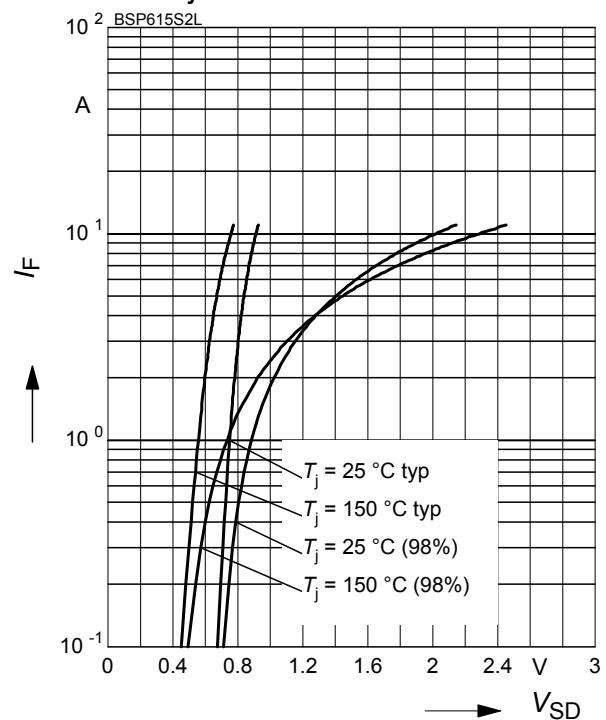
parameter: $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$



12 Forward character. of reverse diode

$$I_F = f(V_{SD})$$

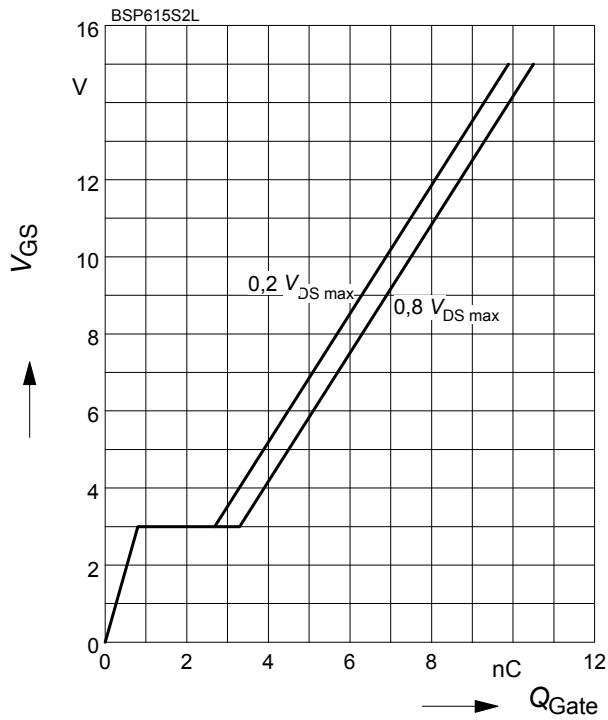
parameter: T_j , $t_p = 80 \mu\text{s}$



13 Typ. gate charge

$$V_{GS} = f(Q_{Gate})$$

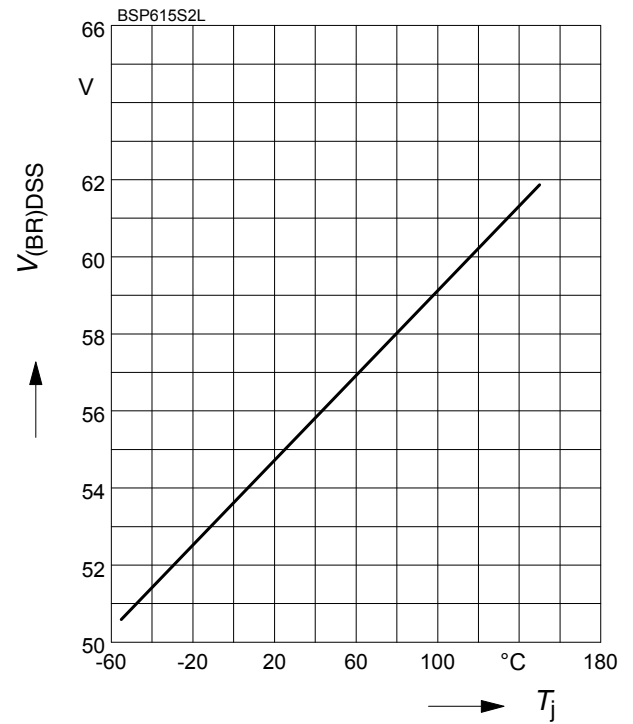
parameter: $I_D = 2.8 \text{ A}$ pulsed



14 Drain-source breakdown voltage

$$V_{(BR)DSS} = f(T_j)$$

parameter: $I_D = 10 \text{ mA}$



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Attention please!

Maximum soldering conditions: Maximum 3 times IR profile acc. to IPC 9501 (235°C +5/-0)

Jedec level 3

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