OptiMOS™3 Power-Transistor

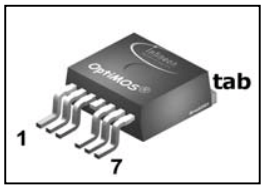
Features

- MOSFET for ORing and Uninterruptible Power Supply
- Qualified according to JEDEC[1] for target applications
- N-channel
- Normal level
- Ultra-low on-resistance $R_{DS(on)}$
- 100% Avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

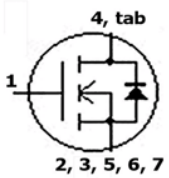
Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	2.0	mΩ
I_D	140	A

PG-TO263-7



RoHS Halogen-Free



Type	Package	Marking
IPB020N04N G	PG-TO263-7	020N04N

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	140	A
		V_{GS}=10 V, T_C=100 °C	140	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	980	
Avalanche current, single pulse[3]	I_{AS}	T_C=25 °C	100	
Avalanche energy, single pulse	E_{AS}	I_D=100 A, R_{GS}=25 Ω	140	mJ
Gate source voltage	V_{GS}		±20	V

[1] J-STD20 and JESD22

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	167	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.9	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm² cooling area[4)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=95 µA	2	-	4	
Zero gate voltage drain current	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=100 A	-	1.7	2	mΩ
Gate resistance	R_G		-	2.1	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=100 A	85	170	-	S

[2)] See figure 3 for more detailed information

[3)] See figure 13 for more detailed information

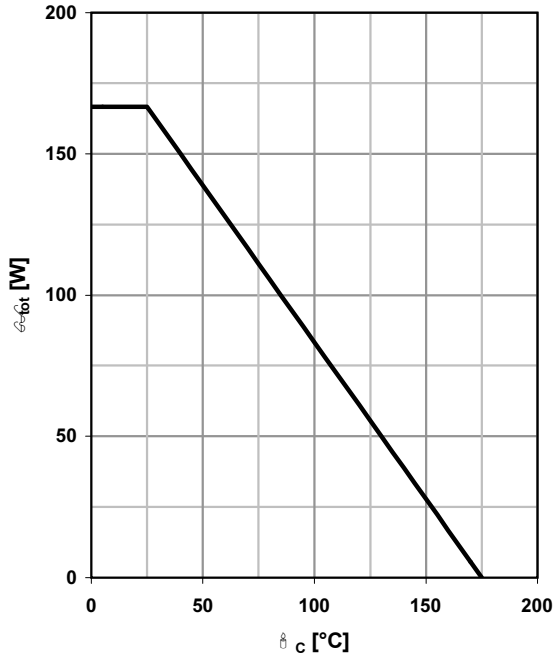
[4)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz	-	7300	9700	pF
Output capacitance	C_{oss}		-	2000	2700	
Reverse transfer capacitance	C_{rss}		-	77	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω	-	27	-	ns
Rise time	t_r		-	6.4	-	
Turn-off delay time	$t_{d(off)}$		-	40	-	
Fall time	t_f		-	7.8	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=20 V, I_D=30 A, V_{GS}=0 to 10 V	-	35	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	22	-	
Gate to drain charge	Q_{gd}		-	11	-	
Switching charge	Q_{sw}		-	24	-	
Gate charge total	Q_g		-	90	120	
Gate plateau voltage	$V_{plateau}$		-	4.8	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 10 V	-	85	-	
Output charge	Q_{oss}	V_{DD}=20 V, V_{GS}=0 V	-	73	-	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	139	A
Diode pulse current	$I_{S,pulse}$		-	-	980	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	-	0.91	1.2	V
Reverse recovery charge	Q_{rr}	V_R=20 V, I_F=I_S, di_F/dt =400 A/µs	-	88	-	nC

[5)] See figure 16 for gate charge parameter definition

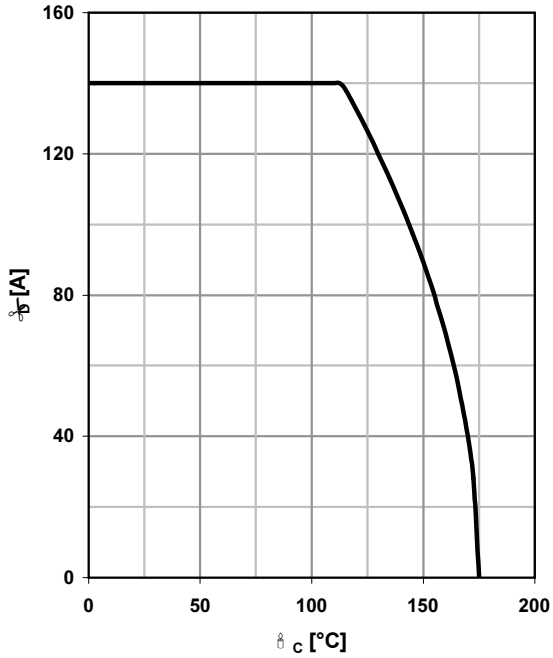
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

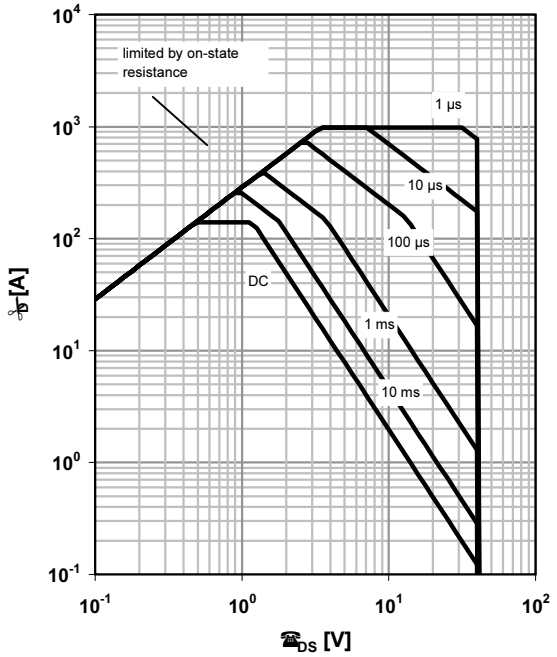
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

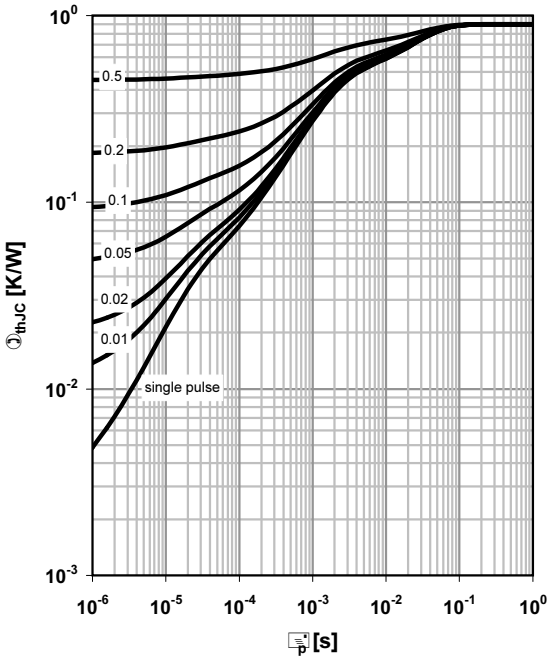
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

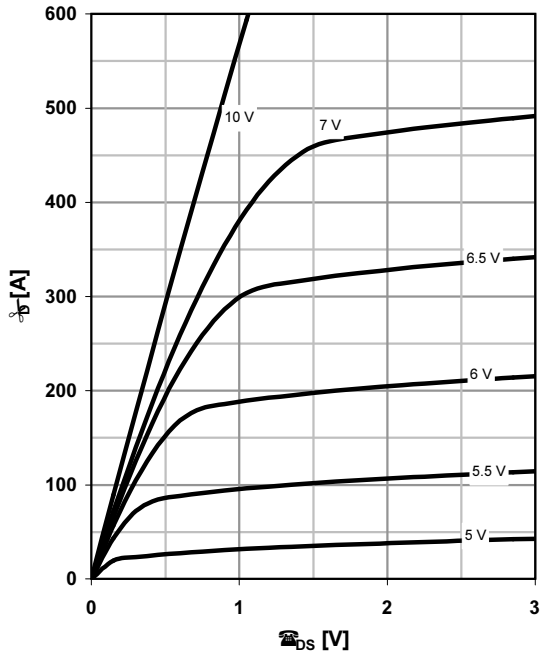
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

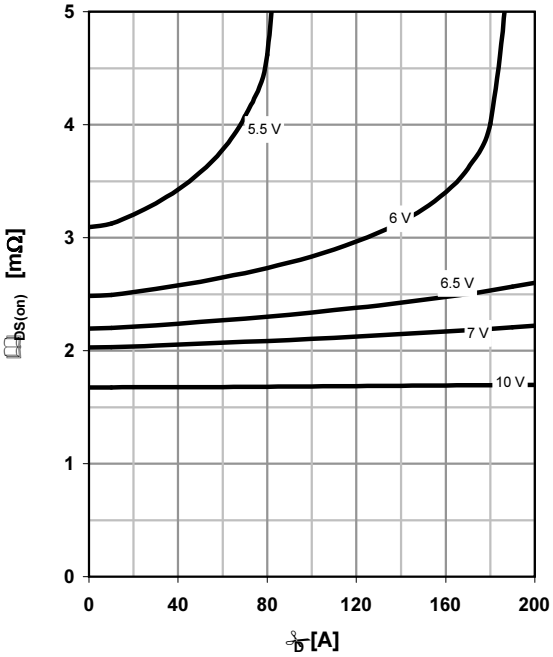
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

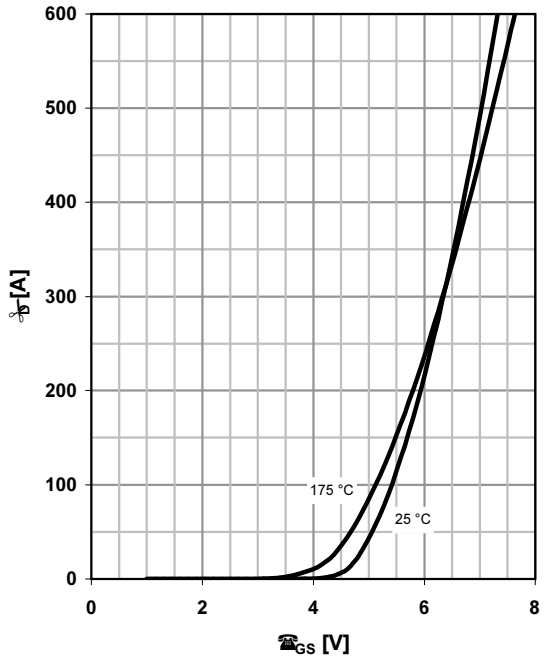
parameter: V_{GS}



7 Typ. transfer characteristics

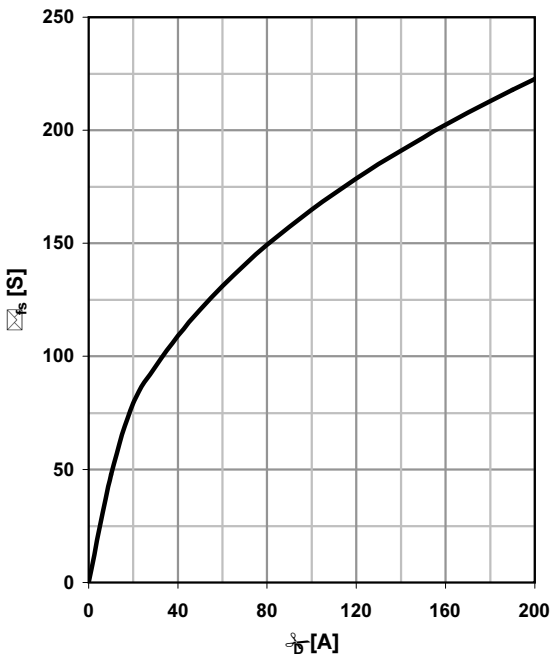
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



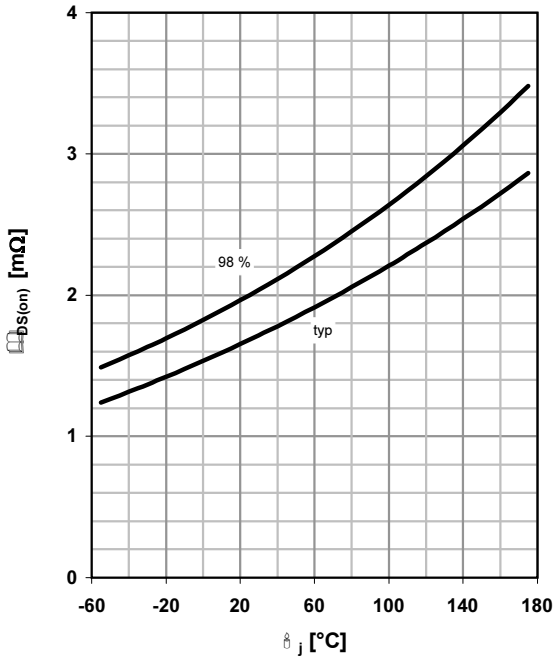
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



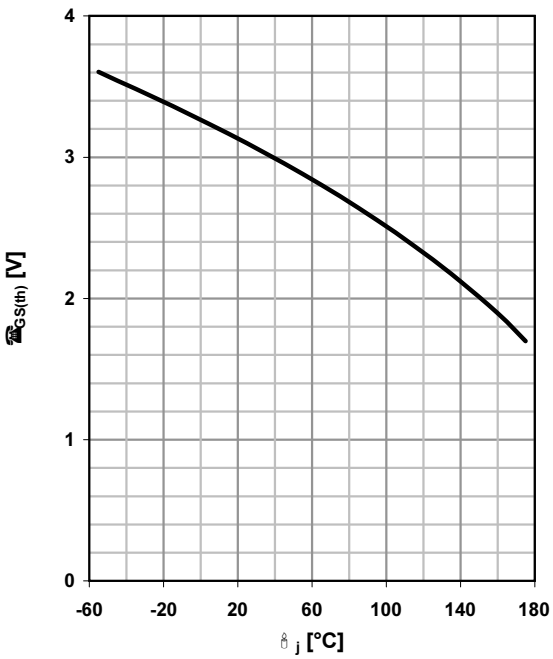
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_j)$; $I_D=100$ A; $V_{GS}=10$ V



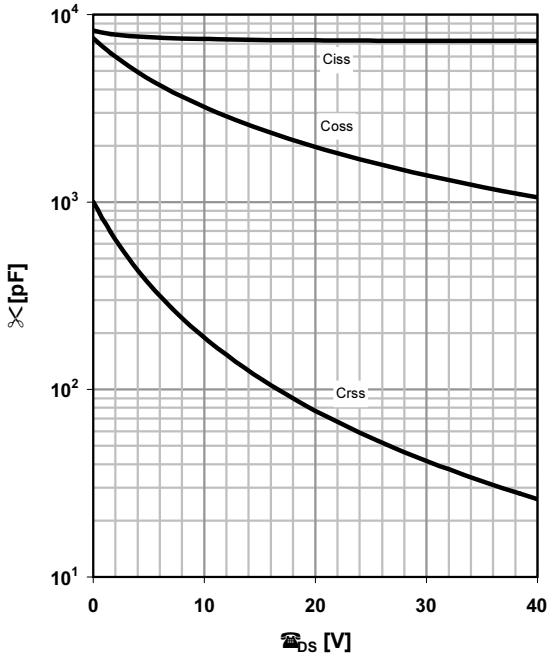
10 Typ. gate threshold voltage

$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; $I_D=250$ µA



11 Typ. capacitances

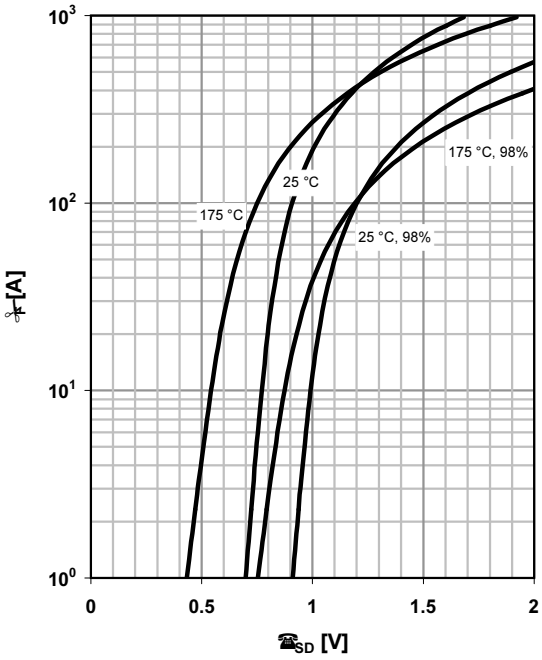
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

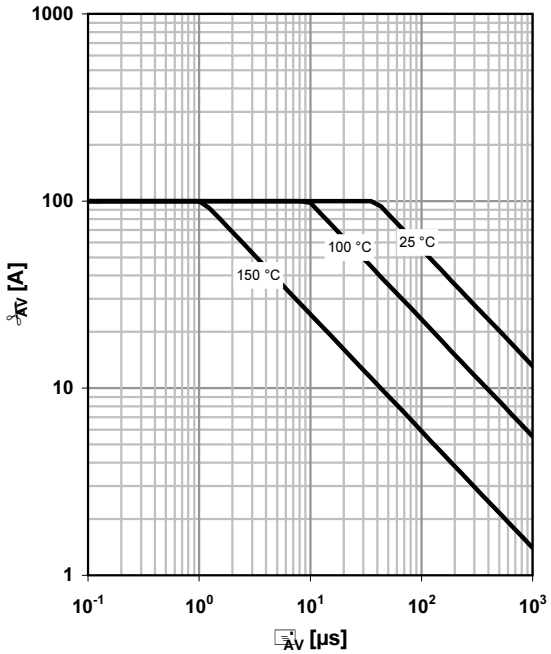
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

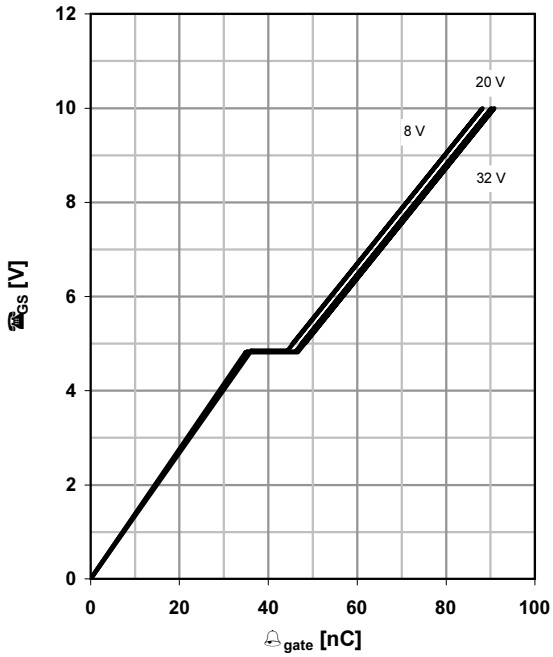
parameter: $T_{j(start)}$



14 Typ. gate charge

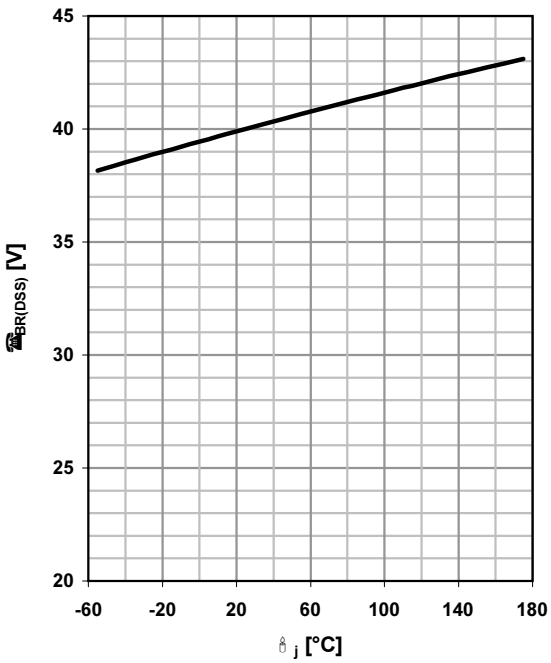
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

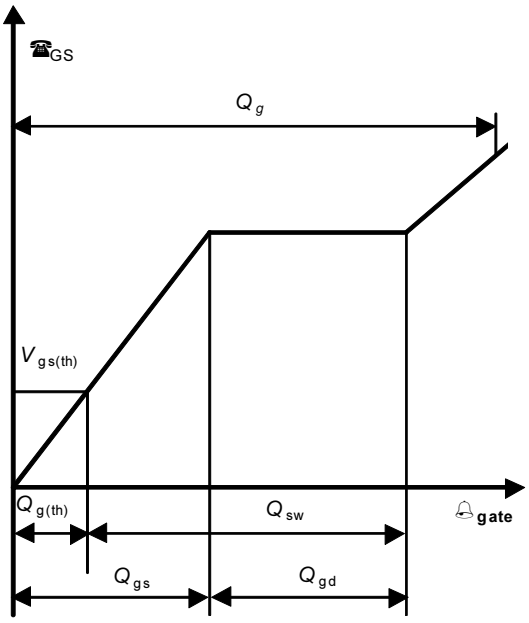


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

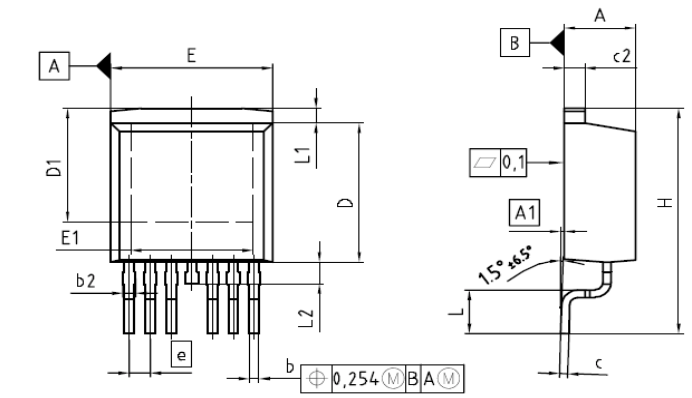


16 Gate charge waveforms

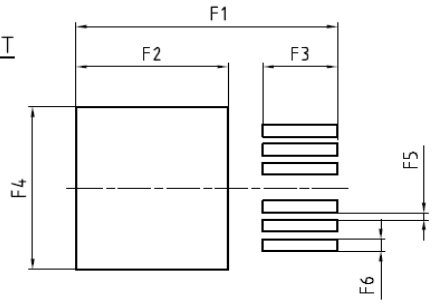


Package Outline **PG-TO263-7**

TO263-7-2 / TO263-7-3 / TO263-7-5 / TO263-7-7



FOOTPRINT

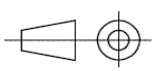


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0,50	0,70	0,020	0,028
b2	0.50	1.00	0.020	0.039
c	0.33	0.65	0.013	0.026
c2	1,17	1,40	0.046	0,055
D	8.51	9.45	0.335	0.372
D1	6.90	7.90	0.272	0.311
E	9,80	10,31	0,386	0,406
E1	6.50	8.60	0.256	0.339
e	1.27		0.050	
N	6		6	
H	14.61	15.88	0.575	0.625
L	2,29	3,00	0,090	0,118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16,05	16,25	0.632	0,640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10,70	10,90	0.421	0,429
F5	0.37	0.57	0.015	0.022
F6	0.70	0.90	0.028	0.035

DOCUMENT NO.
Z8B00134765

SCALE 0 5 5 7.5mm

EUROPEAN PROJECTION



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