

## N-channel 600 V, 0.350 $\Omega$ typ., 8 A MDmesh™ DM2 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data

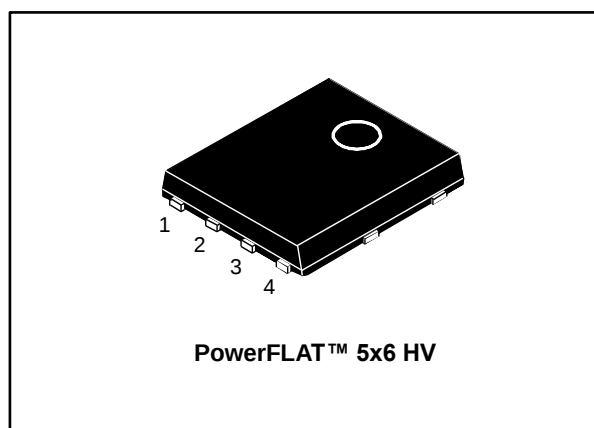
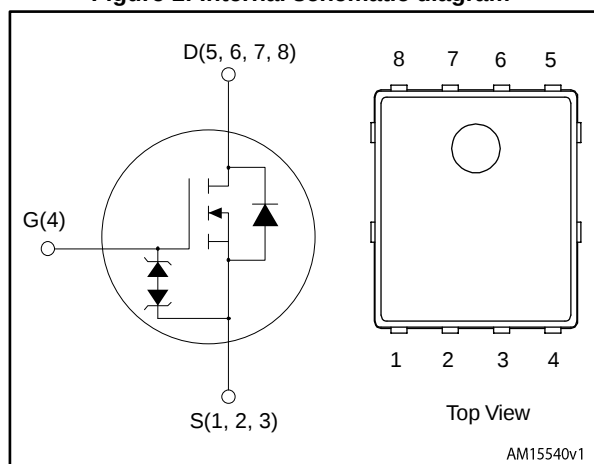


Figure 1: Internal schematic diagram



### Features

| Order code  | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|-------------|-----------------|--------------------------|----------------|
| STL13N60DM2 | 600 V           | 0.370 $\Omega$           | 8 A            |

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

| Order code  | Marking  | Package           | Packing       |
|-------------|----------|-------------------|---------------|
| STL13N60DM2 | 13N60DM2 | PowerFLAT™ 5x6 HV | Tape and reel |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol                  | Parameter                                                         | Value            | Unit               |
|-------------------------|-------------------------------------------------------------------|------------------|--------------------|
| $V_{GS}$                | Gate-source voltage                                               | $\pm 25$         | V                  |
| $I_D$                   | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 8 <sup>(1)</sup> | A                  |
| $I_D$                   | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 5                | A                  |
| $I_{DM}$ <sup>(2)</sup> | Drain current (pulsed)                                            | 32               | A                  |
| $P_{TOT}$               | Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$           | 52               | W                  |
| $dv/dt$ <sup>(3)</sup>  | Peak diode recovery voltage slope                                 | 40               | V/ns               |
| $dv/dt$ <sup>(4)</sup>  | MOSFET $dv/dt$ ruggedness                                         | 50               | V/ns               |
| $T_{stg}$               | Storage temperature range                                         | - 55 to 150      | $^{\circ}\text{C}$ |
| $T_j$                   | Operating junction temperature range                              | 150              |                    |

**Notes:**

<sup>(1)</sup>The value is limited by package.

<sup>(2)</sup>Pulse width limited by safe operating area.

<sup>(3)</sup> $I_{SD} \leq 8\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$

<sup>(4)</sup> $V_{DS} \leq 480\text{ V}$

Table 3: Thermal data

| Symbol         | Parameter                                          | Value | Unit                        |
|----------------|----------------------------------------------------|-------|-----------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max               | 2.40  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-pcb}$  | Thermal resistance junction-pcb max <sup>(1)</sup> | 59    | $^{\circ}\text{C}/\text{W}$ |

**Notes:**

<sup>(1)</sup>When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

Table 4: Avalanche characteristics

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetetive or not repetetive (pulse width limited by $T_{jmax}$ )                                   | 2.5   | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 340   | mJ   |

## 2 Electrical characteristics

(T<sub>C</sub> = 25 °C unless otherwise specified)

Table 5: On/off states

| Symbol               | Parameter                         | Test conditions                                                                        | Min. | Typ.  | Max.  | Unit |
|----------------------|-----------------------------------|----------------------------------------------------------------------------------------|------|-------|-------|------|
| V <sub>(BR)DSS</sub> | Drain-source breakdown voltage    | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA                                           | 600  |       |       | V    |
| I <sub>DSS</sub>     | Zero gate voltage Drain current   | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V                                         |      |       | 1.5   | μA   |
|                      |                                   | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V, T <sub>C</sub> = 125 °C <sup>(1)</sup> |      |       | 100   | μA   |
| I <sub>GSS</sub>     | Gate-body leakage current         | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V                                         |      |       | ±10   | μA   |
| V <sub>GS(th)</sub>  | Gate threshold voltage            | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA                            | 3    | 4     | 5     | V    |
| R <sub>DS(on)</sub>  | Static drain-source on-resistance | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A                                           |      | 0.350 | 0.370 | Ω    |

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

Table 6: Dynamic

| Symbol                              | Parameter                     | Test conditions                                                                                                                                  | Min. | Typ. | Max. | Unit |
|-------------------------------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| C <sub>iss</sub>                    | Input capacitance             | V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0 V                                                                                        | -    | 730  | -    | pF   |
| C <sub>oss</sub>                    | Output capacitance            |                                                                                                                                                  | -    | 38   | -    | pF   |
| C <sub>rss</sub>                    | Reverse transfer capacitance  |                                                                                                                                                  | -    | 0.9  | -    | pF   |
| C <sub>oss eq.</sub> <sup>(1)</sup> | Equivalent output capacitance | V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V                                                                                            | -    | 70   | -    | pF   |
| R <sub>G</sub>                      | Intrinsic gate resistance     | f = 1 MHz, I <sub>D</sub> = 0 A                                                                                                                  | -    | 5.1  | -    | Ω    |
| Q <sub>g</sub>                      | Total gate charge             | V <sub>DD</sub> = 480 V, I <sub>D</sub> = 11 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> ) | -    | 19   | -    | nC   |
| Q <sub>gs</sub>                     | Gate-source charge            |                                                                                                                                                  | -    | 4.4  | -    | nC   |
| Q <sub>gd</sub>                     | Gate-drain charge             |                                                                                                                                                  | -    | 9.9  | -    | nC   |

**Notes:**

<sup>(1)</sup>C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

Table 7: Switching times

| Symbol              | Parameter           | Test conditions                                                                                                                                                                                                                                | Min. | Typ. | Max. | Unit |
|---------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| t <sub>d(on)</sub>  | Turn-on delay time  | V <sub>DD</sub> = 300 V, I <sub>D</sub> = 5.5 A<br>R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 12.3 | -    | ns   |
| t <sub>r</sub>      | Rise time           |                                                                                                                                                                                                                                                | -    | 4.8  | -    | ns   |
| t <sub>d(off)</sub> | Turn-off delay time |                                                                                                                                                                                                                                                | -    | 42.5 | -    | ns   |
| t <sub>f</sub>      | Fall time           |                                                                                                                                                                                                                                                | -    | 10.6 | -    | ns   |

Table 8: Source drain diode

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                           | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                           | -    |      | 8    | A    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                           | -    |      | 32   | A    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 8\text{ A}$                                                                                                                                                                             | -    |      | 1.6  | V    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ (see <a href="#">Figure 16</a> :<br>"Test circuit for inductive load switching and diode recovery times")                         | -    | 90   |      | ns   |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                           | -    | 252  |      | nC   |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                           | -    | 5.6  |      | A    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ °C}$ (see <a href="#">Figure 16</a> :<br>"Test circuit for inductive load switching and diode recovery times") | -    | 170  |      | ns   |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                           | -    | 667  |      | ns   |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                           | -    | 8.6  |      | A    |

**Notes:**

(1) Pulse width is limited by safe operating area

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Table 9: Gate-source Zener diode

| Symbol        | Parameter                     | Test conditions                                 | Min.     | Typ. | Max. | Unit |
|---------------|-------------------------------|-------------------------------------------------|----------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$ | $\pm 30$ | -    | -    | V    |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

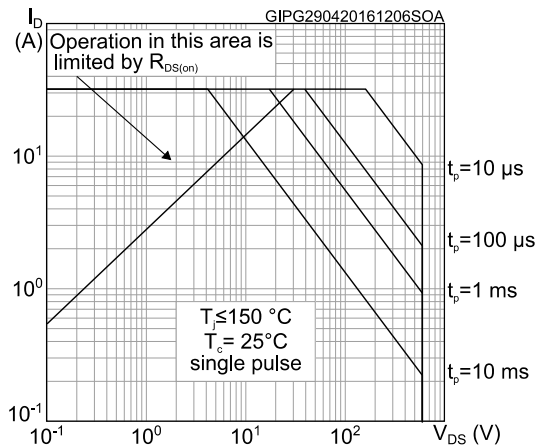


Figure 3: Thermal impedance

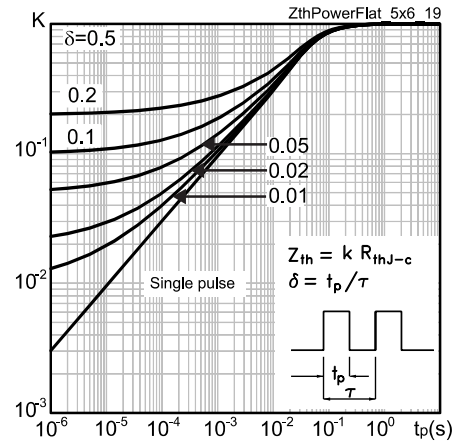


Figure 4: Output characteristics

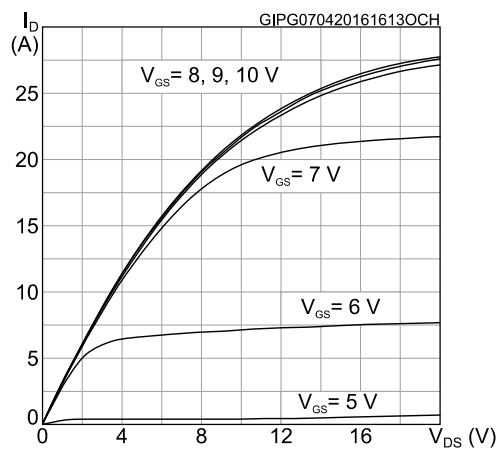


Figure 5: Transfer characteristics

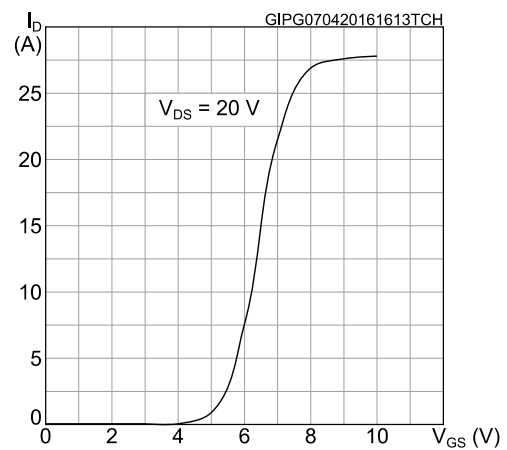


Figure 6: Gate charge vs gate-source voltage

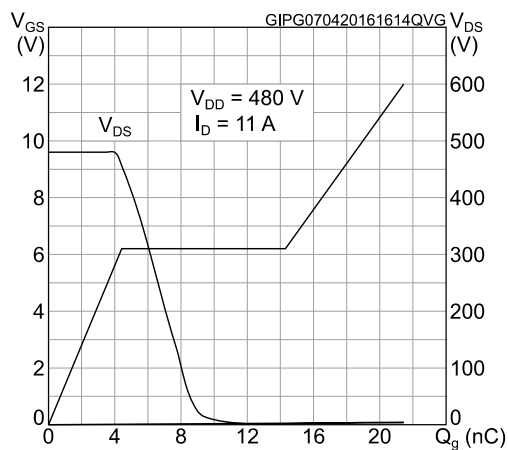


Figure 7: Static drain-source on-resistance

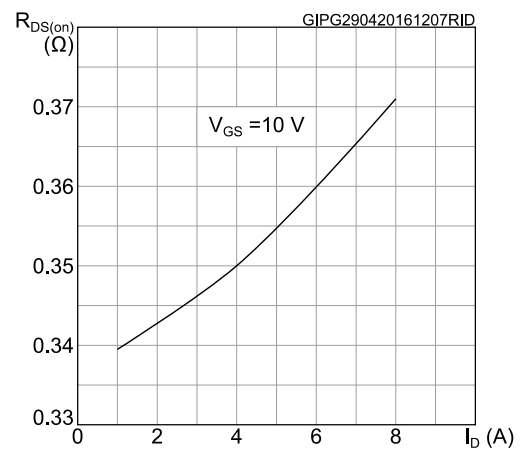


Figure 8: Capacitance variations

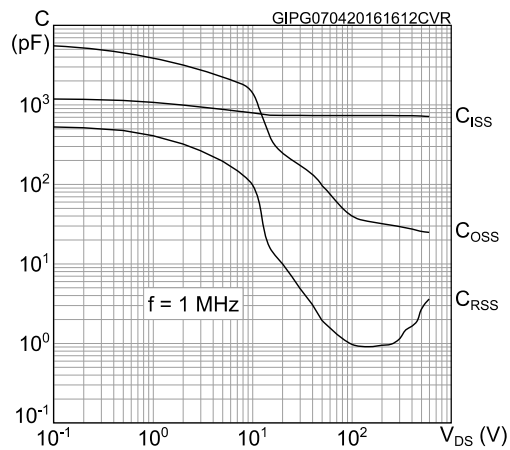


Figure 9: Normalized gate threshold voltage vs temperature

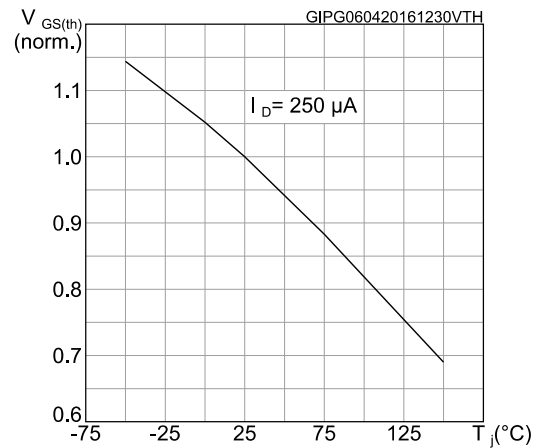


Figure 10: Normalized on-resistance vs temperature

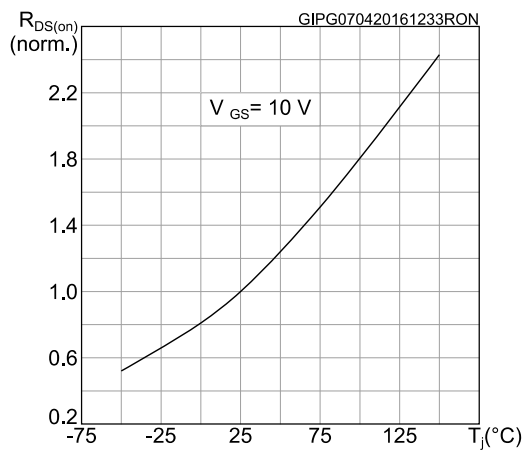


Figure 11: Normalized V(BR)DSS vs temperature

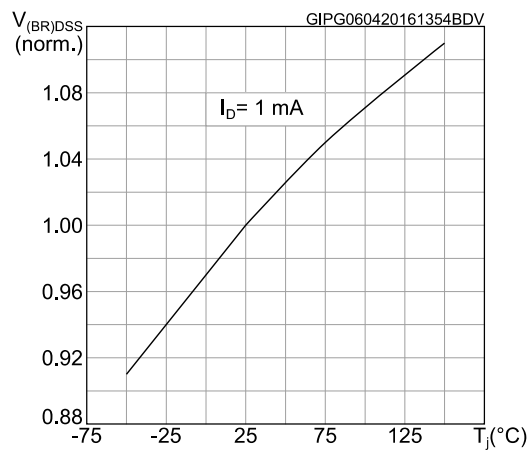


Figure 12: Source-drain diode forward characteristics

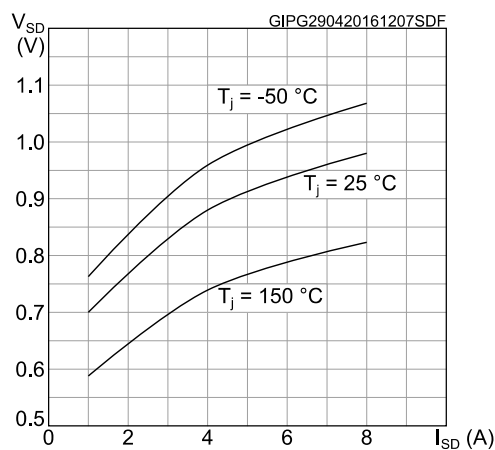
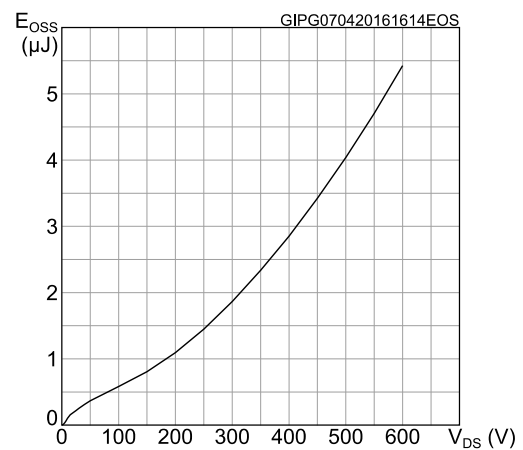
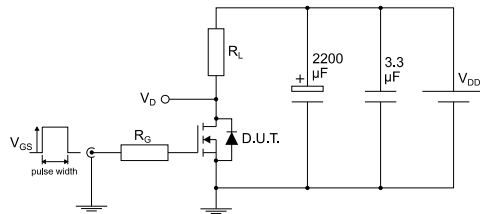


Figure 13: Output capacitance stored energy



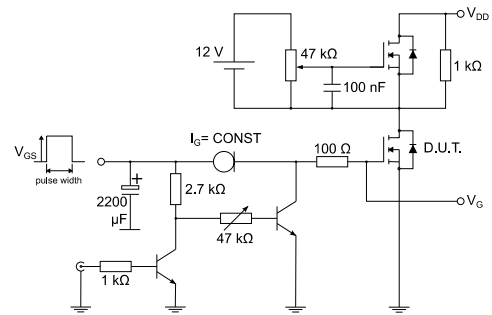
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



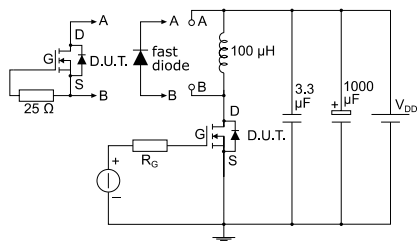
AM01468v1

**Figure 15: Test circuit for gate charge behavior**



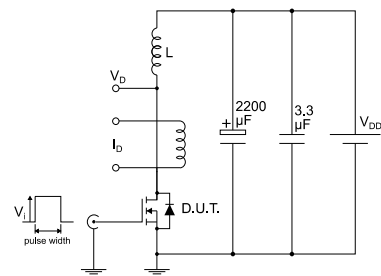
AM01469v1

**Figure 16: Test circuit for inductive load switching and diode recovery times**



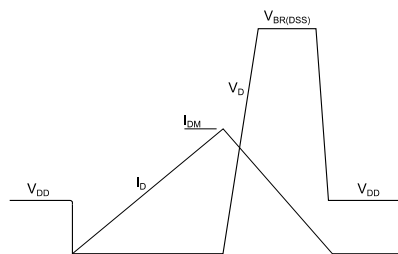
AM01470v1

**Figure 17: Unclamped inductive load test circuit**



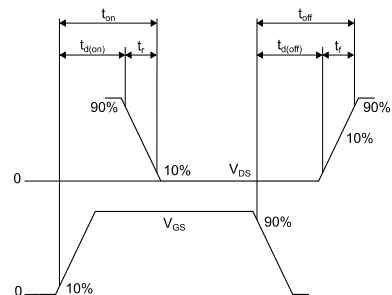
AM01471v1

**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **[www.st.com](http://www.st.com)**. ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

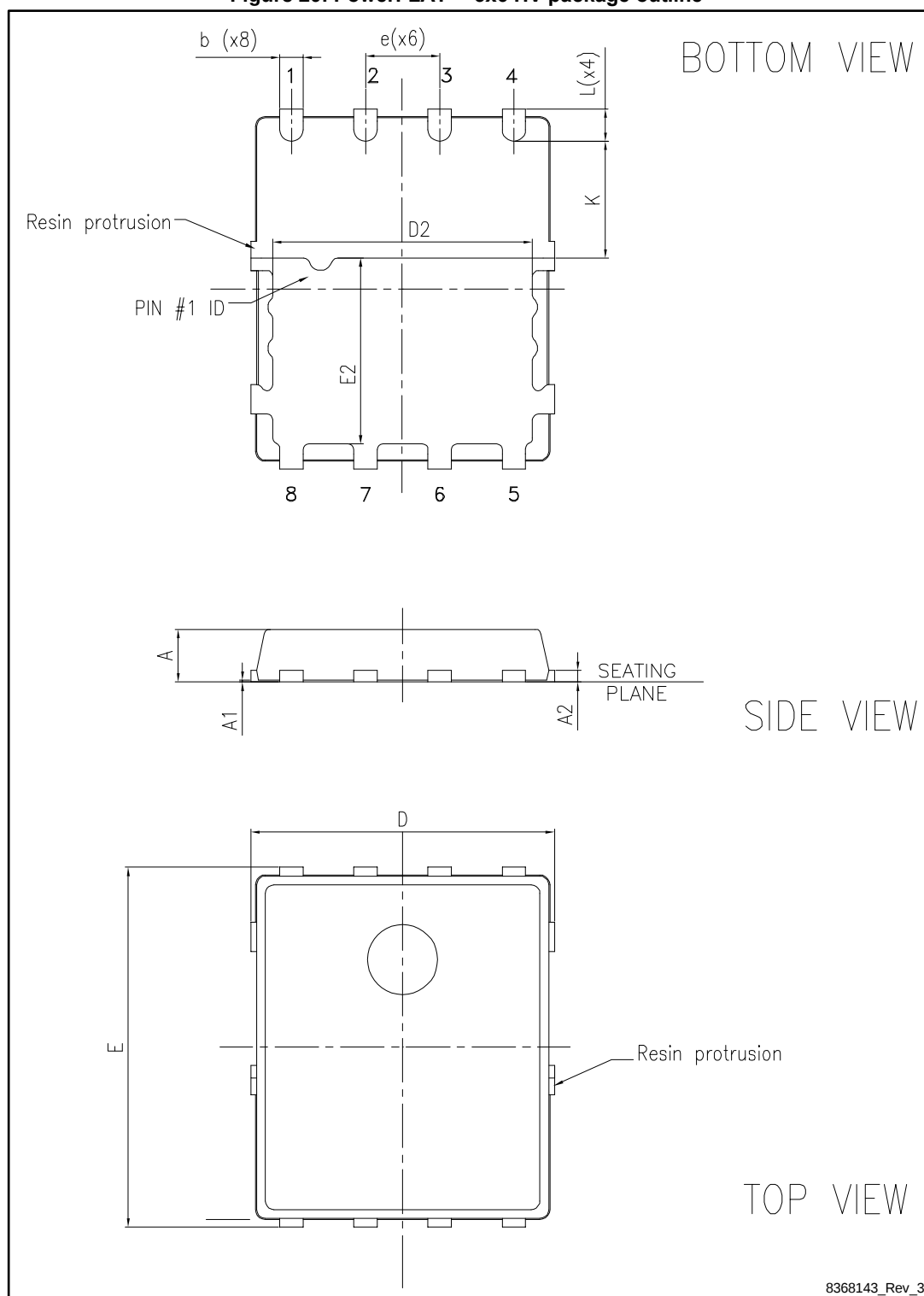
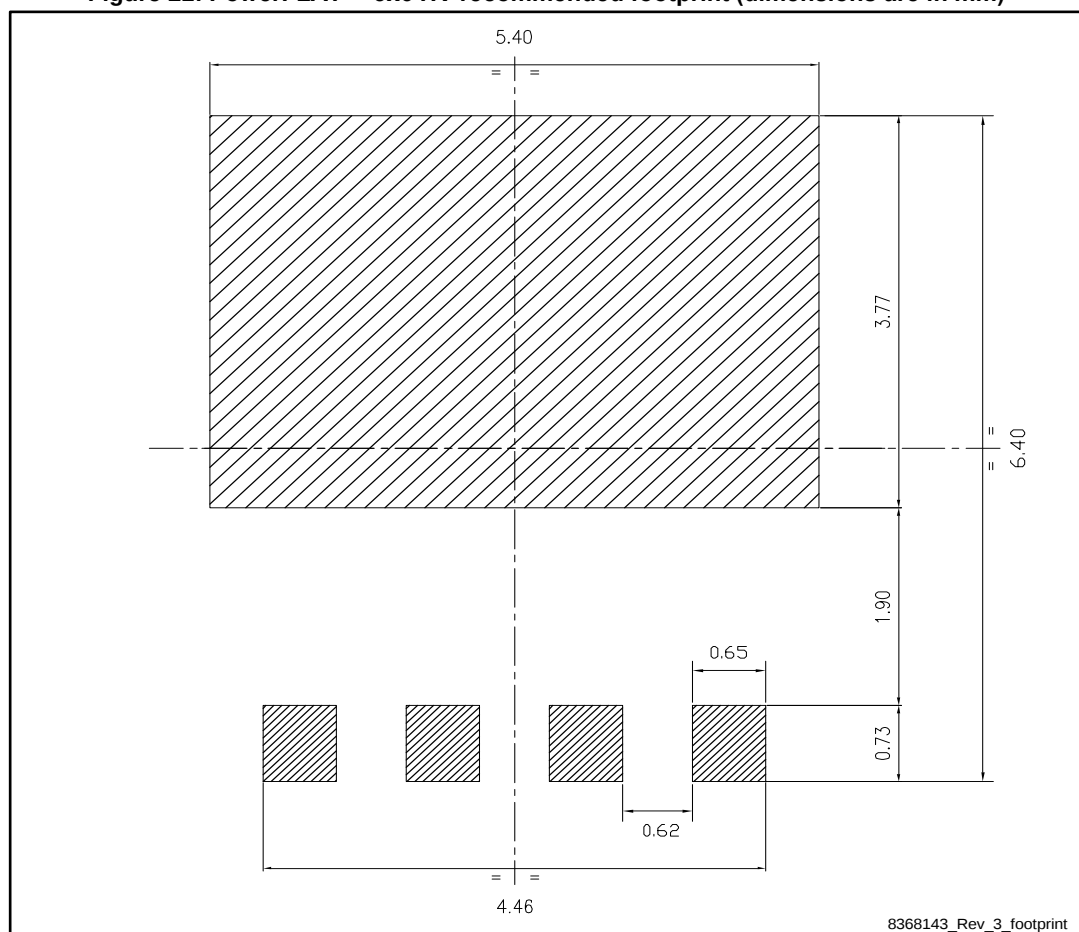


Table 10: PowerFLAT™ 5x6 HV mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 0.80 |      | 1.00 |
| A1   | 0.02 |      | 0.05 |
| A2   |      | 0.25 |      |
| b    | 0.30 |      | 0.50 |
| D    | 5.10 | 5.20 | 5.30 |
| E    | 6.05 | 6.15 | 6.25 |
| E2   | 3.10 | 3.20 | 3.30 |
| D2   | 4.30 | 4.40 | 4.50 |
| e    |      | 1.27 |      |
| L    | 0.50 | 0.55 | 0.60 |
| K    | 1.90 | 2.00 | 2.10 |

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



## 4.2 Packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

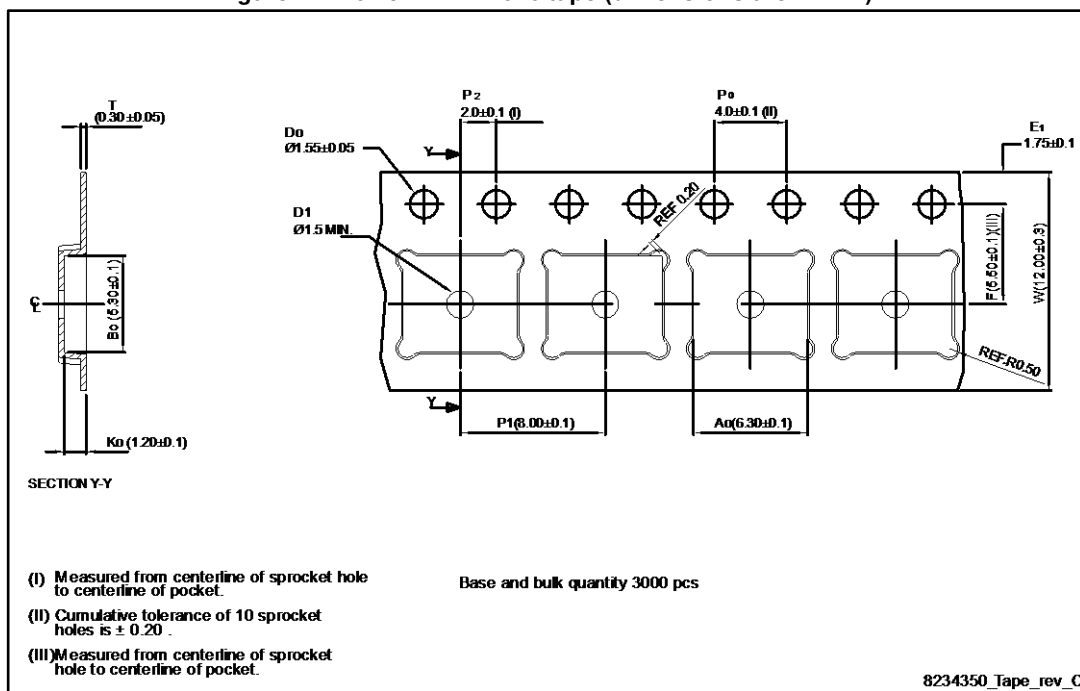


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

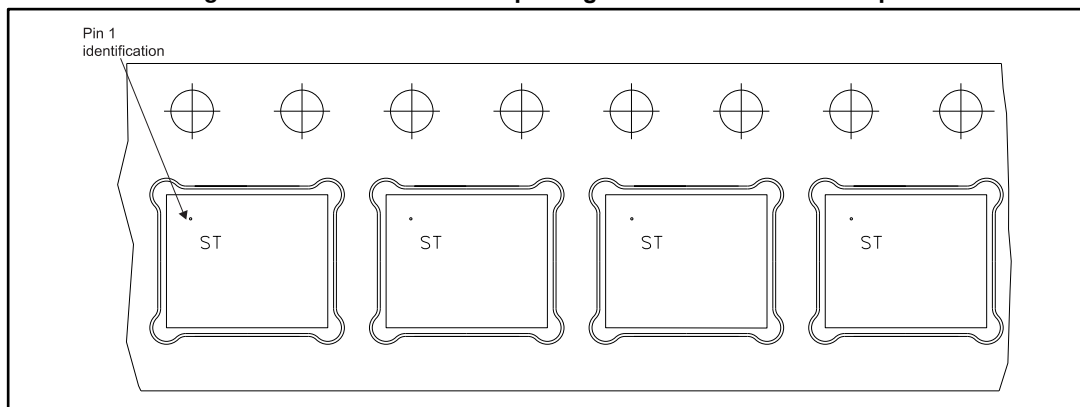
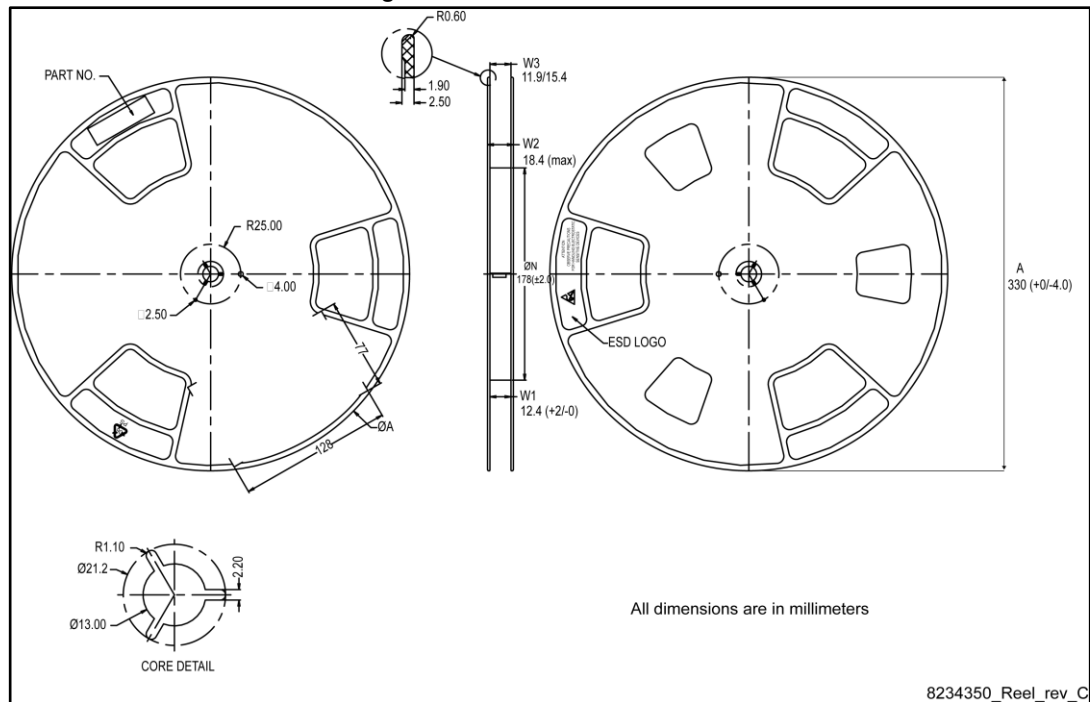


Figure 24: PowerFLAT™ 5x6 reel



## 5 Revision history

**Table 11: Document revision history**

| Date        | Revision | Changes                                                       |
|-------------|----------|---------------------------------------------------------------|
| 02-May-2016 | 1        | First release.                                                |
| 07-Dec-2016 | 2        | Document status promoted from preliminary to production data. |

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