

SN54ABT543A, SN74ABT543A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-II^B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

description

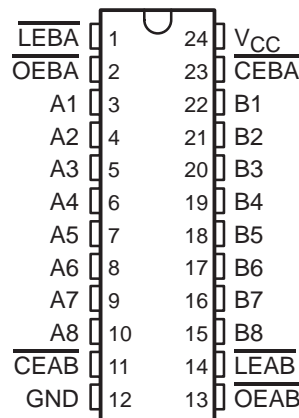
The 'ABT543A octal transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

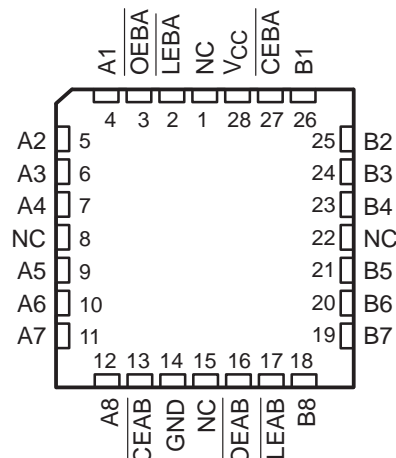
To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT543A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT543A is characterized for operation from -40°C to 85°C .

SN54ABT543A . . . JT OR W PACKAGE
SN74ABT543A . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT543A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-II^B is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

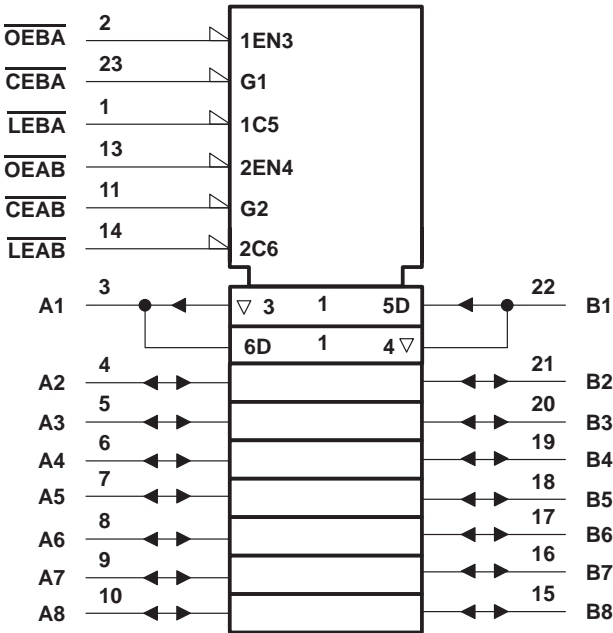
SN54ABT543A, SN74ABT543A
OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

FUNCTION TABLE†				
INPUTS				OUTPUT B
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^\ddagger
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.
‡ Output level before the indicated steady-state input conditions were established

logic symbols§

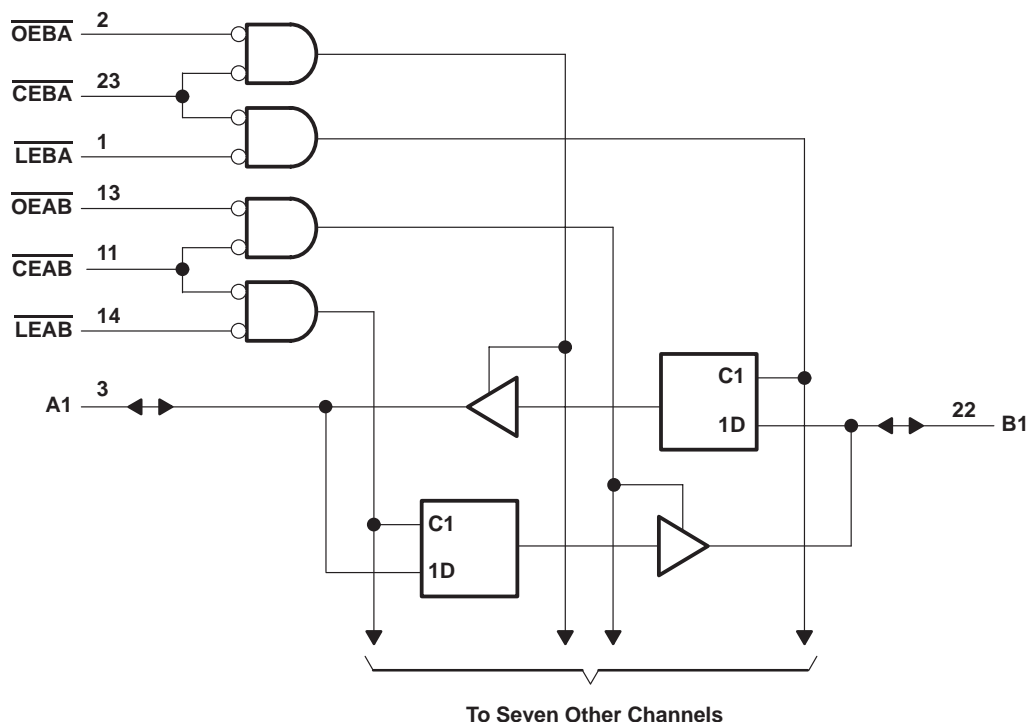


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

SN54ABT543A, SN74ABT543A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT543A	96 mA
SN74ABT543A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	104°C/W
DW package	81°C/W
NT package	67°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

SN54ABT543A, SN74ABT543A

OCTAL REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

recommended operating conditions (see Note 3)

			SN54ABT543A		SN74ABT543A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current			–24		–32	mA
I _{OL}	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT543A		SN74ABT543A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = –3 mA	3			3		3		
		V _{CC} = 4.5 V, I _{OH} = –24 mA	2			2				
		V _{CC} = 4.5 V, I _{OH} = –32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 48 mA			0.55		0.55			V
		V _{CC} = 4.5 V, I _{OL} = 64 mA			0.55*				0.55	
V _{hys}				100						mV
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
	A or B ports				±100		±100		±100	
I _{OZH} ‡		V _{CC} = 5.5 V, V _O = 2.7 V			10§		10§		10§	μA
I _{OZL} ‡		V _{CC} = 5.5 V, V _O = 0.5 V			–10§		–10§		–10§	μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high			50		50		50	μA
I _O ¶		V _{CC} = 5.5 V, V _O = 2.5 V	–50*	–100	–180*	–50	–200	–50	–180	mA
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs high		1	250*		350		250	μA
		Outputs low		24	30*		34		30	mA
		Outputs disabled		0.5	250*		350		250	μA
ΔI _{CC} #		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V			4					pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V			7					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT543A, SN74ABT543A
OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT543A		UNIT		
				$V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$			MIN	MAX
				MIN	MAX			
t_w	Pulse duration, \overline{LEAB} or \overline{LEBA} low			3.5	3.5	ns		
t_{su}	Setup time	Data before \overline{LEAB} or $\overline{LEBA}\uparrow$	High	2.5	2.5	ns		
			Low	3	3			
		Data before \overline{CEAB} or $\overline{CEBA}\uparrow$	High	2.5	2.5			
			Low	3	3			
t_h	Hold time	Data after \overline{LEAB} or $\overline{LEBA}\uparrow$	1	1	ns			
		Data after \overline{CEAB} or $\overline{CEBA}\uparrow$	1	1				

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN74ABT543A		UNIT		
				$V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$			MIN	MAX
				MIN	MAX			
t_w	Pulse duration, \overline{LEAB} or \overline{LEBA} low			3.5	3.5	ns		
t_{su}	Setup time	Data before \overline{LEAB} or $\overline{LEBA}\uparrow$	High	3.5	3.5	ns		
			Low	3	3			
		Data before \overline{CEAB} or $\overline{CEBA}\uparrow$	High	3.5	3.5			
			Low	3	3			
t_h	Hold time	Data after \overline{LEAB} or $\overline{LEBA}\uparrow$	0.5	0.5	ns			
		Data after \overline{CEAB} or $\overline{CEBA}\uparrow$	0.5	0.5				

SN54ABT543A, SN74ABT543A

OCTAL REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT543A					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1.6†	4.4	4.4	1.6†	5.5	ns
t _{PHL}			1.6	4.4	5.1	1.6	6.2	
t _{PLH}	LEBA or LEAB	A or B	1.6†	4.1	5.1	1.6†	6.6	ns
t _{PHL}			1.6	4.6	5.4	1.6	6.4	
t _{PZH}	OEBA or OEAB	A or B	1.4	3.9	4.1	1.4	5.1	ns
t _{PZL}			2	5	4.9	2	5.8	
t _{PHZ}	OEBA or OEAB	A or B	2.5†	5.9	5.8	2.5†	6.9	ns
t _{PLZ}			2.5†	5.5	6.1	2.5†	7.6	
t _{PZH}	CEBA or CEAB	A or B	1.4	3.9	4.7	1.4	5.6	ns
t _{PZL}			2	5	5.7	2	6.2	
t _{PHZ}	CEBA or CEAB	A or B	3.2†	5.9	6.5	3.2†	7.3	ns
t _{PLZ}			2.5†	5.5	6.7	2.5†	7.8	

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

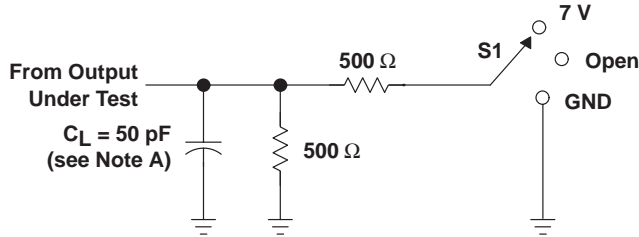
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT543A					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1.8†	4.4	5.9	1.8†	6.9	ns
t _{PHL}			1.9	4.4	5.9	1.9	6.9	
t _{PLH}	LEBA or LEAB	A or B	1.5†	4.1	5.6	1.5†	6.6	ns
t _{PHL}			2.1	4.6	6.1	2.1	7.1	
t _{PZH}	OEBA or OEAB	A or B	1.4	3.9	5.4	1.4	6.4	ns
t _{PZL}			2.5	5	6.5	2.5	7.5	
t _{PHZ}	OEBA or OEAB	A or B	2.5†	5.9	7.4	2.5†	8.4	ns
t _{PLZ}			2.5†	5.5	7	2.5†	8	
t _{PZH}	CEBA or CEAB	A or B	1.4	3.9	5.4	1.4	6.4	ns
t _{PZL}			2.5	5	6.5	2.5	7.5	
t _{PHZ}	CEBA or CEAB	A or B	2.9†	5.9	7.4	2.9†	8.4	ns
t _{PLZ}			2.4†	5.5	7	2.4†	8	

† This data sheet limit may vary among suppliers.



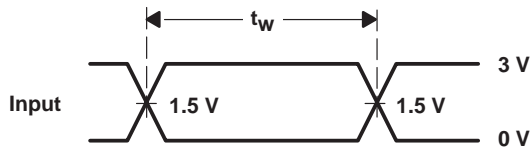
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

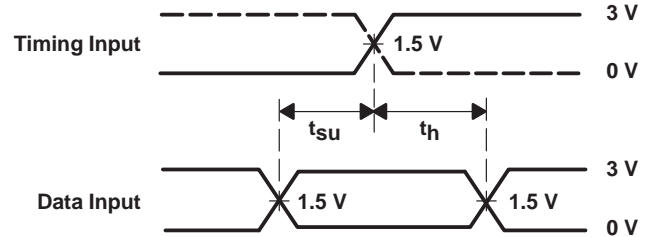


LOAD CIRCUIT

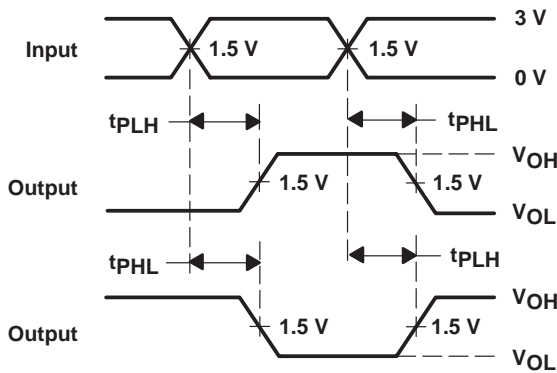
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



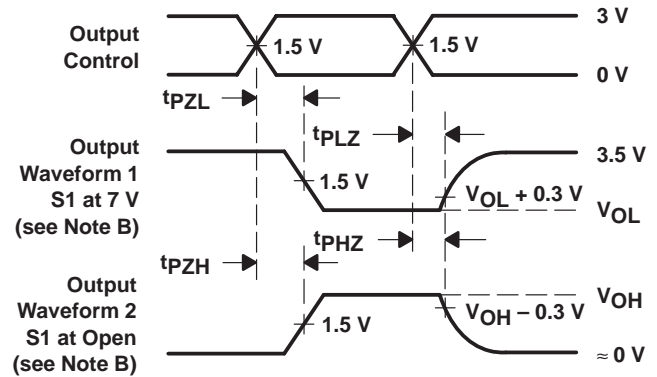
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.