

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

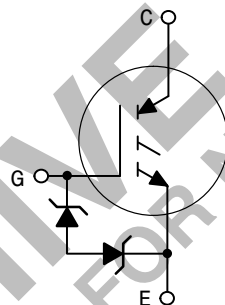
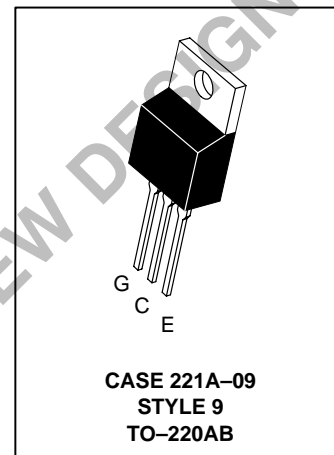
N-Channel Enhancement-Mode Silicon Gate

MGP11N60E

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage-blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. This new E-series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO-220 Package
- High Speed: $E_{off} = 60 \mu\text{J/A}$ typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 400 V
- Low On-Voltage 2.0 V typical at 8.0 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate-Emitter Zener Diodes

IGBT IN TO-220
11 A @ 90°C
15 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON-VOLTAGE



MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	600	Vdc
Collector-Gate Voltage ($R_{GE} = 1.0 \text{ M}\Omega$)	V_{CGR}	600	Vdc
Gate-Emitter Voltage — Continuous	V_{GE}	± 20	Vdc
Collector Current — Continuous @ $T_C = 25^\circ\text{C}$ — Continuous @ $T_C = 90^\circ\text{C}$ — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	15 11 22	Adc Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	96 0.77	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	°C
Short Circuit Withstand Time ($V_{CC} = 400 \text{ Vdc}$, $V_{GE} = 15 \text{ Vdc}$, $T_J = 125^\circ\text{C}$, $R_G = 20 \Omega$)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.3 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C
Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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MGP11N60E

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($V_{GE} = 0\text{ Vdc}$, $I_C = 25\text{ }\mu\text{Adc}$) Temperature Coefficient (Positive)	$V_{(BR)CES}$	600 —	— 870	— —	Vdc mV/ $^\circ\text{C}$
Emitter-to-Collector Breakdown Voltage ($V_{GE} = 0\text{ Vdc}$, $I_{EC} = 100\text{ mAdc}$)	$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current ($V_{CE} = 600\text{ Vdc}$, $V_{GE} = 0\text{ Vdc}$) ($V_{CE} = 600\text{ Vdc}$, $V_{GE} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{CES}	— —	— —	10 200	μAdc
Gate-Body Leakage Current ($V_{GE} = \pm 20\text{ Vdc}$, $V_{CE} = 0\text{ Vdc}$)	I_{GES}	—	—	50	μAdc

ON CHARACTERISTICS (1)

Collector-to-Emitter On-State Voltage ($V_{GE} = 15\text{ Vdc}$, $I_C = 4.0\text{ Adc}$) ($V_{GE} = 15\text{ Vdc}$, $I_C = 4.0\text{ Adc}$, $T_J = 125^\circ\text{C}$) ($V_{GE} = 15\text{ Vdc}$, $I_C = 8.0\text{ Adc}$)	$V_{CE(on)}$	— — —	1.6 1.5 2.0	1.9 — 2.4	Vdc
Gate Threshold Voltage ($V_{CE} = V_{GE}$, $I_C = 1.0\text{ mAdc}$) Threshold Temperature Coefficient (Negative)	$V_{GE(th)}$	4.0 —	6.0 10	8.0 —	Vdc mV/ $^\circ\text{C}$
Forward Transconductance ($V_{CE} = 10\text{ Vdc}$, $I_C = 8.0\text{ Adc}$)	g_{fe}	—	3.5	—	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{CE} = 25\text{ Vdc}$, $V_{GE} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{ies}	—	779	—	pF
Output Capacitance		C_{oes}	—	81	—	
Transfer Capacitance		C_{res}	—	13	—	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	$(V_{CC} = 360\text{ Vdc}$, $I_C = 8.0\text{ Adc}$, $V_{GE} = 15\text{ Vdc}$, $L = 300\text{ }\mu\text{H}$, $R_G = 20\text{ }\Omega$) Energy losses include "tail"	$t_{d(on)}$	—	46	—	ns
Rise Time		t_r	—	34	—	
Turn-Off Delay Time		$t_{d(off)}$	—	102	—	
Fall Time		t_f	—	226	—	
Turn-Off Switching Loss		E_{off}	—	0.32	0.40	mJ
Turn-On Delay Time	$(V_{CC} = 360\text{ Vdc}$, $I_C = 8.0\text{ Adc}$, $V_{GE} = 15\text{ Vdc}$, $L = 300\text{ }\mu\text{H}$, $R_G = 20\text{ }\Omega$, $T_J = 125^\circ\text{C}$) Energy losses include "tail"	$t_{d(on)}$	—	42	—	ns
Rise Time		t_r	—	26	—	
Turn-Off Delay Time		$t_{d(off)}$	—	214	—	
Fall Time		t_f	—	228	—	
Turn-Off Switching Loss		E_{off}	—	0.48	—	mJ
Gate Charge	$(V_{CC} = 360\text{ Vdc}$, $I_C = 8.0\text{ Adc}$, $V_{GE} = 15\text{ Vdc}$)	Q_T	—	39.2	—	nC
		Q_1	—	8.7	—	
		Q_2	—	17.4	—	

INTERNAL PACKAGE INDUCTANCE

Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)	L_E	—	7.5	—	nH
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(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

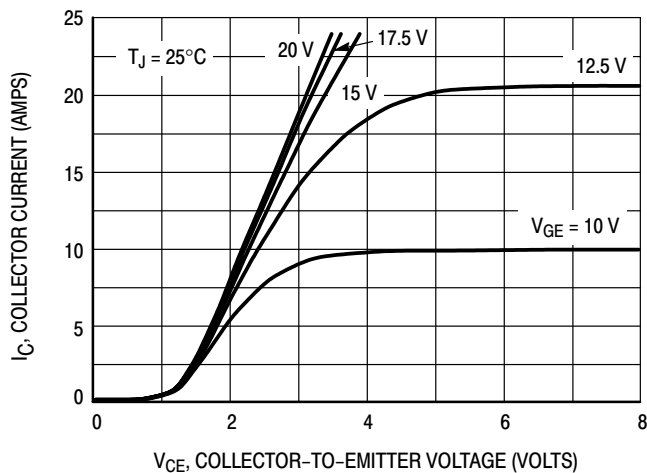


Figure 1. Output Characteristics

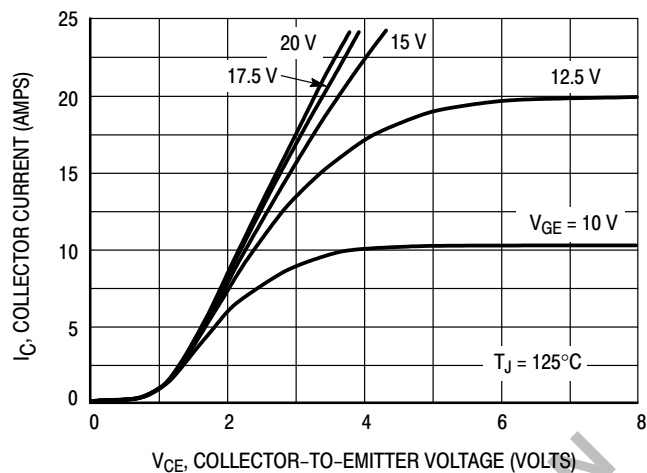


Figure 2. Output Characteristics

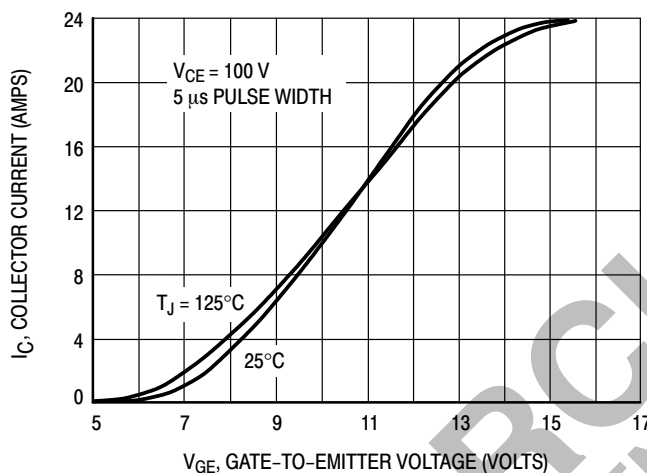


Figure 3. Transfer Characteristics

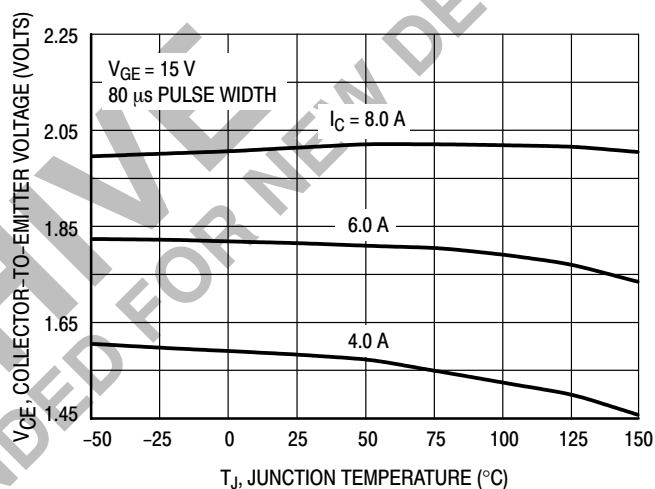


Figure 4. Collector-To-Emitter Saturation Voltage versus Junction Temperature

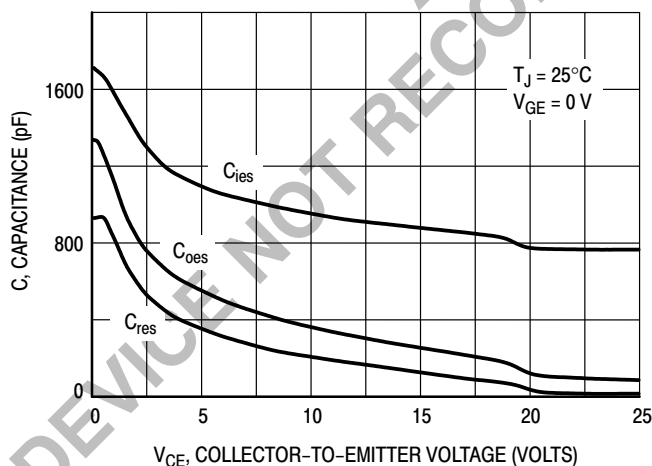


Figure 5. Capacitance Variation

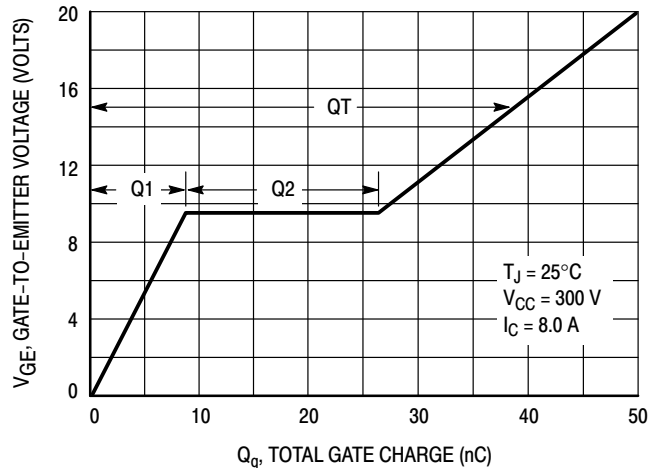


Figure 6. Gate-To-Emitter Voltage versus Total Charge

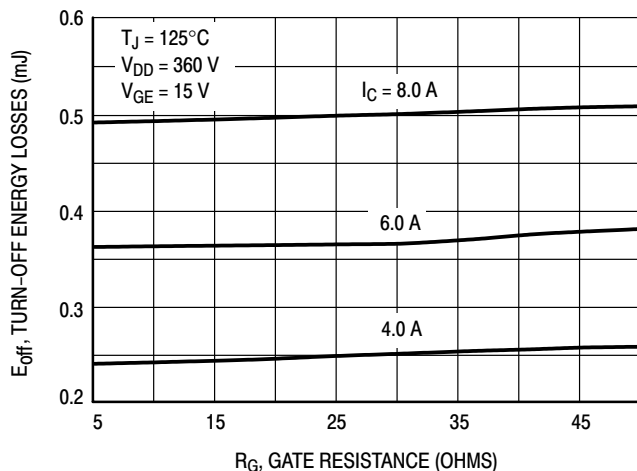


Figure 7. Turn-Off Losses versus Gate Resistance

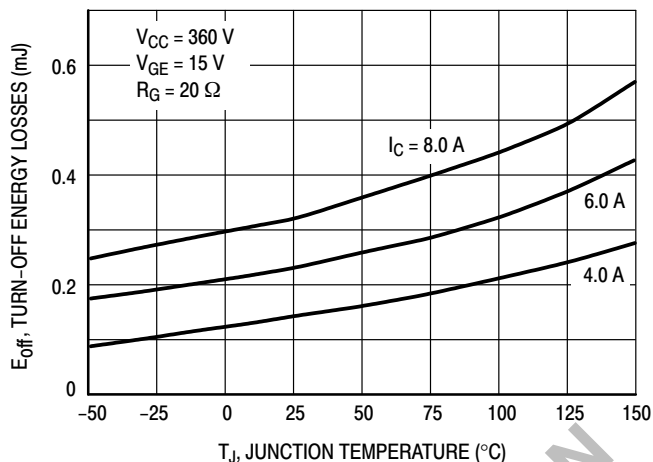


Figure 8. Turn-Off Losses versus Junction Temperature

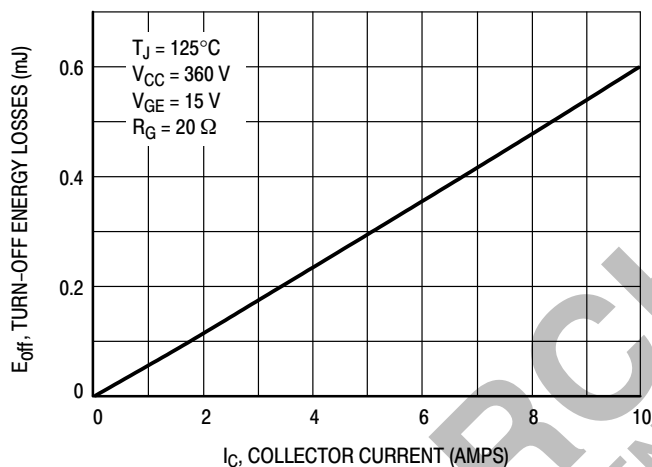


Figure 9. Turn-Off Losses versus Collector Current

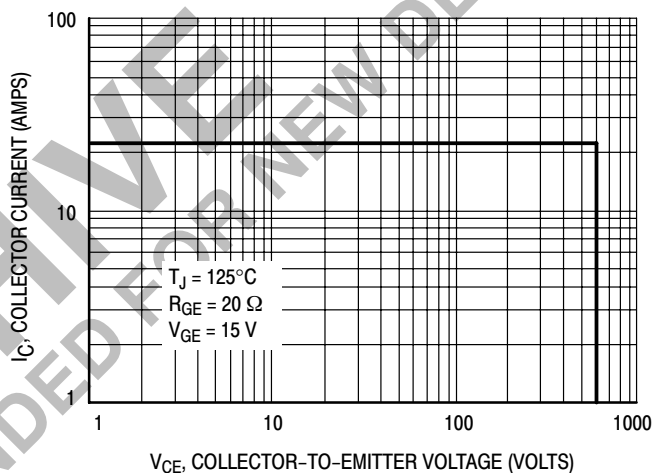
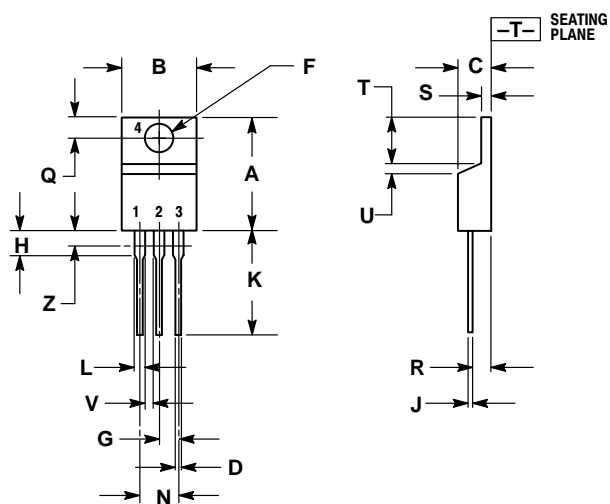


Figure 10. Reverse Biased Safe Operating Area

PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 9:

- PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-09
TO-220AB
ISSUE Z

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RECOMMENDED FOR NEW DESIGN

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