# Si501/2/3/4

**LVCMOS CMEMS® Programmable Oscillator Series**

## Description

The Si501/2/3/4 CMEMS programmable oscillator series combines standard CMOS + MEMS in a single, monolithic IC to provide high-quality and high-reliability oscillators. Each device is specified for guaranteed performance across voltage, process, temperature, shock, vibration and aging for 10 years. More information on CMEMS available at www.silabs.com/cmems.

**Applications**: General purpose microcontrollers, industrial control, IP cameras, surveillance systems, metering, home and office automation, security systems, sleep clocking, 10/100 Ethernet/EtherCAT, SPI, SAS3.0 / SATA3.0, PCIe ref clock, NVMe, HDD, SSD, hybrid storage, DDR3/3L, USB2.0, USB OTG/2.0, M2M, HDMI

**Not recommended**: Wi-Fi, Bluetooth, USB 3.0, Gigabit Ethernet

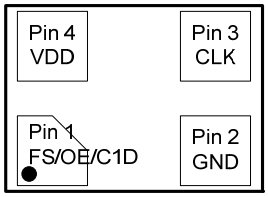
## Features

- Any frequency oscillator from 32 kHz to 100 MHz
  - Contact Silicon Labs Marketing for frequencies above 100 MHz
- Frequency stability: ±20/±30/±50 ppm including 10-year aging
- -20 to +70 °C: Extended Commercial
- -40 to +85 °C: Industrial
- Highly configurable: low power vs. low jitter, frequency, $F_{STAB}$, $T_R/T_F$, $V_{DD}$, OE/FS functionality (see ordering guide below)
- In-circuit programmable via C1D 1-pin interface (Si504)
- Seamless $V_{DD}$ from +1.71 to +3.63 V
- Low period jitter mode / low power mode
- Glitchless start and stop
- RoHS compliant, Pb-free

## Product Selector Guide

| Part Number | Description | Control |
|---|---|---|
| Si501 | Single frequency | OE |
| Si502 | Dual frequency | FS/OE |
| Si503 | Quad frequency | FS |
| Si504 | Programmable for any supported frequency or configuration | C1D 1-pin interface (see Si504 data sheet for details) |

## Pin-out




(top view)

## Pin Description

| Pin Number | Description |
|---|---|
| 1 | FS = Frequency Select<br>OE = Output Enable<br>C1D = Single wire interface |
| 2 | GND = Ground |
| 3 | CLK = Clock out |
| 4 | VDD = Power Supply |

## Ordering Guide

| | VDD | TYP $T_R/T_F$ | Jitter vs Power |
|---|---|---|---|
| A | 1.7-3.6 | 0.7 ns[1] | Low Power |
| B | 3.3V | 1.3 ns[2] | |
| C | 2.5V | 1.3 ns[2] | |
| D | 1.8V | 1.3 ns[2] | |
| E | 1.7-3.6 | 3 ns[3] | |
| F | 1.7-3.6 | 5 ns[3] | |
| G | 1.7-3.6 | 8 ns[3] | |
| H | 1.7-3.6 | 0.7 ns[1] | Low Jitter |
| J | 3.3V | 1.3 ns[2] | |
| K | 2.5V | 1.3 ns[2] | |
| L | 1.8V | 1.3 ns[2] | |
| M | 1.7-3.6 | 3 ns[3] | |
| N | 1.7-3.6 | 5 ns[3] | |
| P | 1.7-3.6 | 8 ns[3] | |

| 501 | | | |
|---|---|---|---|
| | OE High | OE Low | Internal Pull Resistor |
| A | Enable | Stop | Pull-Up |
| B | | Doze | |
| C | | Sleep | |
| D | Stop | Enable | Pull-Down |
| E | Doze | | |
| F | Sleep | | |
| G | Enable | Stop | None |
| H | | Doze | |
| J | | Sleep | |
| K | Stop | Enable | |
| L | Doze | | |
| M | Sleep | | |

| 502[6] | | |
|---|---|---|
| | OE Low | Internal Pull Resistor |
| A | Stop | Pull-Up |
| B | Doze | |
| C | Sleep | |
| D | Stop | None |
| E | Doze | |
| F | Sleep | |

| 503 | |
|---|---|
| A | Pull-Up |
| B | None |

| 504 | |
|---|---|
| A | Pull-Up only |

| 504 only[5] | |
|---|---|
| | Maximum $F_{OUT}$ |
| A | 0.032 – 80 MHz |
| B | 0.032 – 100 MHz |

| | Temp Range |
|---|---|
| F | -20 to 70 °C |
| G | -40 to 85 °C |

| OPN Prefix | Description |
|---|---|
| 501 | Single frequency |
| 502 | Dual frequency |
| 503 | Quad frequency |
| 504 | Any frequency |

50X - - - - - - - - - - A - R

| | ppm |
|---|---|
| A | ± 50 |
| B | ± 30 |
| C | ± 20 |

| OPN | Freq Code | Description |
|---|---|---|
| 501 only | Mxxxxxx | $f_{OUT}$ < 1 MHz |
| | xMxxxxx | 1 MHz ≤ $f_{OUT}$ < 10 MHz |
| | xxMxxxx | 10 MHz ≤ $f_{OUT}$ < 100 MHz |
| | 100M000 | $f_{OUT}$ = 100 MHz |
| 501/2/3/4 | xxxxxx | Silicon Labs 6-digit code for 502/3/4, or >6-decimal freq on 501 |

| | Reel |
|---|---|
| R | Reel |
| | Cut Tape |

| | Package Dimension |
|---|---|
| B | 3.2 x 5 mm[4] |
| C | 2.5 x 3.2 mm |
| D | 2 x 2.5 mm |

Ordering Guide Notes:
1. Series termination resistor ($R_S$ – see Apps Circuits section) is recommended for this configuration.
2. Series termination resistor ($R_S$) is not needed for this configuration. Output impedance is 50Ω for the indicated supply condition.
3. Series termination resistor ($R_S$) is not needed for this configuration. Reduced EMI setting.
4. 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.
5. Select option to support maximum anticipated frequency needed.
6. The Si502 OE pin has three (3) states: OE High = Freq 1; OE Weak High = Freq 2; OE Low is configurable.



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This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

## Selected Electrical Specifications

$V_{DD}$ = +1.71 V to +3.63 V, $T_A$ = -40 to 85 ºC unless stated otherwise.

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency Range | $F_{CLK}$ | Programmable family range | 0.032 | — | 100 | MHz |
| Supply Voltage | $V_{DD}$ | Supports continuous $V_{DD}$ from Min to Max | 1.71 | — | 3.63 | V |
| Supply Current | $I_{DD1}$ | 3.3 $V_{DD}$, $F_{CLK}$ = 1 MHz, 4 pF, Low Power mode | — | 1.7 | 2.5 | mA |
| | | 3.3 $V_{DD}$, $F_{CLK}$ = 1 MHz, 4 pF, Low Jitter mode | — | 3.9 | 4.9 | mA |
| Static Supply Current[1] | $I_{DD2}$ | Stop mode, $F_{CLK}$ = 1 MHz, Low Power mode | — | 1.7 | 2.5 | mA |
| | | Stop mode, $F_{CLK}$ = 1 MHz, Low Jitter mode | — | 3.9 | 4.9 | mA |
| | | Doze mode | — | 670 | 890 | µA |
| | | Sleep mode | — | 0.3 | 1 | µA |
| Frequency Stability[2] | $F_{STAB}$ | TA = -20 ºC to +70 ºC, -40 ºC to +85 ºC | -20 | — | +20 | ppm |
| | | | -30 | — | +30 | ppm |
| | | | -50 | — | +50 | ppm |
| CMOS Rise/Fall Time[3] | $T_R/T_F$ | 1st option code = A[4] or H[4] | 0.4 | 0.7 | 1.2 | ns |
| | | 1st option code = B, C, D, J, K, L | 1 | 1.3 | 1.6 | ns |
| | | 1st option code = E, M | 2 | 3 | 4 | ns |
| | | 1st option code = F, N | 4 | 5 | 7 | ns |
| | | 1st option code = G, P | 7 | 8 | 11 | ns |
| Cycle-to-Cycle Jitter | $J_{CCPP}$ | $F_{CLK}$ = 100 MHz, Low Jitter mode<br>1st option code = H | — | 14 | 25 | ps pk-pk |
| Period Jitter Pk-Pk | $J_{PPKPK}$ | $F_{CLK}$ = 100 MHz, Low Jitter mode<br>1st option code = H | — | 9 | 13 | ps pk-pk |
| Period Jitter | $J_{PRMS}$ | $F_{CLK}$ = 100 MHz, Low Jitter mode<br>1st option code = H | — | 1 | 1.6 | ps rms |
| Phase Jitter[5] | ϕ | $F_{CLK}$ = 75 MHz, $F_{OFFSET}$ = 900 kHz - 7.5 MHz<br>Low Jitter mode, 1st option code = H | — | 1 | 1.3 | ps rms |
| Duty Cycle | DC | Drive strength selected such that $T_R/T_F$ (20% to 80%) < 10 % of period | 45 | 50 | 55 | % |
| Input High Voltage | $V_{IH}$ | | 0.7 x $V_{DD}$ | — | — | V |
| Input Low Voltage | $V_{IL}$ | | — | — | 0.3 x $V_{DD}$ | V |
| Output High Voltage | $V_{OH}$ | | 0.9 x $V_{DD}$ | — | — | V |
| Output Low Voltage | $V_{OL}$ | | — | — | 0.1 x $V_{DD}$ | V |

1. Si501 supports OE/mode functionality. Si502 supports OE/mode and FS functionality. Si503 supports only FS functionality. See data sheet functional description section for more information.
2. Frequency stability includes initial tolerance, solder shift, operating temp range, rated power supply voltage change, load change, 10-year aging, shock, and vibration.
3. $C_L$ = 15 pF, $T_R/T_F$ (20% to 80%), 3.3 V unless otherwise stated. See datasheet for additional $T_R/T_F$ options.
4. Recommended series termination resistor ($R_S$) = 24.9 Ω for $Z_0$=50 Ω.
5. Integrated phase jitter exceeds some high-performance data communications system requirements. See AN783 for more information.

## Absolute Maximum Ratings[1]

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Storage Temperature | $T_S$ | | -55 to 125 | ºC |
| Supply Voltage | $V_{DD}$ | | -0.5 to 3.8 | ºC |
| Input Voltage | $V_{IN}$ | | 0.5 to $V_{DD}$ +0.3 | V |
| ESD HBM (JESD22-A114) | HBM | | 2000 | V |
| ESD CDM | CDM | | 500 | V |
| Solder Temp[2] | $T_{PEAK}$ | | 260 | ºC |
| Solder Time at $T_{PEAK}$[2] | $T_P$ | | 20-40 | s |
| Max Junction Temp | $T_J$ | | 125 | ºC |

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

## Environmental Compliance and Package Information

| Parameter | Test Condition |
|---|---|
| Mechanical Shock | MIL-STD-883, M2002 Cond B. (1,500g) |
| Mechanical Shock High g | MIL-STD-883, M2002, Cond. E (10,000g) |
| Mechanical Vibration | MIL-STD-883, Method 2007 |
| Solderability | MIL-STD-883, Method 2003 |
| Temperature Cycle | JESD22, Method A104 |
| Resistance to Solder Heat | MIL-STD-883, Method 2036 |
| Contact Pads | Gold over Nickel/Palladium |

## Thermal Conditions

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Thermal Impedance | $\Theta_{JA}$ | 3.2 x 5 mm, still air | 187 | °C/W |
| | | 2.5 x 3.2 mm, still air | 239 | |
| | | 2 x 2.5 mm, still air | 241 | |

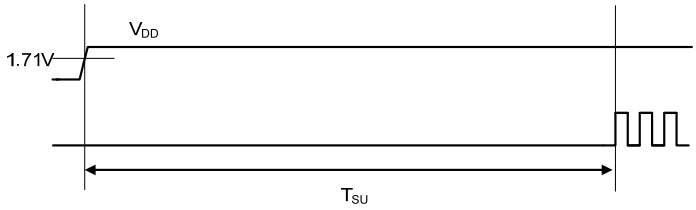
## Clock Timing Characteristics

$V_{DD}$ = +1.71 V to +3.63 V, $T_A$ = -40 to 85 ºC unless stated otherwise.

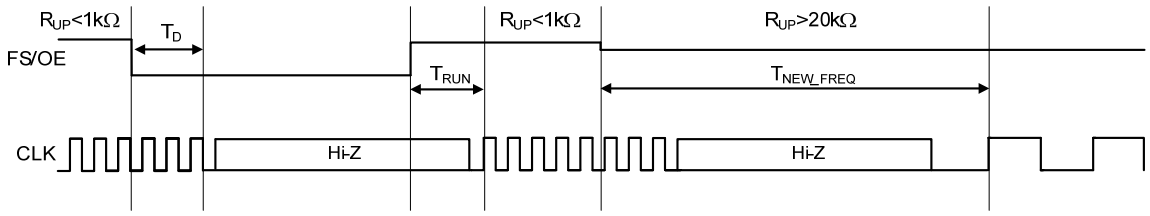
| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Startup Time[1] | $T_{SU}$ | From $V_{DD}$ crossing 1.71 to first clock | — | 2.5 | 4 | ms |
| Resume Time [2, 3] | $T_{RUN}$ | From Stop mode | — | — | 1.5 x $T_{CLK}$ + 35 | ns |
| | | From Sleep mode | — | 2.5 | 5 | ms |
| | | From Doze mode | — | — | 2.55 | |
| Output Disable Time [2, 3] | $T_D$ | To Stop | — | — | 1.5 x $T_{CLK}$ + 35 | ns |
| | | To Sleep/Doze | — | — | 225 | µs |
| Frequency Update Time [2] | $T_{NEW_FREQ}$ | To New Frequency | — | — | 5 | ms |

1. Hold FS/OE high (strong or weak) during powerup for fastest time to clock.
2. Si501 and Si502 only. Si503 has frequency select (FS) only and does not support Stop, Doze or Sleep.
3. $T_{CLK}$ = clock period = 1/ $F_{CLK}$.

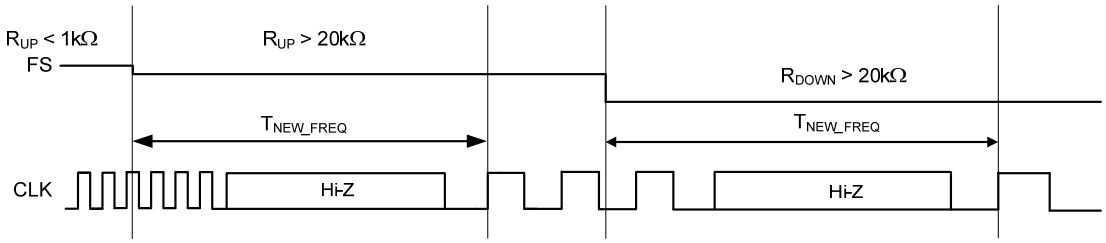
## AC Waveforms




**Si501/2/3 Power On Time**

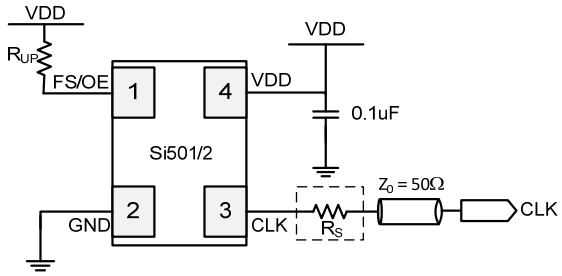



**Si501/2 AC Waveform**

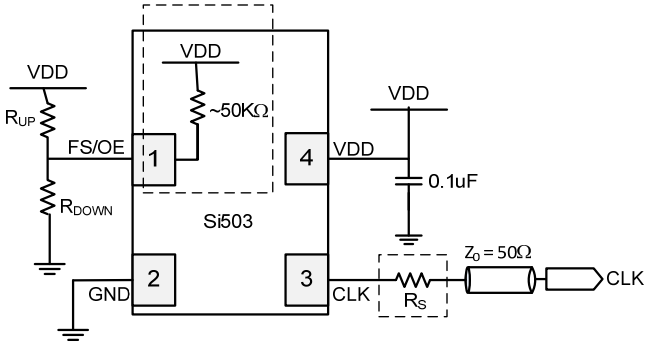



**Si503 AC Waveform**

## Applications Circuits




**Si501/2 Apps Circuit w/ Optional Series Resistor**




**Si503 Apps Circuit w/ Configurable Options**

Notes:
1. Dotted line boxes show optional components depending on configuration options. See data sheet for additional information and for applications using a microcontroller. Data sheet is available at www.silabs.com/cmems.
2. Recommended series termination resistor ($R_S$) = 24.9 Ω for $Z_0$ = 50 Ω.

### Si502 FS/OE States and Resistor Values

| FS/OE State | $R_{UP}$ | Clock Output |
|---|---|---|
| Strong High | 0 Ω ≤ $R_{UP}$ ≤ 1 kΩ | Frequency 1 |
| Weak High | 20 kΩ ≤ $R_{UP}$ ≤ 200 kΩ | Frequency 2 |
| Low | — | Hi-Z |

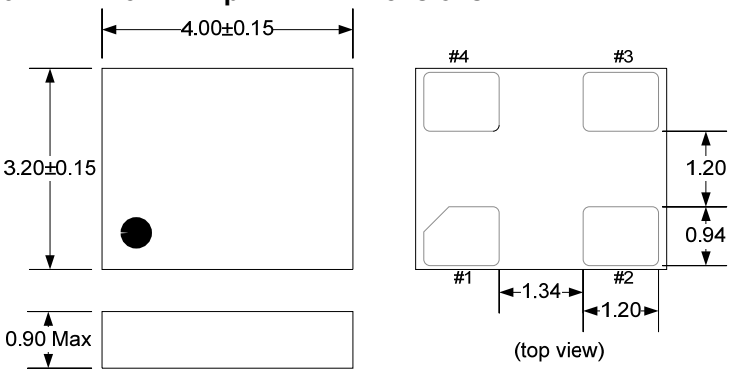
### Si503 FS States and Resistor Values

| FS/OE State | $R_{UP}$ | $R_{DOWN}$ | Clock Output |
|---|---|---|---|
| Strong High | 0 Ω ≤ $R_{UP}$ ≤ 1 kΩ | No pop | Frequency 1 |
| Weak High | 20 kΩ ≤ $R_{UP}$ ≤ 200 kΩ | No pop | Frequency 2 |
| Weak Low | No pop | 20 kΩ ≤ $R_{DOWN}$ ≤ 200 kΩ | Frequency 3 |
| Low | No pop | 0 Ω ≤ $R_{DOWN}$ ≤ 1 kΩ | Frequency 4 |

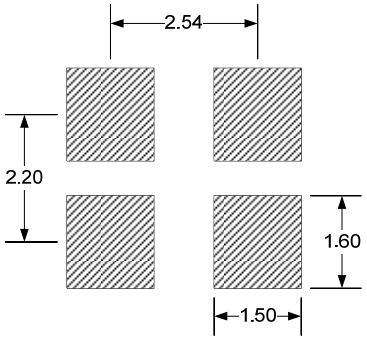
Notes for both FS/OE tables above:
1. If the internal pull-up resistor order option is NOT selected, an MCU internal pull-up resistor or an external pull-up resistor should be used. See data sheet for more information.
2. The parallel combination of all pull-up resistors on the FS/OE pin including the optional internal pull-up resistor must be > 20 kΩ to select Weak High.
3. If the Si50x internal pull-up resistor is enabled with no other external OE connections, the OE state will be detected as “Weak High”, selecting Frequency 2 by default.

## Package Dimensions and Landing Patterns

### 3.2 mm x 5 mm 4-pin DFN Dimensions

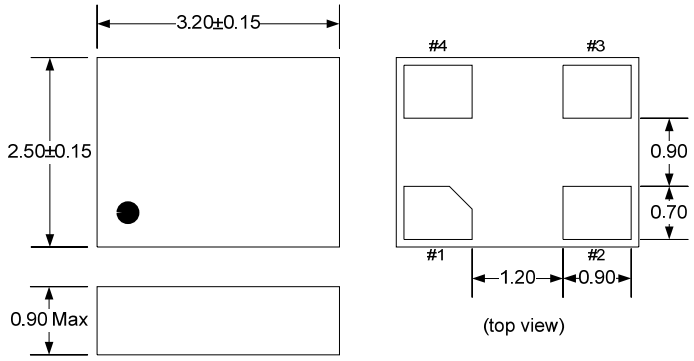



### 3.2 mm x 5 mm 4-pin DFN Landing Pattern

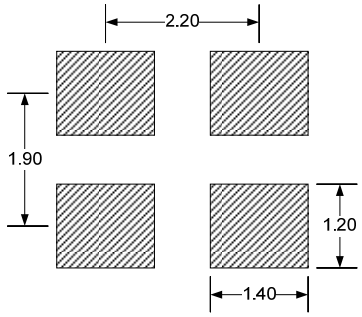



Note: The 3.2 x 5 mm package is delivered as a 3.2 x 4 mm package and is drop-in compatible to industry-standard 3.2 x 5 landing patterns.

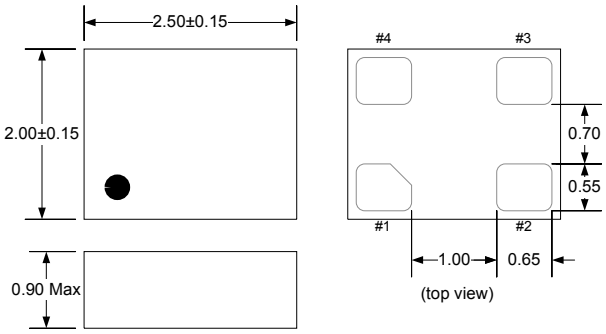
### 2.5 mm x 3.2 mm 4-pin DFN Dimensions



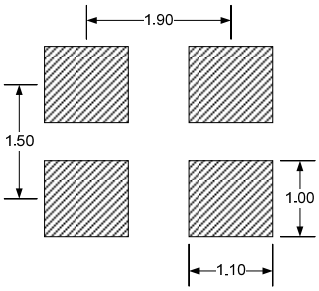

### 2.5 mm x 3.2 mm 4-pin DFN Landing Pattern




### 2 mm x 2.5 mm 4-pin DFN Dimensions

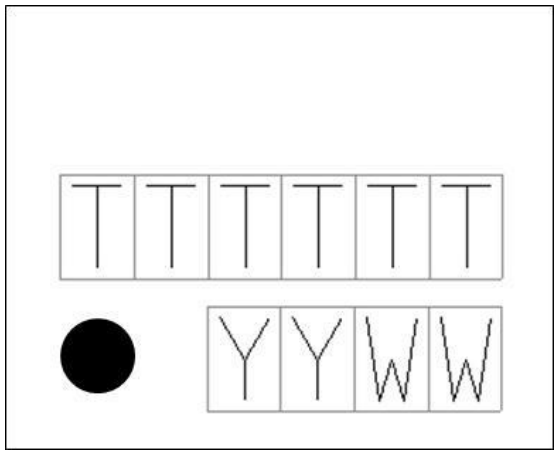



### 2 mm x 2.5 mm 4-pin DFN Landing Pattern



## Package Top Marks and Explanations

### 3.2 mm x 5 mm Top Mark




### 3.2 mm x 5 mm Top Mark Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Font:** | 0.66 mm Right-Justified | |
| **Line 1 Marking:** | TTTTTT=Trace Code | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 2 Marking:** | Circle=0.5mm diameter Left-Justified | Pin 1 Indicator |
| | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the build date. |

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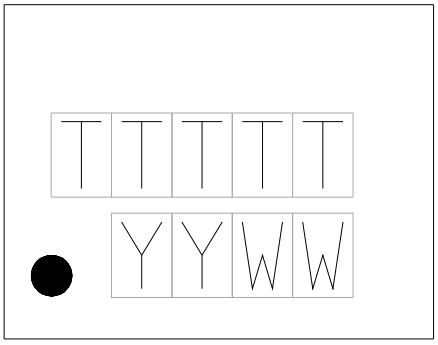
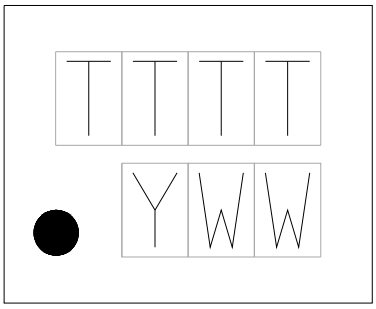
### 2.5 mm x 3.2 mm Top Mark




### 2.5 mm x 3.2 mm Top Mark Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Font:** | 0.50 mm Right-Justified | |
| **Line 1 Marking:** | TTTTT=Trace Code | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 2 Marking:** | Circle=0.3 mm diameter Left-Justified | Pin 1 Indicator |
| | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the build date. |

### 2 mm x 2.5 mm Top Mark




### 2 mm x 2.5 mm Top Mark Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Font:** | 0.50 mm Right-Justified | |
| **Line 1 Marking:** | TTTT=Trace Code | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 2 Marking:** | Circle=0.3 mm diameter Left-Justified | Pin 1 Indicator |
| | Y = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the build date. |

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