

# N-Channel 60 V (D-S), 175 °C MOSFET, Logic Level

## PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>
60	0.0093 at $V_{GS} = 10$ V	50
	0.0122 at $V_{GS} = 4.5$ V	50

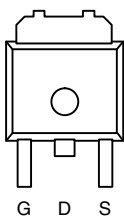
## FEATURES

- 175 °C Junction Temperature
- TrenchFET<sup>®</sup> Power MOSFET
- Material categorization:  
For definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT

TO-252

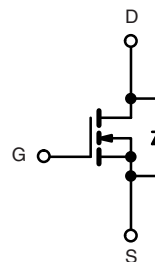


Top View

Drain Connected to Tab

### Ordering Information:

SUD50N06-09L-E3 (Lead (Pb)-free)



N-Channel MOSFET

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_J = 175$ °C) <sup>b</sup>	$I_D$	50	A
		50 <sup>a</sup>	
Pulsed Drain Current	$I_{DM}$	100	
Continuous Source Current (Diode Conduction)	$I_S$	50 <sup>a</sup>	
Avalanche Current	$I_{AS}$	50	
Single Avalanche Energy (Duty Cycle $\leq 1$ %)	$E_{AS}$	125	mJ
Maximum Power Dissipation	$P_D$	136	W
		3 <sup>b</sup> , 8.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	15	18	°C/W
		40	50	
Maximum Junction-to-Case	$R_{thJC}$	0.85	1.1	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

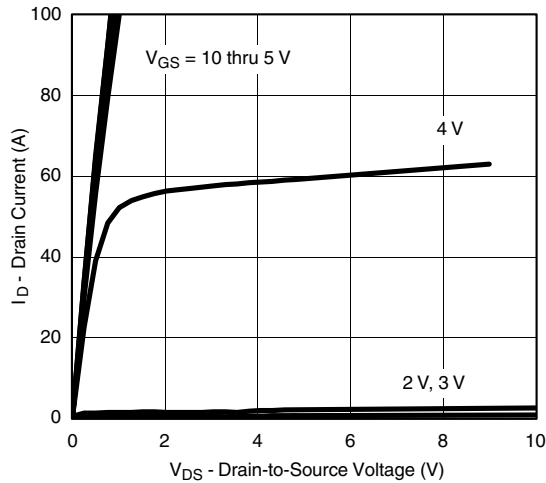
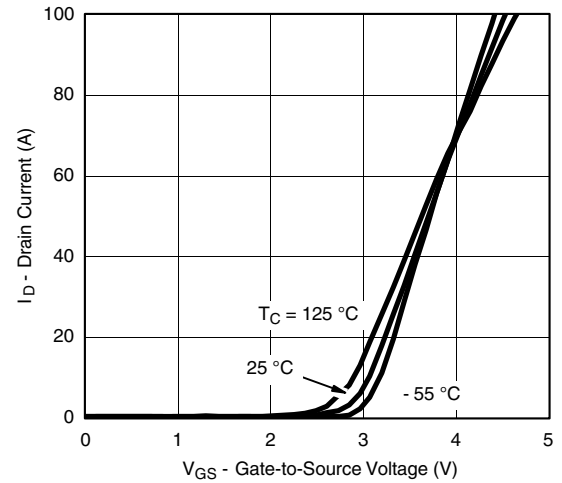
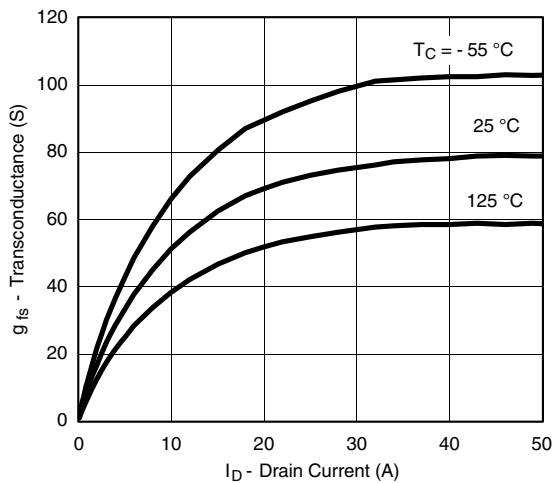
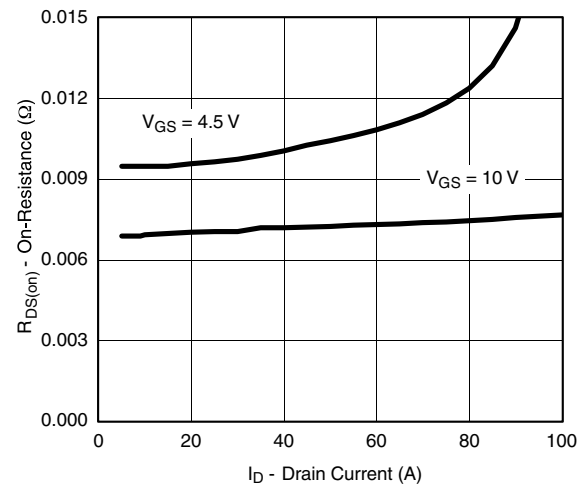
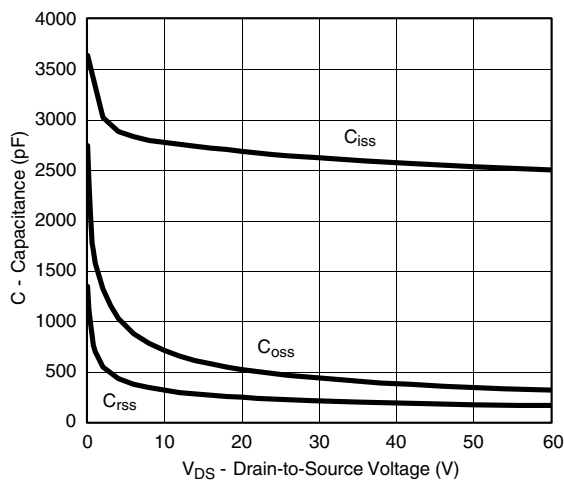
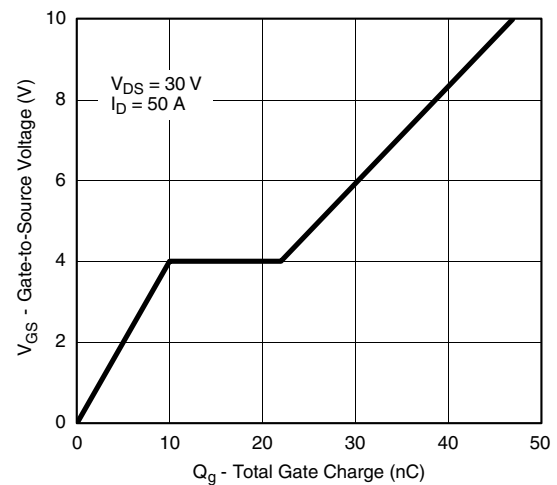
c.  $t \leq 10$  s.

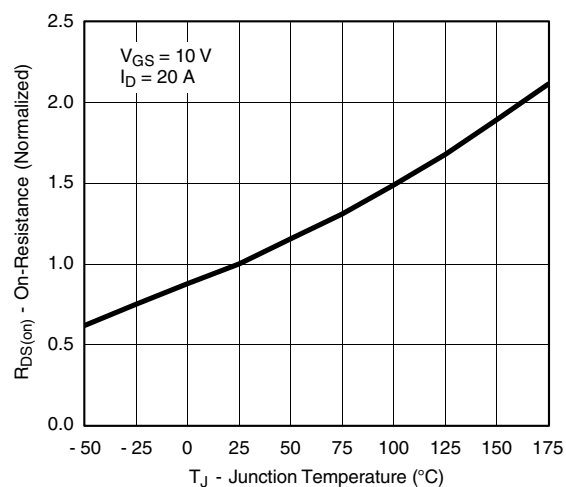
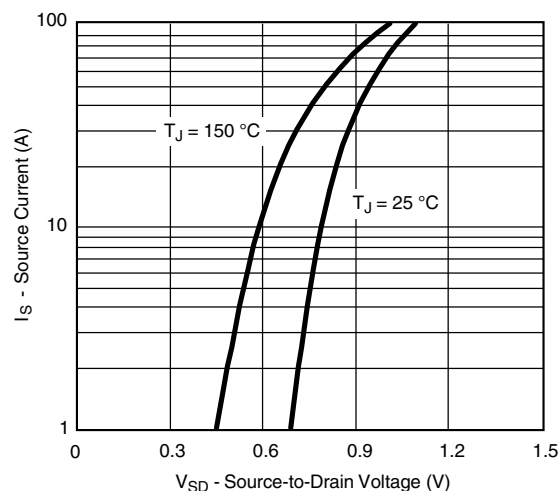
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	2	3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0074	0.0093	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C			0.0160	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C			0.0200	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A			0.0122	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		60		S
Dynamic						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		2650		pF
Output Capacitance	C <sub>oss</sub>			470		
Reverse Transfer Capacitance	C <sub>rss</sub>			225		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		47	70	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			10		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			12		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 0.6 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 2.5 Ω		10	20	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			15	25	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			35	50	
Fall Time <sup>c</sup>	t <sub>f</sub>			20	30	
Source-Drain Diode Ratings and Characteristics (T <sub>C</sub> = 25 °C)						
Pulsed Current	I <sub>SM</sub>				100	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		1	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs		45	100	ns

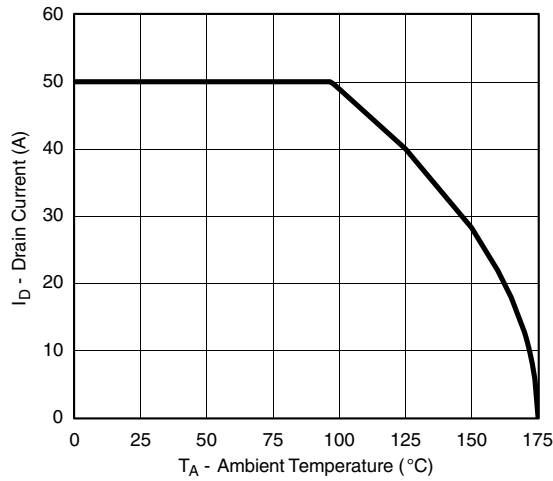
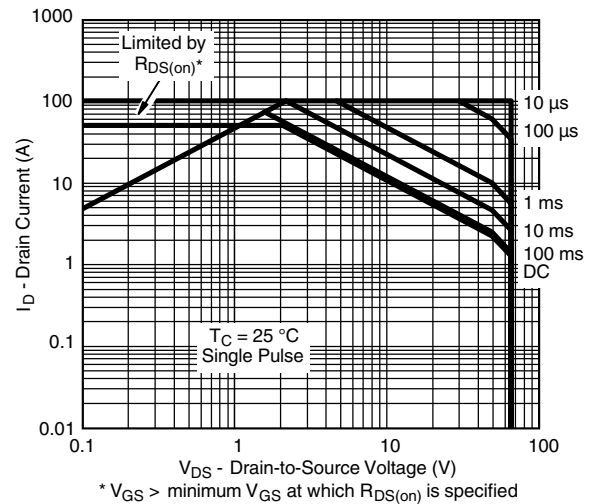
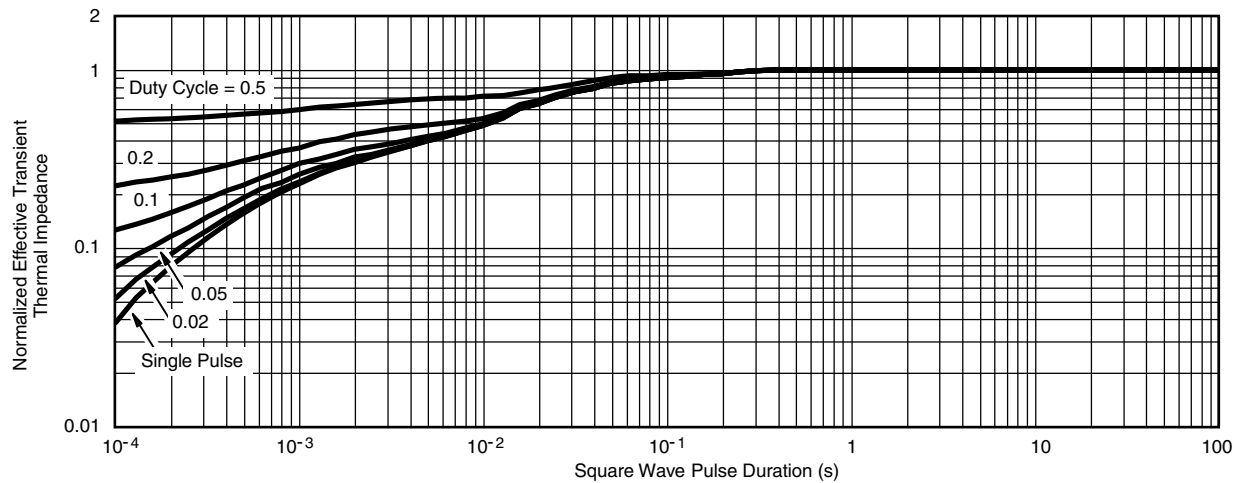
## Notes:

- a. For design aid only; not subject to production testing.  
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C unless noted)**Output Characteristics****Transfer Characteristics****Transconductance****On-Resistance vs. Drain Current****Capacitance****Gate Charge**

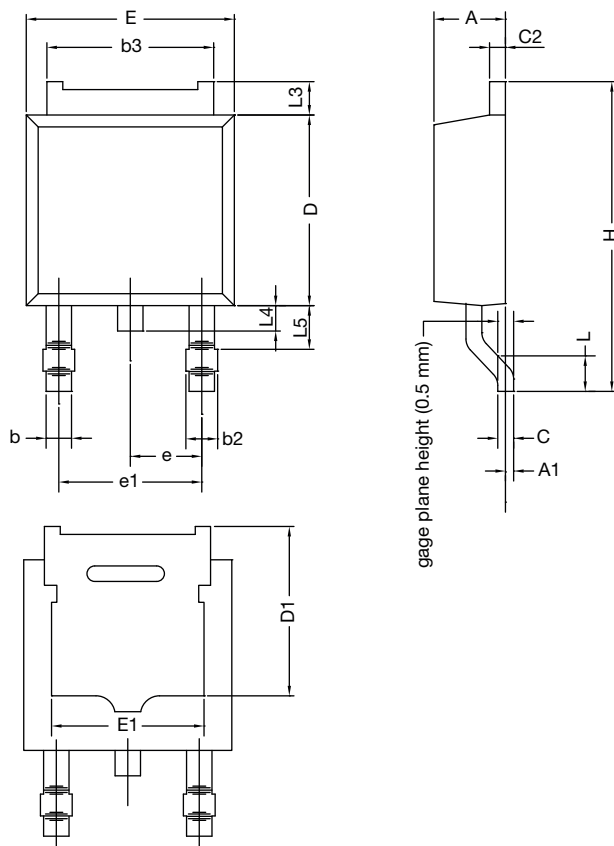
**TYPICAL CHARACTERISTICS** (25 °C unless noted)**On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage**

**THERMAL RATINGS****Maximum Drain Current vs. Ambient Temperature****Safe Operating Area****Normalized Thermal Transient Impedance, Junction-to-Case**

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## TO-252AA Case Outline

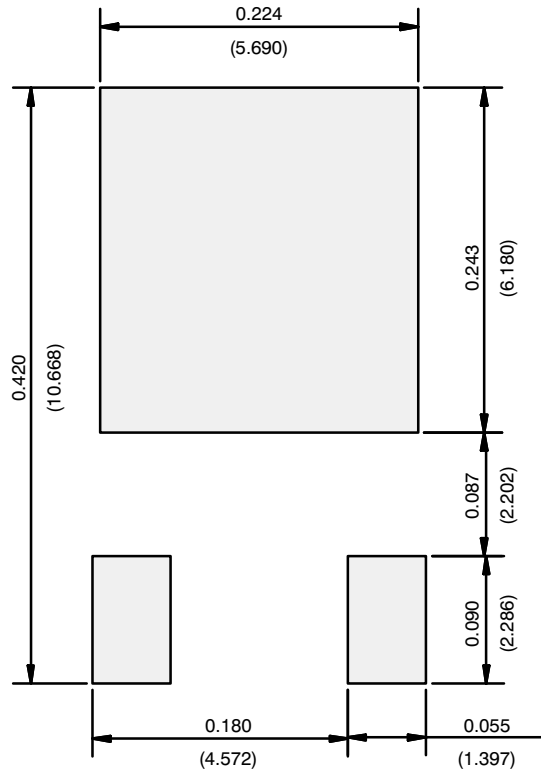


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

### Notes

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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