Memory/Clock Drivers

MH0026/MH0026C 5 MHz two phase MOS clock driver

general description

The MH0026/MH0026C is a low cost monolithic high speed two phase MOS clock driver and interface circuit. Unique circuit design along with advanced processing provide both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 series gates and flip-flops or from drivers such as the DM8830 or DM7440. The MH0026 is intended for applications in which the output pulse width is logically controlled: i.e., the output pulse width is equal to the input pulse width.

features

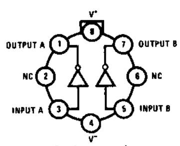
- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on load
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

The MH0026 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16 bit MM1103 RAM memory system. Information on the correct usage of the MH0026 in these as well as other systems is included in the application section starting on page 5. A thorough understanding of its usage will insure optimum performance of the device.

The device is available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt TO-8 packages.

connection diagrams

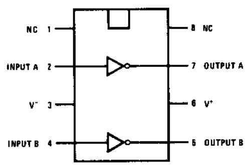
Metal Can Package



Note: Pin 4 connected to case.
TOP VIEW

Order Number MH0026H or MH0026CH
See Package 11

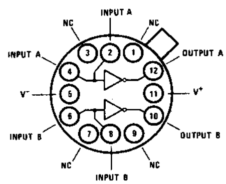
Dual-In-Line Package



TOP VIEW

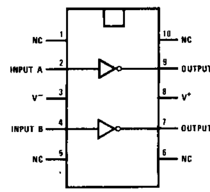
Order Number MH0026CN
See Package 20

Metal Can Package



Order Number MH0026G or MH0026CG
See Package 6

Flat Package

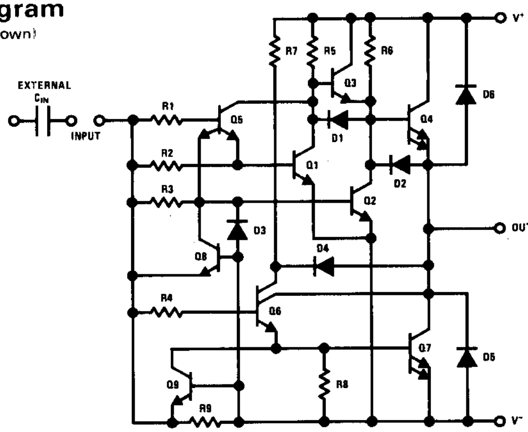


TOP VIEW

Order Number MH0026F or MH0026CF
See Package 3

schematic diagram

(1/2 of Circuit Shown)



absolute maximum ratings

$V^+ - V^-$ Differential Voltage		22V
Input Current		100 mA
Input Voltage ($V_{IN} - V^-$)		5.5V
Peak Output Current		1.5A
Power Dissipation		See curves
Operating Temperature Range	MH0026	−55°C to +125°C
	MH0026C	0°C to 85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics (Notes 1 & 2)

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Logic "1" Input Voltage	$V_{OUT} = V^- + 1.0V$	2.5	1.5		V
Logic "1" Input Current	$V_{IN} - V^- = 2.5V$, $V_{OUT} = V^- + 1.0V$		10	15	mA
Logic "0" Input Voltage	$V_{OUT} = V^+ - 1.0V$		0.6	0.4	V
Logic "0" Input Current	$V_{IN} - V^- = 0V$, $V_{OUT} = V^+ - 1.0V$		−0.005	−10	μA
Logic "0" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$, $V_{IN} = -11.6$	4.0	4.3		V
Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$	$V^+ - 1.0$	$V^+ - 0.7$		V
Logic "1" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$, $V_{IN} = -9.5V$		−11.5	−11.0	V
Logic "1" Output Voltage	$V_{IN} - V^- = 2.5V$		$V^- + 0.5$	$V^- + 1.0$	V
"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.5V$		30	40	mA
"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0.0V$		10	100	μA

ac electrical characteristics (Notes 1 & 2, AC test circuit, $T_A = 25°C$)

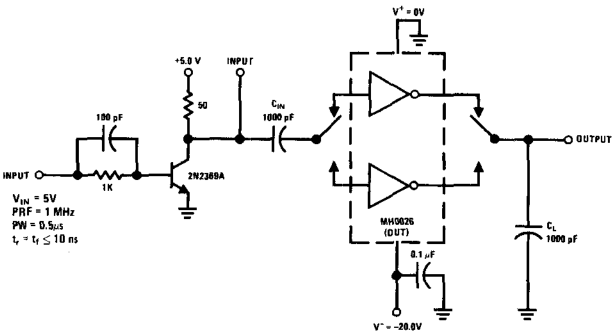
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Delay (t_{ON})		5.0	7.5	12	ns
Turn-Off Delay (t_{OFF})		5.0	12	15	ns
Rise time (t_r) – Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		12		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		15	18	ns
	$C_L = 1000$ pF		20	35	ns
Falltime (t_f) – Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		10		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		12	16	ns
	$C_L = 1000$ pF		17	25	ns

Note 1: These specifications apply for $V^+ - V^- = 10V$ to $20V$, $C_L = 1000$ pF, over the temperature range −55°C to +125°C for the MH0026 and 0°C to +85°C for the MH0026C, unless otherwise specified.

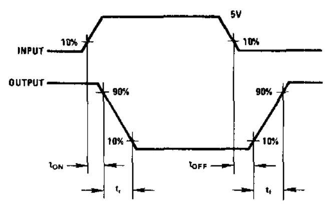
Note 2: All typical values for the $T_A = 25°C$.

Note 3: Rise and fall time are given for MOS logic levels; i.e., rise time is transistion from logic "0" to logic "1" which is voltage fall. See waveforms on the following pages.

ac test circuit

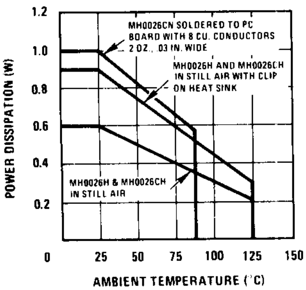


switching time waveforms

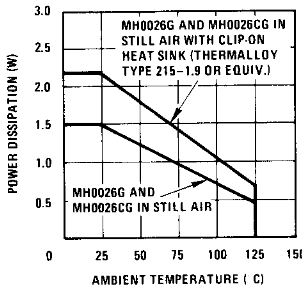


typical performance characteristics

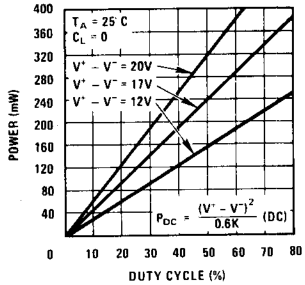
TO-5 & DIP Power Ratings



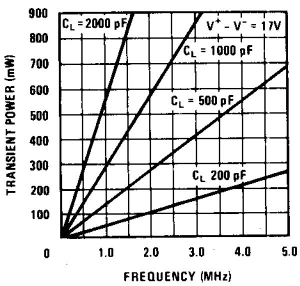
TO-8 Package Power Rating



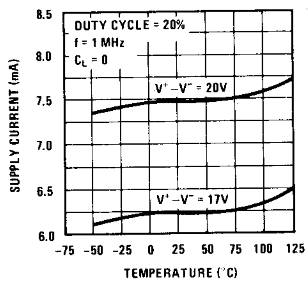
DC Power (P_{DC}) vs Duty Cycle



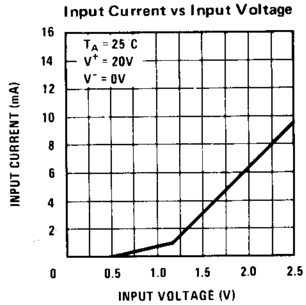
Transient Power (P_{AC}) vs Frequency



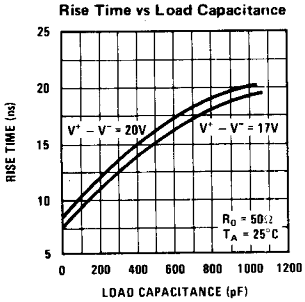
Supply Current vs Temperature



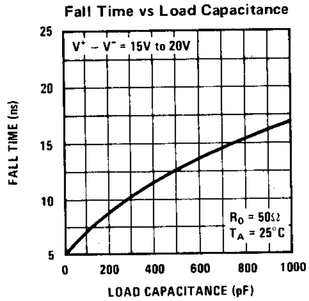
Input Current vs Input Voltage



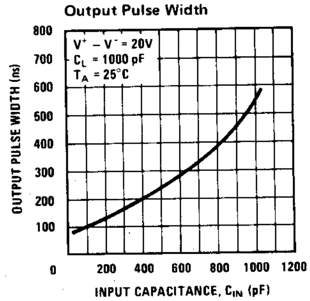
Rise Time vs Load Capacitance



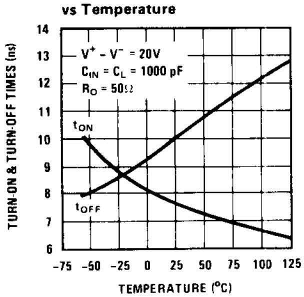
Fall Time vs Load Capacitance



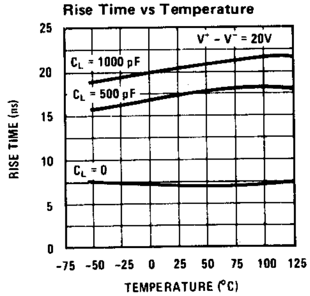
Optimum Input Capacitance vs Output Pulse Width



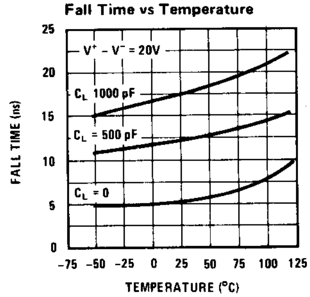
Turn-On & Turn-Off Time vs Temperature



Rise Time vs Temperature

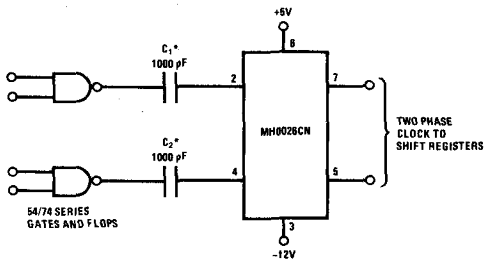


Fall Time vs Temperature



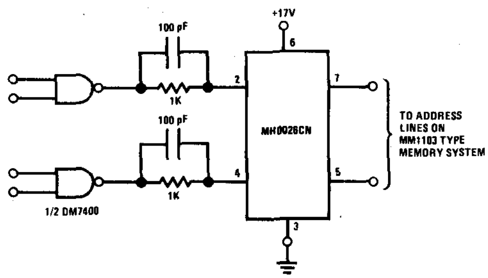
typical applications (cont.)

AC Coupled MOS Clock Driver

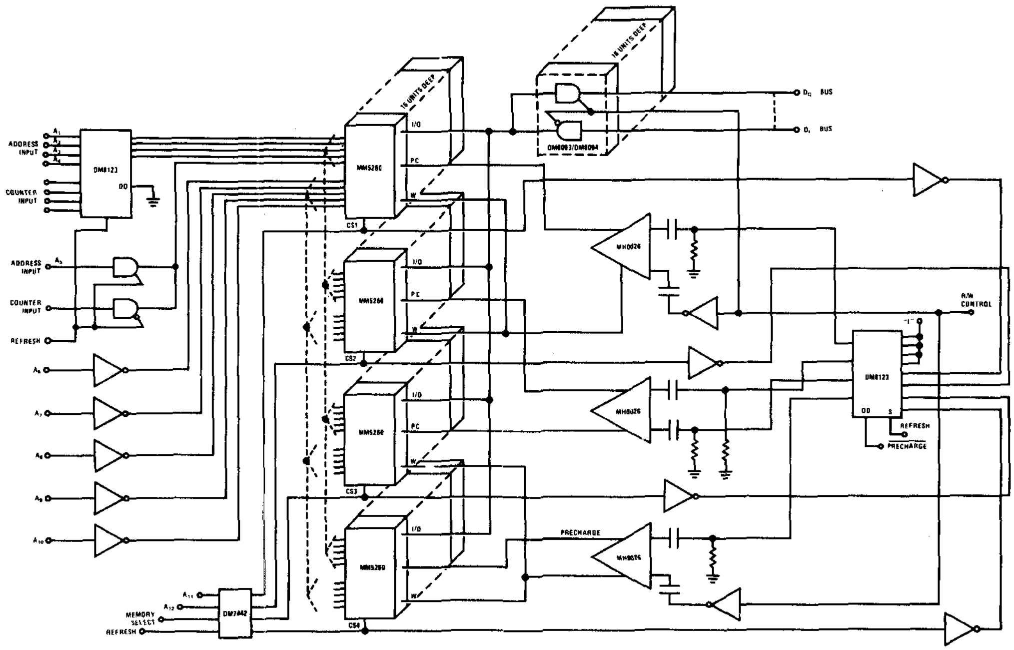


*See applications section for detailed information on input/output design criterion.

DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

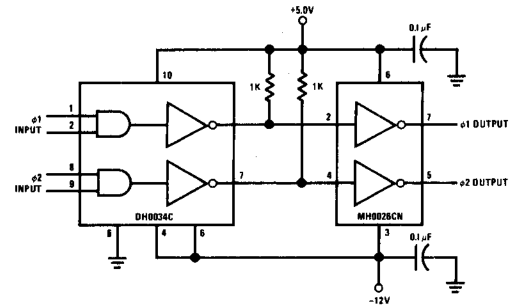


Precharge Driver for MOS RAM Memories

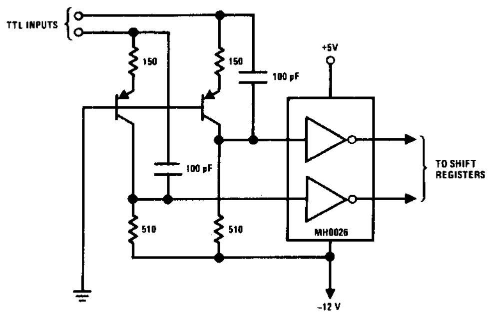


typical applications

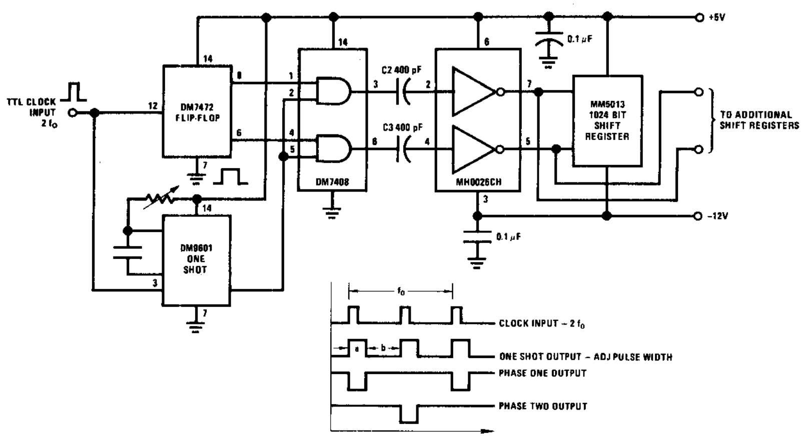
DC Coupled MOS Clock Driver



Transistor Coupled MOS Clock Driver



Logically Controlled AC Coupled Clock Driver



application information

1.0 Introduction

The MH0026 is capable of delivering 30 watts peak power (1.5 amps at 20V needed to rapidly charge large capacitative loads) while its package is limited to the watt range. This section describes the operation of the circuit and how to obtain optimum system performance. If additional design information is required, please contact your local National field application engineer.

2.0 Theory of Operation

Conventional MOS clock drivers like the MH0013 and similar devices have relied on the circuit configuration in Figure 1. The AC coupling of an input pulse allows the device to work over a wide range of supplies while the output pulse width may be controlled by the time constant $-R_1 \times C_1$.

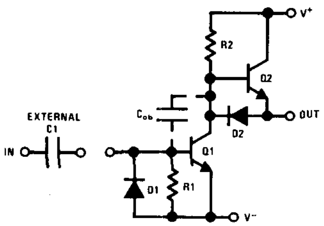


FIGURE 1. Conventional MOS Clock Drive

D_2 provides 0.7V of dead-zone thus preventing Q_1 and Q_2 from conducting at the same time. In order to drive large capacitive loads, Q_1 and Q_2 are large geometry devices but C_{ob} now limits useful output rise time. A high voltage TTL output stage (Figure 2) could be used; however, during switching until the stored charge is removed from Q_1, both output devices conduct at the same time. This is familiar in TTL with supply line glitches in the order of 60 to 100 mA. A clock driver built this way would introduce 1.5 amp spikes into the supply lines.

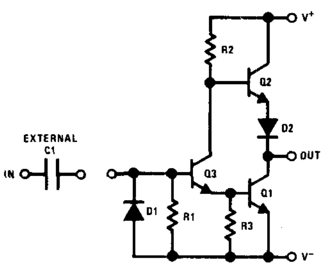


FIGURE 2. Alternate MOS Clock Drive

Unique circuit design and advanced semiconductor processing overcome these clasic problems allowing the high volume manufacture of a device, the MH0026, that delivers 1.5A peak output currents with 20ns rise and fall times into 1000pF loads. In a simplified diagram, D_1 (Figure 3) provides 0.7V dead zone so that Q_3 is turned ON for a rising input pulse and Q_2 OFF prior to Q_1 turning ON a few nanoseconds later. D_2 prevents zenering of the emitter-base junction of Q_2 and provides an initial discharge path for the load via Q_3. During a falling input, the stored charge in Q_3 is used beneficially to keep Q_3 ON thus preventing Q_2 from conducting until Q_1 is OFF. Q_1 stored charge is quickly discharged by means of common-base transistor Q_4.

The complete circuit of the MH0026 (see schematic on page 1) basically makes Darlingtons out of each of the transistors in Figure 3.

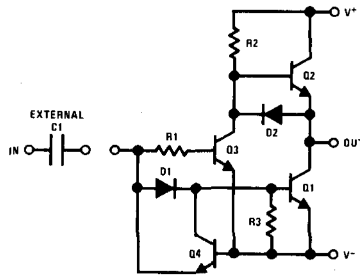


FIGURE 3. Simplified MH0026

When the output of the TTL input element (not shown) goes to the logic "1" state, current is supplied through C_{IN} to the base of Q_1 and Q_2 turning them ON, and Q_3 and Q_4 OFF when the input voltages reaches 0.7V. Initial discharge of the load as well as E-B protection for Q_3 and Q_4 are provided by D_1 and D_2. When the input voltage reaches about 1.5V, Q_6 and Q_7 begin to conduct and the load is rapidly discharged by Q_7. As the input goes low, the input side of C_{IN} goes negative with respect to V^- causing Q_8 and Q_9 to conduct momentarily to assure rapid turn-off of Q_2 and Q_7 respectively. When Q_1 and Q_2 turn OFF, Darlington connected Q_3 and Q_4 rapidly charge the load toward V^+ volts. R_6 assures that the output will reach to within one V_{BE} of the V^+ supply.

The real secret of the device's performance is proper selection of transistor geometries and resistor values so that Q_4 and Q_7 do not conduct at the same time while minimizing delay from input to output.

3.0 Power Dissipation Considerations

There are four considerations in determining power dissipations.

1. Average DC power
2. Average AC power
3. Package and heat sink selection
4. Remember—2 drivers per package

application information (cont.)

The total average power dissipated by the MH0026 is the sum of the DC power and AC transient power. The total must be less than given package power ratings.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Since the device dissipates only 2mW with output voltage high (MOS logic "0"), the dominating factor in average DC power is duty cycle or the percent of time in output voltage low state (MOS logic "1"). Percent of total power contributed by P_{DC} is usually neglible in shift register applications where duty cycle is less than 25%. P_{DC} dominates in RAM address line driver applications where duty cycle can exceed 50%.

3.1 DC Power (per driver)

DC Power is given by:

$$P_{DC} = (V^+ - V^-) \times (I_{S(Low)}) \times \left(\frac{\text{ON time}}{\text{OFF time} - \text{ON time}}\right)$$

or P_{DC} = (Output Low Power) X (Duty Cycle)

where: $I_{S(LOW)} = I_S$ @ $(V^+ - V^-)$

Example 1: $(V^+ = +5V, V^- = -12V)$

a) Duty cycle = 25%, therefore

$P_{DC} = 17V \times 40mA \times 17/20 \times 25\%$

P_{DC} = 145mW worst-case, each side

P_{DC} = 109mW typically

b) Duty cycle = 5%

P_{DC} = 21mW

c) See graph on page 3

The above illustrates that for shift register applications, the minimum clock width allowable for the given type of shift register should be used in order to drive the largest number of registers per clock driver.

Example 2: $(V^+ = +17V, V^- = GND)$:

a) Duty cycle = 50%

P_{DC} = 290mW worst-case

P_{DC} = 218mW typically

b) Duty cycle = 100%

P_{DC} = 580mW

Thus for RAM address line applications, package type and heat sink technique will limit drive capability rather than AC power.

3.2 AC Transient Power (per driver)

AC Transient power is given by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L$$

where: f = frequency of operation

C_L = Load capacitance (including all strays and wiring)

Example 3: $(V^+ = +5V, V^- = -12V)$

$$P_{AC} = 17 \times 17 \times f(\text{MHz}) \times 10^6 \times C_L(\text{nF}) \times 10^{-9}$$

P_{AC} = 290mW per MHz per 1000pF

Thus at 5MHz, a 1000pF load will cause any driver to dissipate one and one half watts. For long shift registers, a driver with the highest package power rating will drive the largest number of bits for the lowest cost per bit.

3.3 Package Selection

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs on page 3 illustrate derating for various operating temperatures.

3.31 TO-5 ("H") Package: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 900mW with clip on heat sink (derate at 6.0mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving capability by 50%.

3.32 8-Pin ("N") Molded Mini-DIP: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 1.0 watt soldered to PC board (derate at 6.6mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600mW when mounted in a socket and not one watt until it is soldered down.)

3.33 TO-8 ("G") Package: Rated at 1.5 watts still air (derate at 10mW/°C above 25°C) and 2.3 watts with clip on heat sink (Wakefield type 215-1.9 or equivalent–derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

application information (cont.)

3.4 Summary—Package Power Considerations

The maximum capacitative load that the MH0026 can drive is thus determined by package type, heat sink technique, ambient temperature, AC power (which is proportional to frequency and capacitive load) and DC power (which is principally determined by duty cycle). Combining equations previously given, the following formula is valid for any clock driver with negligible input power and negligible power in output high state:

$$C_L \text{ (max in pF)} = \frac{10^{-3}}{n} \times \frac{P_{max(mW)}(T_A,\text{pkg}) \times R_{eq} - (V^+ - V^-)^2 \times (Dc) \times 10^3}{(V^+ - V^-)^2 \times R_{eq} \times f(\text{MHz})}$$

or:

$$C_L \text{ (max in pF)} = .5 \times 10^{-3} \times \frac{P_{max}(\text{mW}) \times 500 - V_S^2 \times Dc \times 10^3}{V_S^2 \times 500 \times f(\text{MHz})}$$

Where: n = number of drivers per pkg. (2 for the MH0026)

$P_{max(mW)}(T_A,\ \text{pkg})$ = Package power rating in milliwatts for given package, heat sink, and max, ambient temperature (See graphs)

R_{eq} = equivalent internal resistance

$R_{eq} = (V^+ - V^-)/I_{S(Low)}$ = 500 ohms (worst case over temperature for the MH0026 or 660 ohms typically)

$V_S = (V^+ - V^-)$ = total supply voltage across device

Dc = Duty Cycle =

$$\frac{\text{Time in output low state}}{\text{Time in output low + Time in output high state}}$$

Table I illustrates MH0026 drive capability under various system conditions.

4.0 Pulse Width Control

The MH0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + \frac{t_r + t_f}{2} = PW_{IN} + 25\text{ns}$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the MH0026 discharges to just above the devices threshold (about 1.5V). If the input is allowed to discharge below the threshold, t_{OFF} and t_f will be degraded. The graph on page 3 shows optimum values for C_{IN} vs desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN} = (2 \times 10^{-3})\ (PW)_{OUT}$$

For an output pulse width of 500ns, the optimum value for C_{IN} is:

$$C_{IN} = (2 \times 10^{-3})(500 \times 10^{-9}) \cong 1000\text{pF}$$

TABLE 1. Worst Case Maximum Drive Capability for MH0026*

PACKAGE TYPE		TO-8 WITH HEAT SINK		TO-8 FREE AIR		MINI-DIP SOLDERED DOWN		TO-5 AND MINI-DIP FREE AIR	
Max. Operating Frequency ↓	Max. Ambient Temp. → / Duty Cycle	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C
100kHz	5%	30 k	24 k	19 k	15 k	13 k	10k	7.5k	5.8k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2.7k	2k	1.5k	1.1k
1MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	430
2MHz	25%	1.4k	1.1k	850	650	550	400	280	190
5MHz	25%	620	470	380	290	240	170	120	80
10MHz	25%	280	220	170	130	110	79	—	—

***Note:** Values in pF and assume both sides in use as non-overlaping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$. For loads greater than 1200 pF, rise and fall times will be limited by output current; see Section 5.0.

application information (cont.)

5.0 Rise & Fall Time Considerations (Note 3)

The MH0026's peak output current is limited to 1.5A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leqslant 1.5A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V)(250 \times 10^{-12} + C_L)$$

Where: ΔV = The change in voltage across C_L

$\cong V^+ - V^-$

C_L = The load capacitance

For $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20V)(250 \times 10^{-12} + 10^{-12})$$
$$= 25ns$$

For small values of C_L, equation above predicts optimistic values for t_r. The graph on page 3 shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2R\left(C_S + \frac{C_L}{h_{FE} + 1}\right)$$

6.0 Clock Overshoot

The output waveform of the MH0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the ouput of the MH0026. The critical valve for $R_s = 2\sqrt{L/C\ell}$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_s is readily determined emperically, and values typically range between 10 and 51 ohms. R_s does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2R_SC_L$$

7.0 Clock Line Cross Talk

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the MH0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output has to drop at least 2 V_{BE} before Q_3 and Q_4 come on and pull the output back to V^+. A simple method for eliminating or minimizing this effect is to add bleed resistors between the MH0026 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2k and 10k ohms.

8.0 Power Supply Decoupling

Power supply decoupling is a widespread and accepted practice. Decoupling of V^+ to V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each MH0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.