NTMD2P01R2

Power MOSFET
-2.3 Amps, -16 Volts

Dual SOIC−8 Package

Features

- High Efficiency Components in a Single SOIC−8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$
- Logic Level Gate Drive
- SOIC−8 Surface Mount Package,
  Mounting Information for SOIC−8 Package Provided
- Pb−Free Packages are Available

Applications

- Power Management in Portable and Battery−Powered Products, i.e.:
  Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−16	V
Gate−to−Source Voltage − Continuous	V_{GS}	±10	V
Thermal Resistance − Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 100°C Pulsed Drain Current (Note 4)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	175 0.71 −2.3 −1.45 −9.0	°C/W W A A A
Thermal Resistance − Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 100°C Pulsed Drain Current (Note 4)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	105 1.19 −2.97 −1.88 −12	°C/W W A A A
Thermal Resistance − Junction−to−Ambient (Note 3) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 100°C Pulsed Drain Current (Note 4)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	62.5 2.0 −3.85 −2.43 −15	°C/W W A A A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = −16 Vdc, V_{GS} = −4.5 Vdc, Peak I_L = −5.0 Apk, L = 28 mH, R_G = 25 Ω)	E_{AS}	350	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Minimum FR−4 or G−10 PCB, Steady State.
2. Mounted onto a 2″ square FR−4 Board (1 in sq, 2 oz Cu 0.06″ thick single sided), Steady State.
3. Mounted onto a 2″ square FR−4 Board (1 in sq, 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

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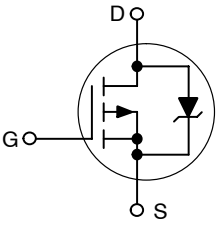
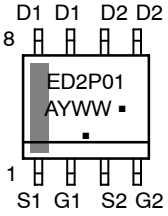
V_{DSS}	$R_{DS(ON)}$ Typ	I_D Max
−16 V	100 mΩ @ −4.5 V	−2.3 A

P−Channel



SOIC−8
SUFFIX NB
CASE 751
STYLE 11

MARKING DIAGRAM*
AND PIN ASSIGNMENT



ED2P01 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
NTMD2P01R2	SOIC−8	2500/Tape & Reel
NTMD2P01R2G	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = −250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 −16 −	 − −12.7	 − −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = −16 Vdc, V_{GS} = 0 Vdc, T_J = 25°C) (V_{DS} = −16 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 − −	 − −	 −1.0 −10	μAdc
Gate−Body Leakage Current (V_{GS} = −10 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	 −	 −	 −100	nAdc
Gate−Body Leakage Current (V_{GS} = +10 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	 −	 −	 100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = −250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 −0.5 −	 −0.90 2.5	 −1.5 −	Vdc mV/°C
Static Drain−to−Source On−State Resistance (V_{GS} = −4.5 Vdc, I_D = −2.4 Adc) (V_{GS} = −2.7 Vdc, I_D = −1.2 Adc) (V_{GS} = −2.5 Vdc, I_D = −1.2 Adc)		$R_{DS(on)}$	 − − −	 0.070 0.100 0.110	 0.100 0.130 0.150	Ω
Forward Transconductance (V_{DS} = −10 Vdc, I_D = −1.2 Adc)		g_{FS}	 −	 4.2	 −	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = −16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	540	750	pF
Output Capacitance		C_{oss}	−	215	325	
Reverse Transfer Capacitance		C_{rss}	−	100	175	
SWITCHING CHARACTERISTICS (Notes 6 and 7)						
Turn−On Delay Time	(V_{DD} = −10 Vdc, I_D = −2.4 Adc, V_{GS} = −4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	−	10	20	ns
Rise Time		t_r	−	35	65	
Turn−Off Delay Time		$t_{d(off)}$	−	33	60	
Fall Time		t_f	−	29	55	
Turn−On Delay Time	(V_{DD} = −10 Vdc, I_D = −1.2 Adc, V_{GS} = −2.7 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	−	15	−	ns
Rise Time		t_r	−	40	−	
Turn−Off Delay Time		$t_{d(off)}$	−	35	−	
Fall Time		t_f	−	35	−	
Total Gate Charge	(V_{DS} = −16 Vdc, V_{GS} = −4.5 Vdc, I_D = −2.4 Adc)	Q_{tot}	−	10	18	nC
Gate−Source Charge		Q_{gs}	−	1.5	−	
Gate−Drain Charge		Q_{gd}	−	5.0	−	
BODY−DRAIN DIODE RATINGS (Note 6)						
Diode Forward On−Voltage	(I_S = −2.4 Adc, V_{GS} = 0 Vdc) (I_S = −2.4 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 −	 −0.88 −0.75	 −1.0 −	Vdc
Reverse Recovery Time	(I_S = −2.4 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	−	37	−	ns
		t_a	−	16	−	
		t_b	−	21	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.025	−	μC

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

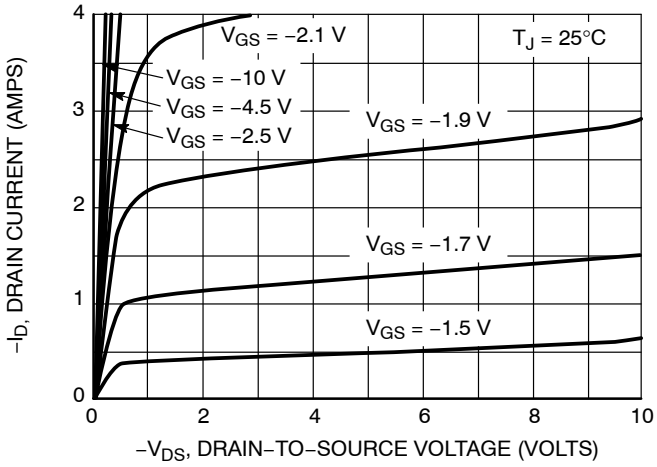


Figure 1. On−Region Characteristics.

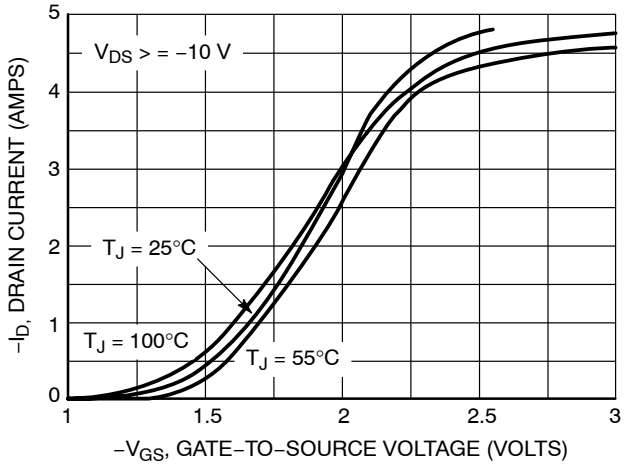


Figure 2. Transfer Characteristics.

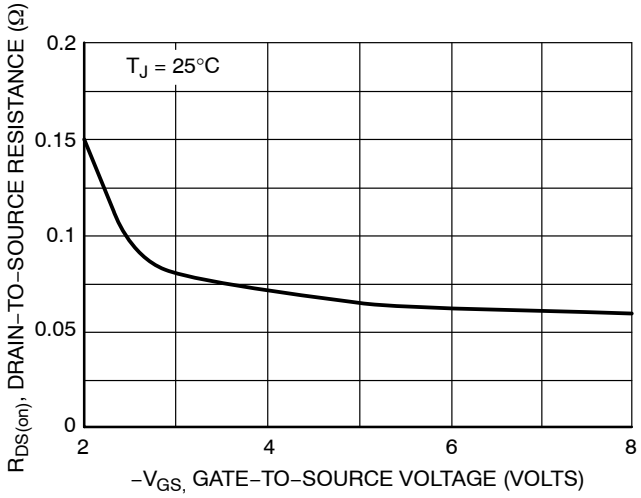


Figure 3. On−Resistance vs. Gate−to−Source Voltage.

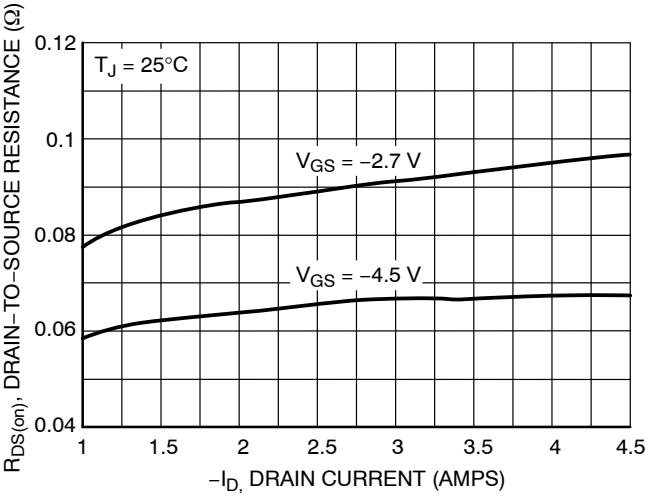


Figure 4. On−Resistance vs. Drain Current and Gate Voltage.

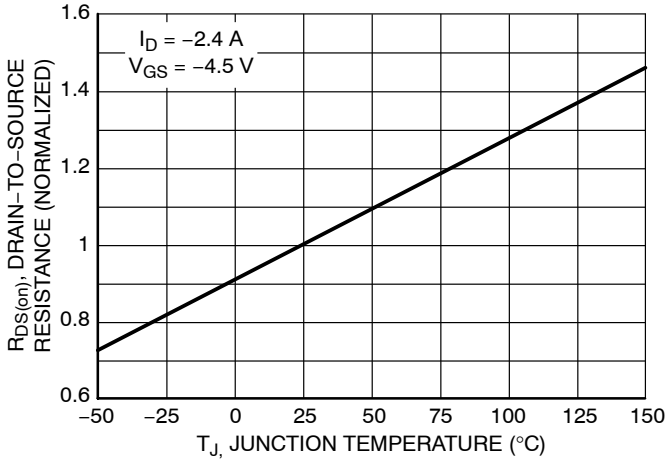


Figure 5. On−Resistance Variation with Temperature.

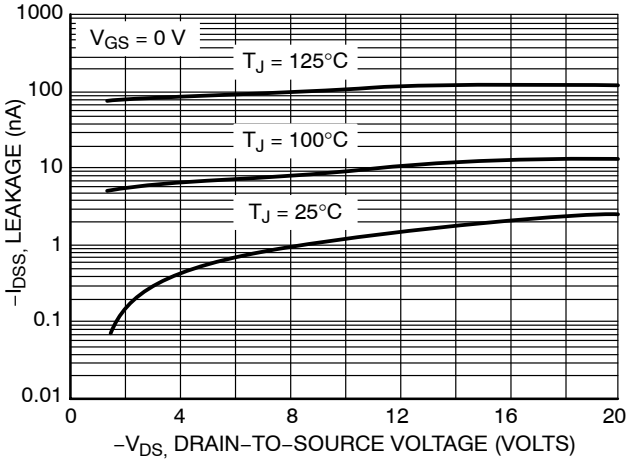


Figure 6. Drain−to−Source Leakage Current vs. Voltage.

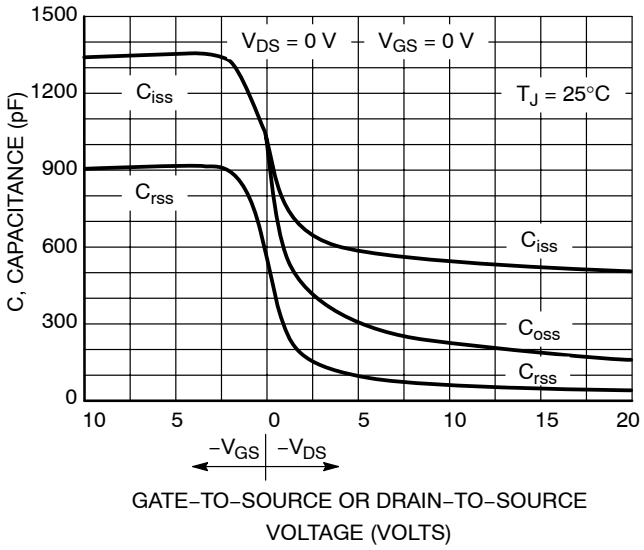


Figure 7. Capacitance Variation

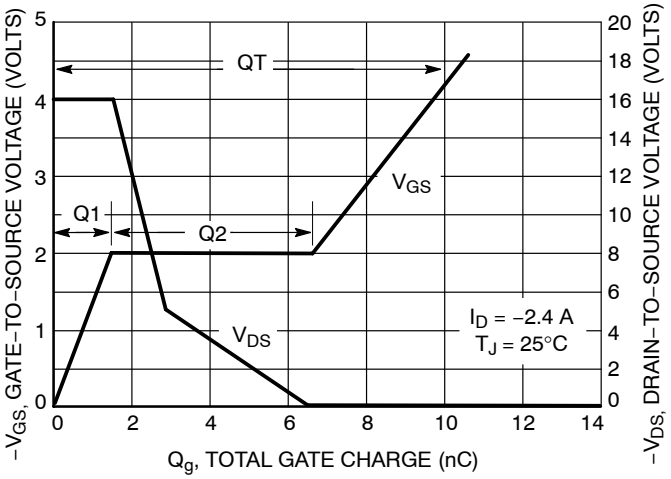


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

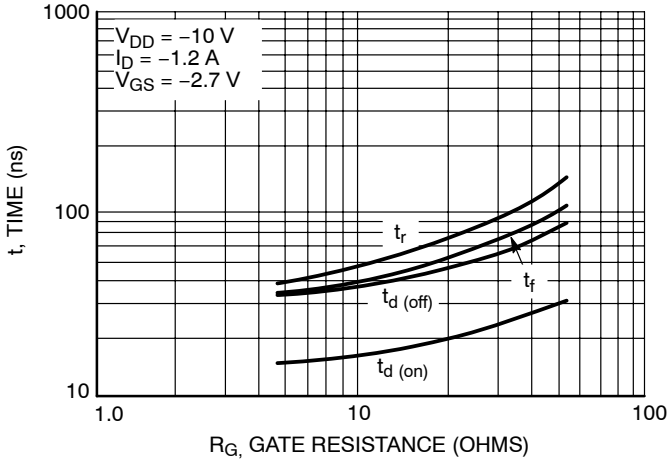


Figure 9. Resistive Switching Time Variation versus Gate Resistance

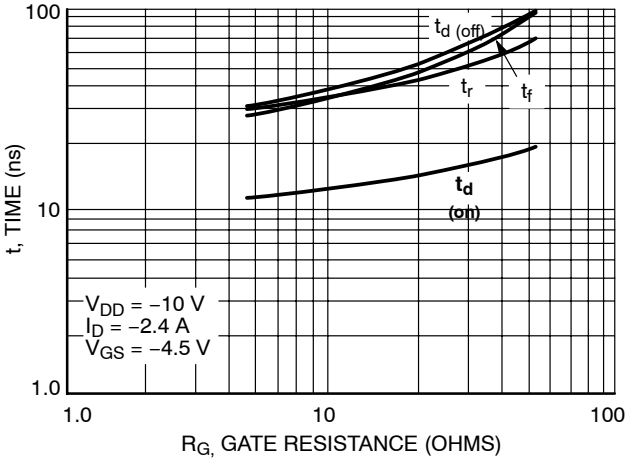


Figure 10. Resistive Switching Time Variation versus Gate Resistance

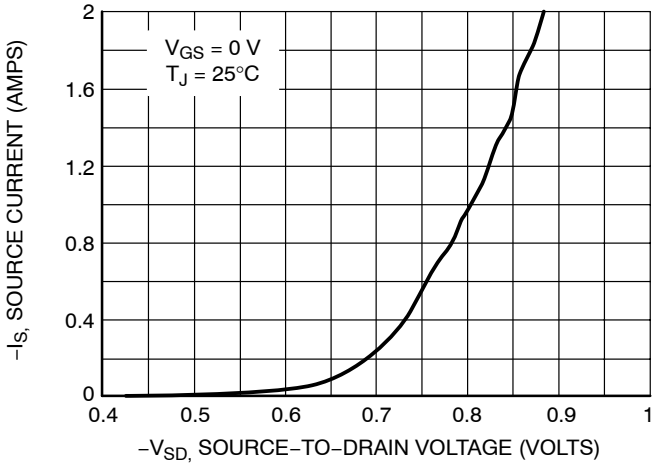


Figure 11. Diode Forward Voltage versus Current

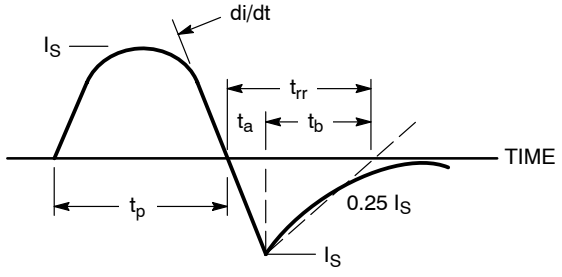


Figure 12. Diode Reverse Recovery Waveform

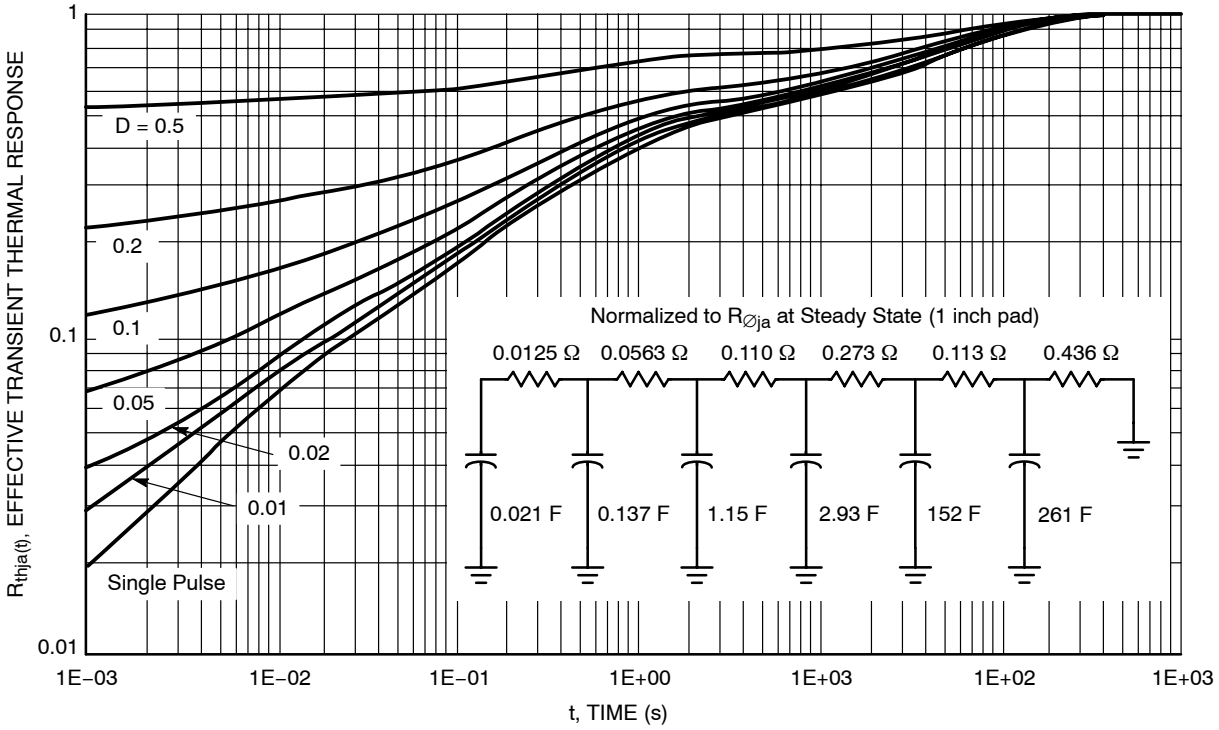
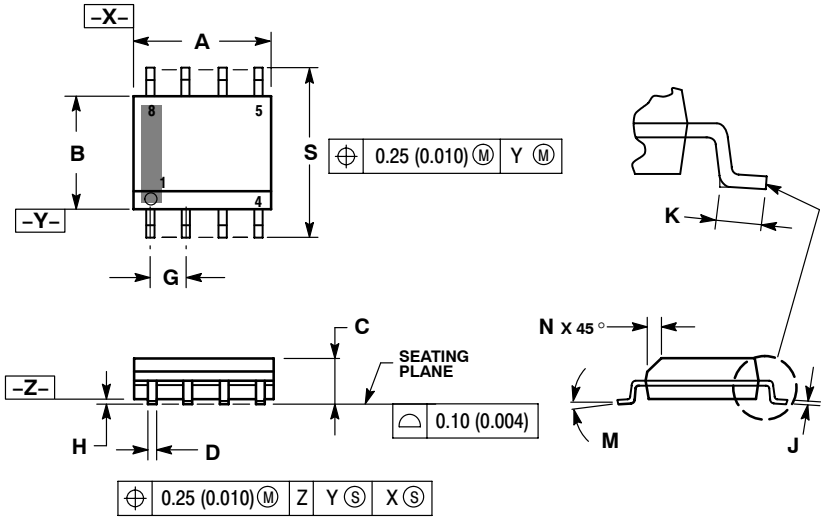


Figure 13. FET Thermal Response

NTMD2P01R2

PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AG

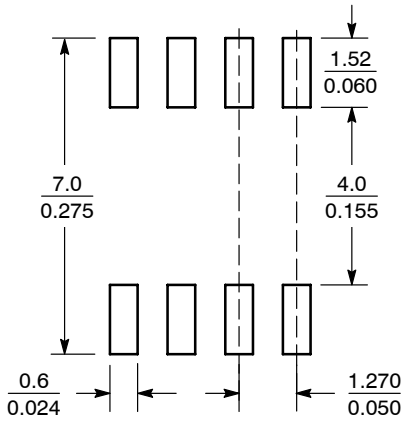


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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