TEXAS INSTRUMENTS

CY54/74FCT827T

10-Bit Buffer

SCCS034 - September 1994 - Revised March 2000

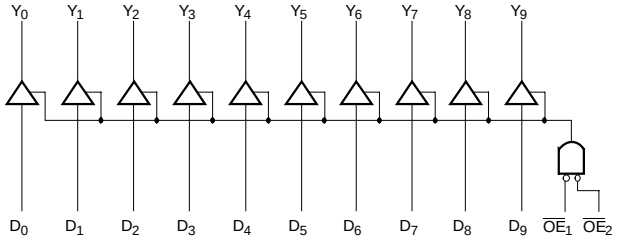
Features

- **Function, pinout, and drive compatible with FCT, F, and AM29827 logic**
- **FCT-C speed at 4.4 ns max. (Com'l)**
  FCT-A speed at 5.0 ns max. (Com'l)
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)

Functional Description

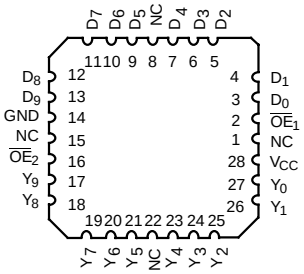
The FCT827T 10-bit bus driver provides high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility. The FCT827T is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All outputs are designed for low-capacitance bus loading in the high-impedance state and are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

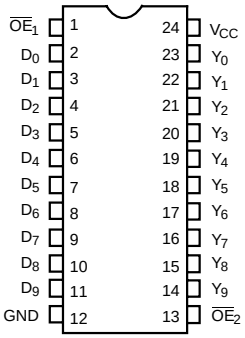


Pin Configurations

LCC/PLCC Top View



SOIC/QSOP Top View



Function Table[1]

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D	Y	Function
L L	L L	L H	L H	Transparent
H X	X H	X X	Z Z	Three-State

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Input Voltage.....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin).....120 mA

Power Dissipation 0.5W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	All	–40°C to + 85°C	5V ± 5%
Military[4]	All	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}= Min., I_{OH}= –32 mA	Com'l	2.0			V
		V_{CC}= Min., I_{OH}= –15 mA	Com'l	2.4	3.3		V
		V_{CC}= Min., I_{OH}= –12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}= Min., I_{OL}= 64 mA	Com'l		0.3	0.55	V
		V_{CC}= Min., I_{OL}= 32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}= Min., I_{IN}= –18 mA			–0.7	–1.2	V
I_I	Input HIGH Current	V_{CC}= Max., V_{IN}= V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}= Max., V_{IN}= 2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}= Max., V_{IN}= 0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				–10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}= Max., V_{OUT}= 0.0V		–60	–120	–225	mA
I_{OFF}	Power-Off Disable	V_{CC}= 0V, V_{OUT}= 4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25˚C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN}\leq$0.2V, $V_{IN}\geq V_{CC}$–0.2V	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.7	1.4	mA
		V_{CC}=Max.,50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	1.6	3.2[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at f_1=2.5 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND,V_{IN}=3.4V or V_{IN}=GND	4.1	13.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	Test Load	FCT827AT				Unit	Fig. No.[13]
			Military		Commercial			
			Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Y	C_L=50 pF R_L=500Ω	1.5	9.0	1.5	8.0	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay D to Y[12]	C_L=300 pF R_L=500Ω	1.5	17.0	1.5	15.0	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	13.0	1.5	12.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y[12]	C_L=300 pF R_L=500Ω	1.5	25.0	1.5	23.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y[12]	C_L=5 pF R_L=500Ω	1.5	9.0	1.5	9.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	10.0	1.5	10.0	ns	1, 7, 8

Parameter	Description	Test Load	FCT827CT		Unit	Fig. No.[13]
			Commercial			
			Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Y	C_L=50 pF R_L=500Ω	1.5	4.4	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay D to Y[12]	C_L=300 pF R_L=500Ω	1.5	10.0	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	7.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y[12]	C_L=300 pF R_L=500Ω	1.5	14.0	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y[12]	C_L=5 pF R_L=500Ω	1.5	5.7	ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	6.0	ns	1, 7, 8

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT827CTQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT827CTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY74FCT827ATQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT827ATSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
9.0	CY54FCT827ATLMB	L64	28-Square Leadless Chip Carrier	Military

Notes:
12. Minimum limits are specified but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.

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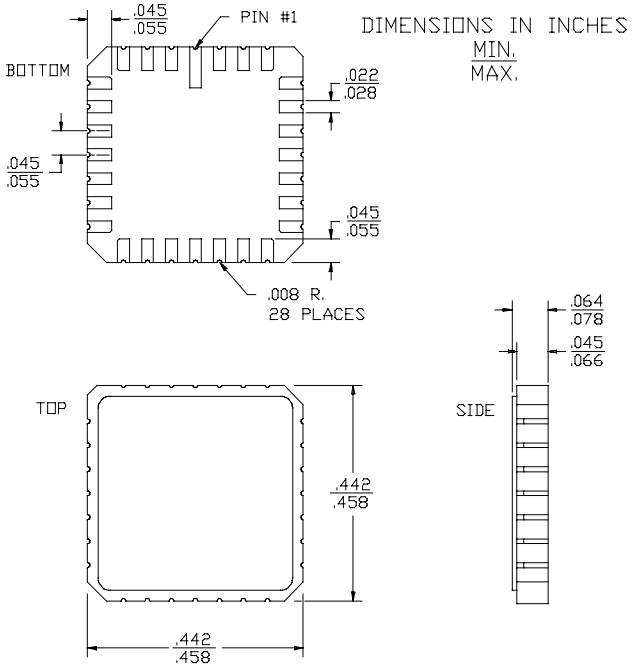
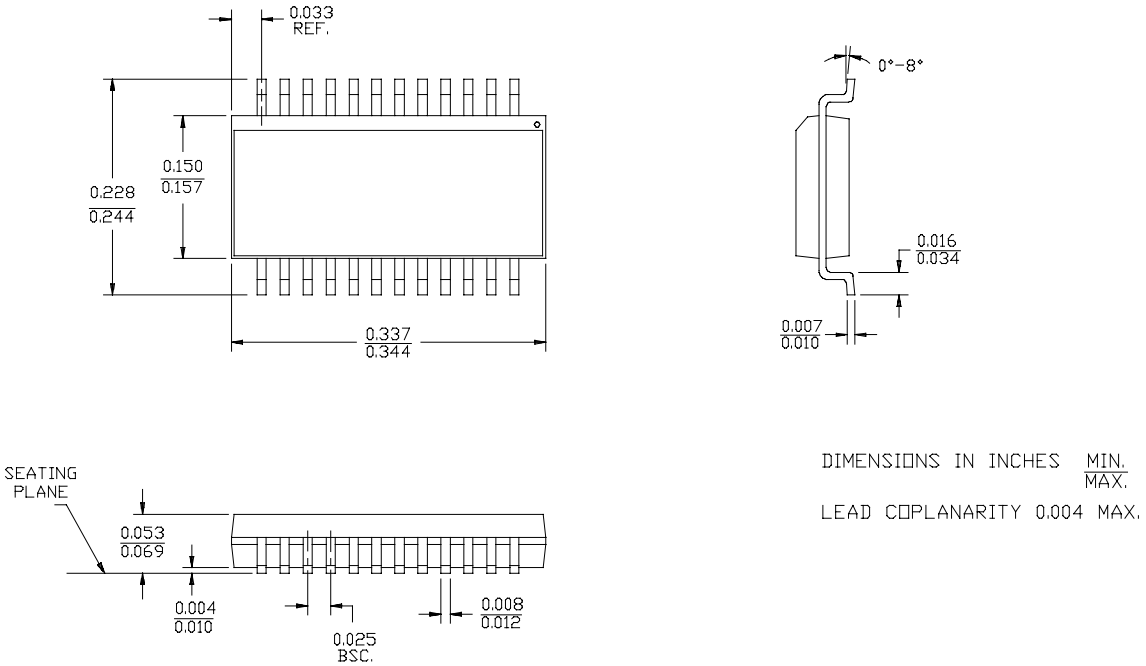
Package Diagrams

28-Square Leadless Chip Carrier L64
MIL-STD-1835 C-4



24-Lead Quarter Size Outline Q13

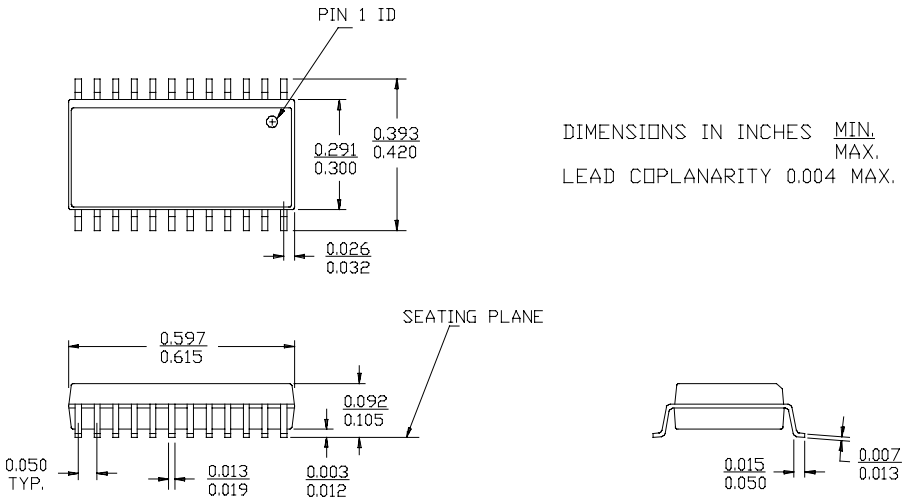


DIMENSIONS IN INCHES MIN. / MAX.

LEAD COPLANARITY 0.004 MAX.

Package Diagrams (continued)

24-Lead (300-Mil) Molded SOIC S13



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